

A

B

C

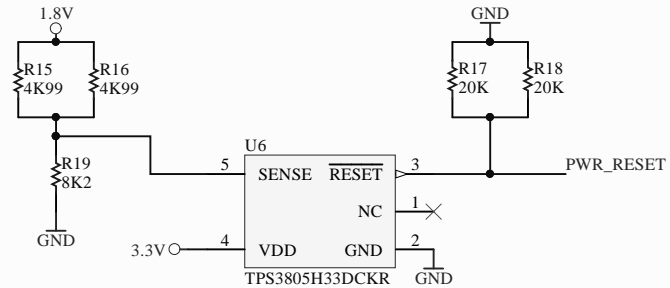
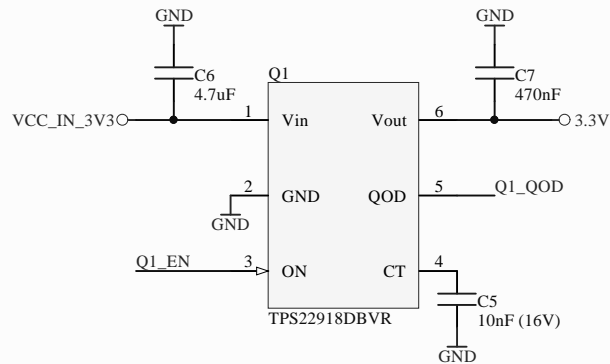
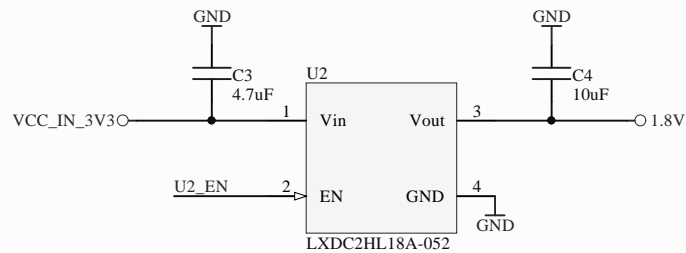
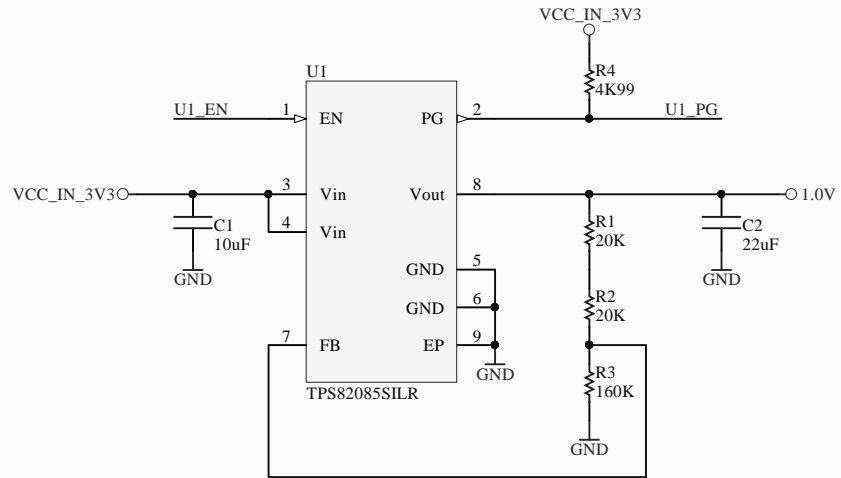
D

A

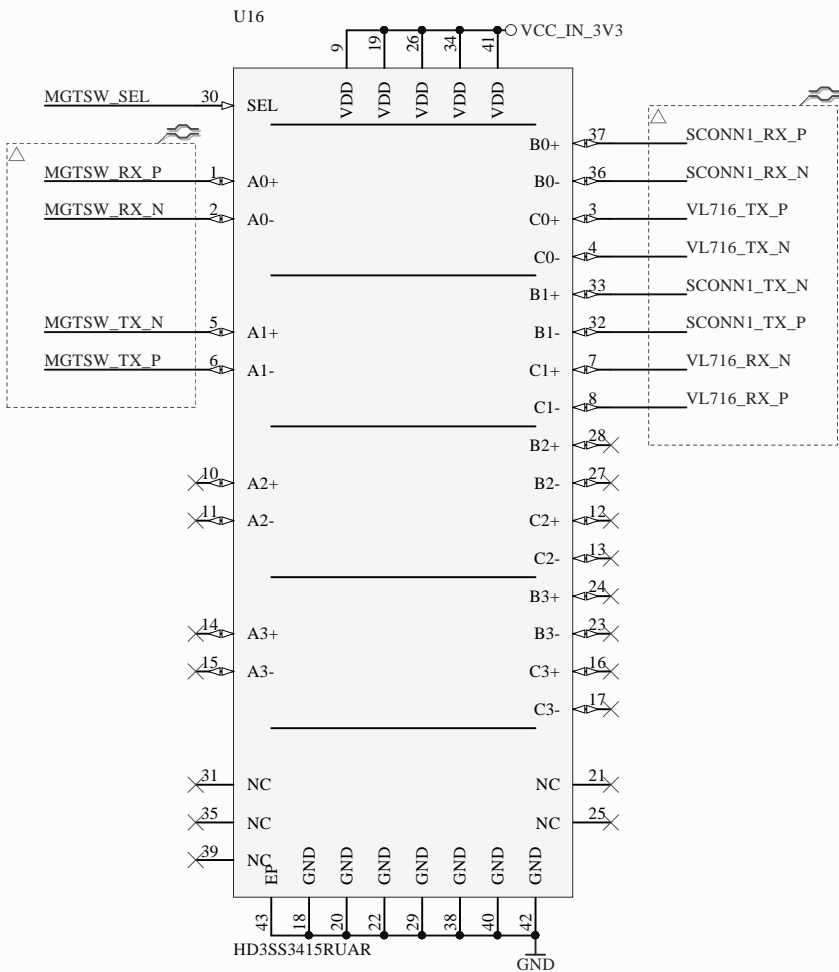
B

C

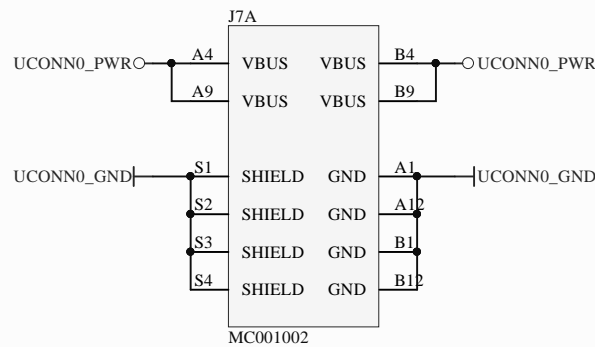
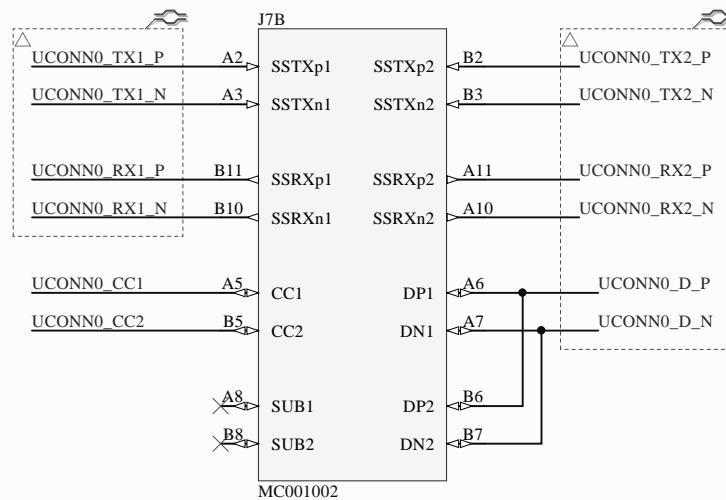
D



Title FPGA main power		
Size A4	Number	Revision
Date: 22.03.2018	Sheet of	
File: C:\Users\...\Sheet1.SchDoc	Drawn By:	



Title Multigigabit switch		
Size A4	Number	Revision
Date: 22.03.2018	Sheet of	
File: C:\Users\...\Sheet10.SchDoc	Drawn By:	



Title USB connection		
Size A4	Number	Revision
Date: 22.03.2018	Sheet of	
File: C:\Users\...\Sheet11.SchDoc	Drawn By:	

A

B

C

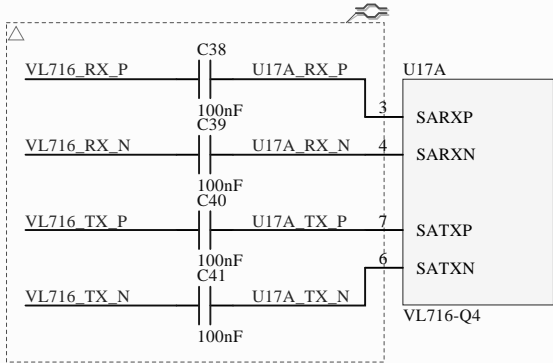
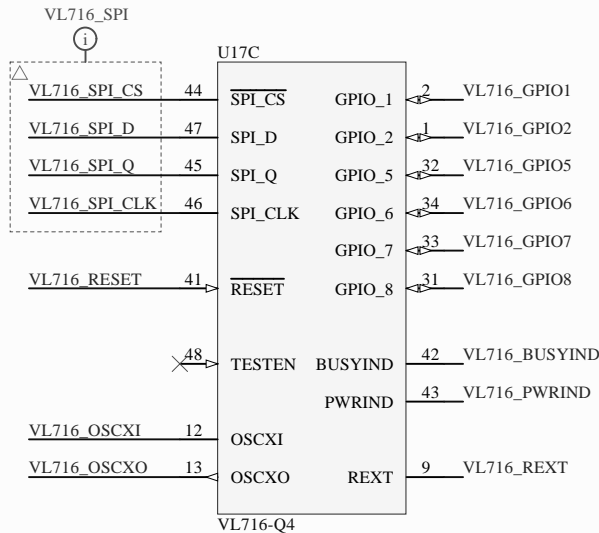
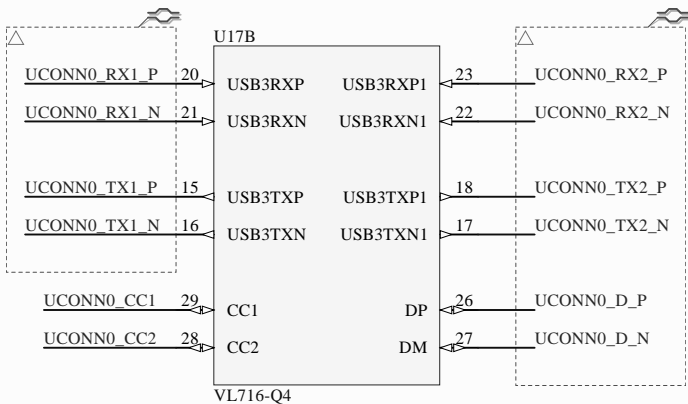
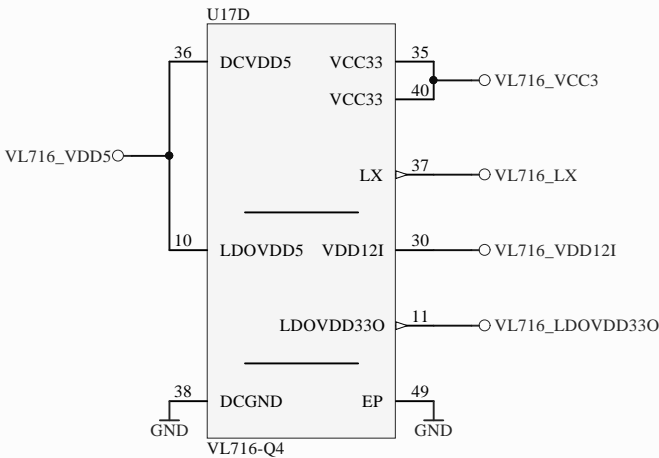
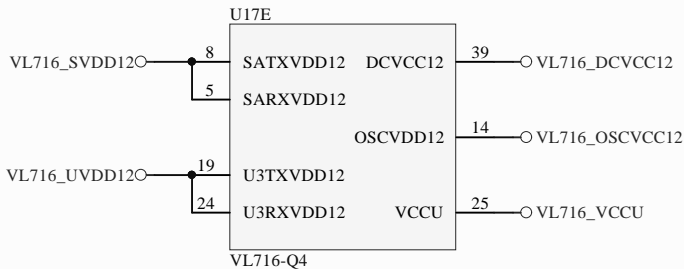
D

A

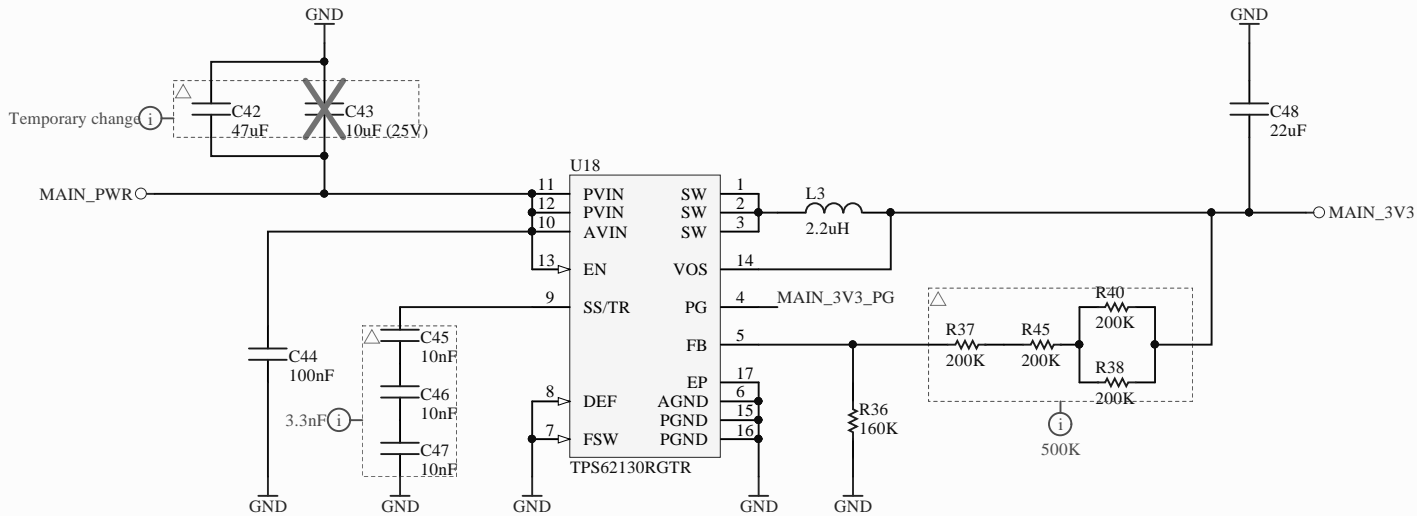
B

C

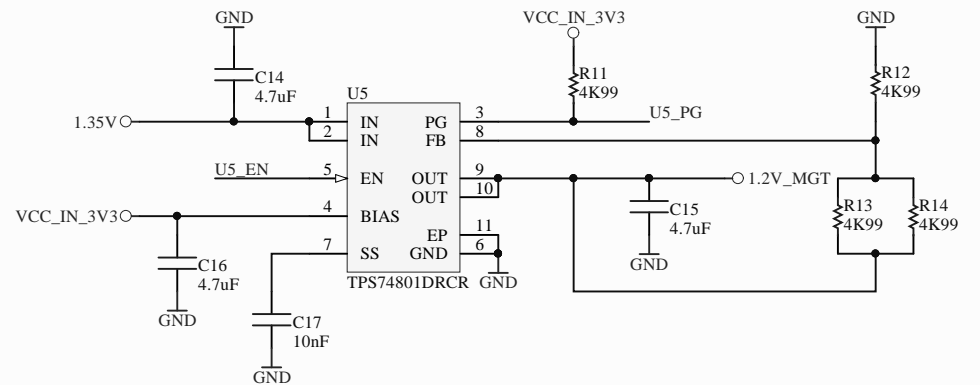
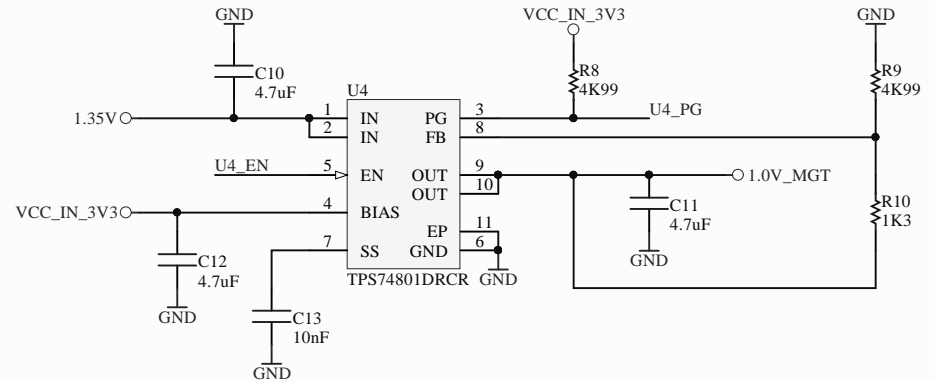
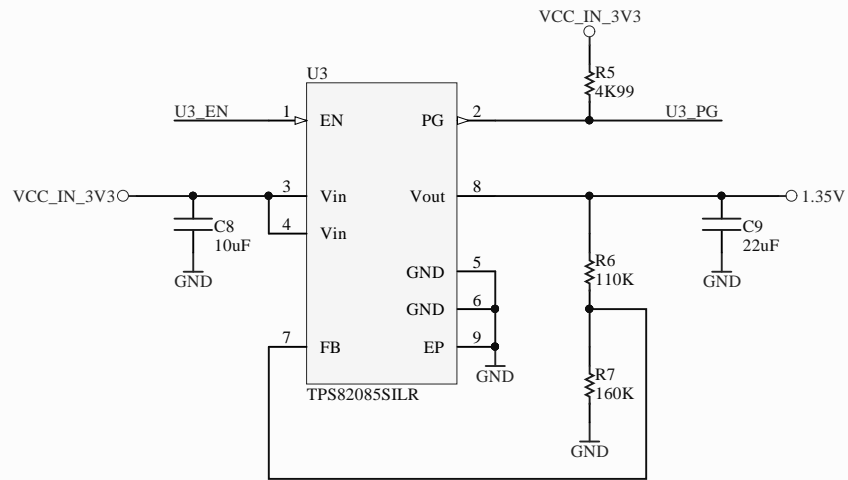
D



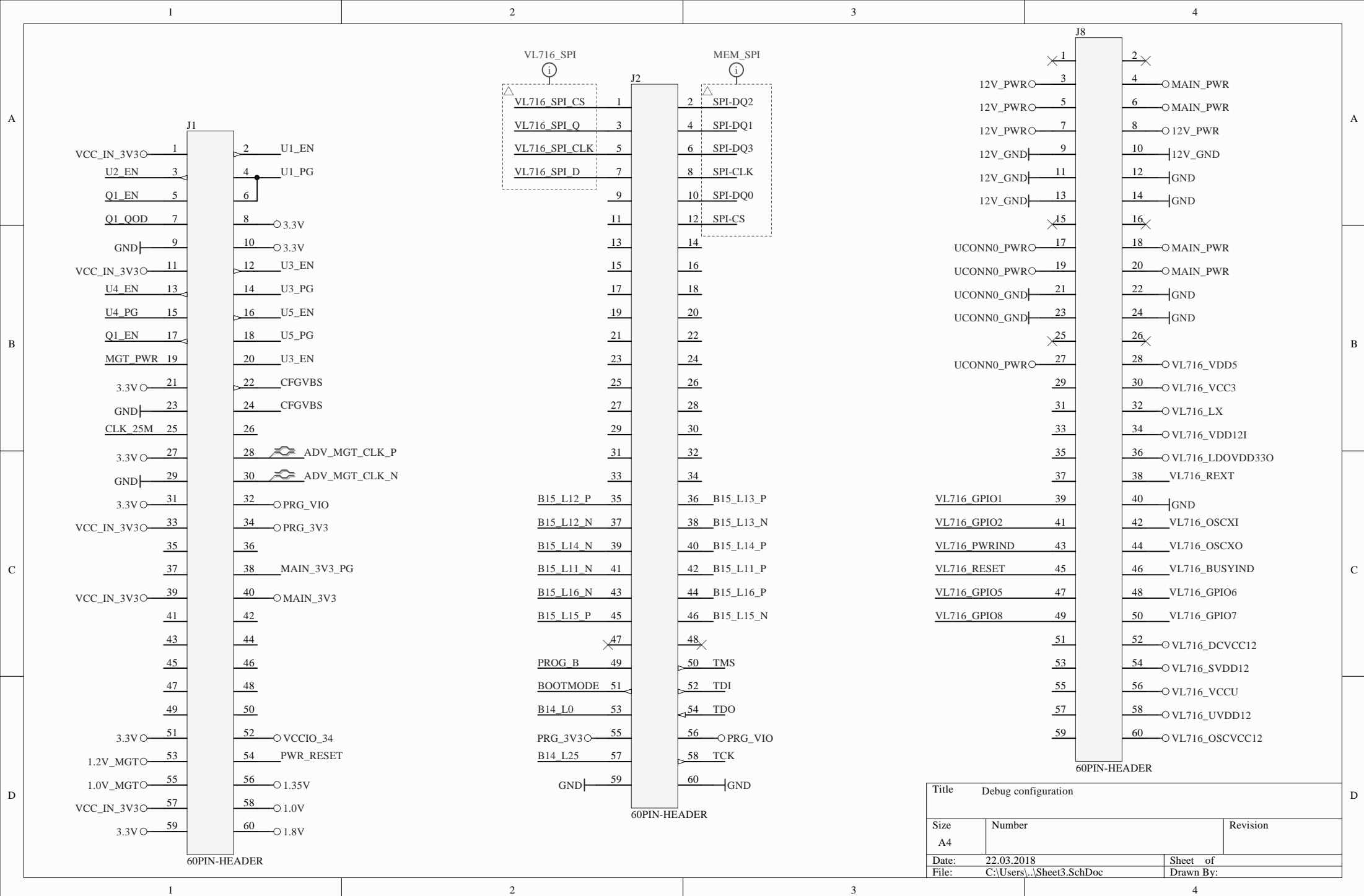
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Size A4	Number	Revision
Date: 22.03.2018	Sheet of	
File: C:\Users\...\Sheet12.SchDoc	Drawn By:	

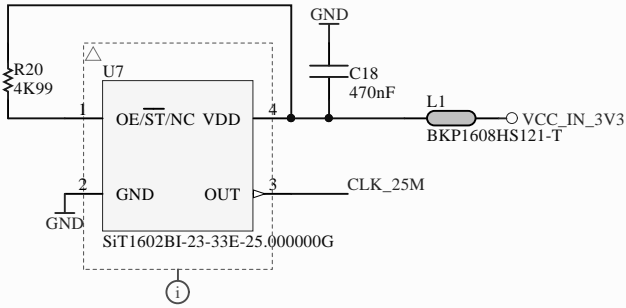


Title Digital power scheme		
Size A4	Number	Revision
Date: 22.03.2018	Sheet of	
File: C:\Users\...\Sheet13.SchDoc	Drawn By:	

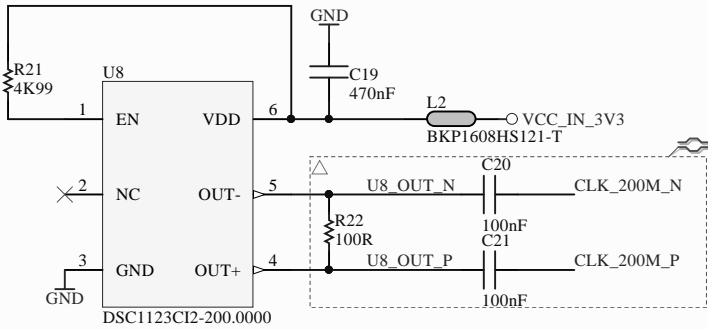


Title		MGT power	
Size	Number		Revision
A4			
Date:	22.03.2018		Sheet of
File:	C:\Users\...\Sheet2.SchDoc		Drawn By:





!!! Low Frequency stability for VL716



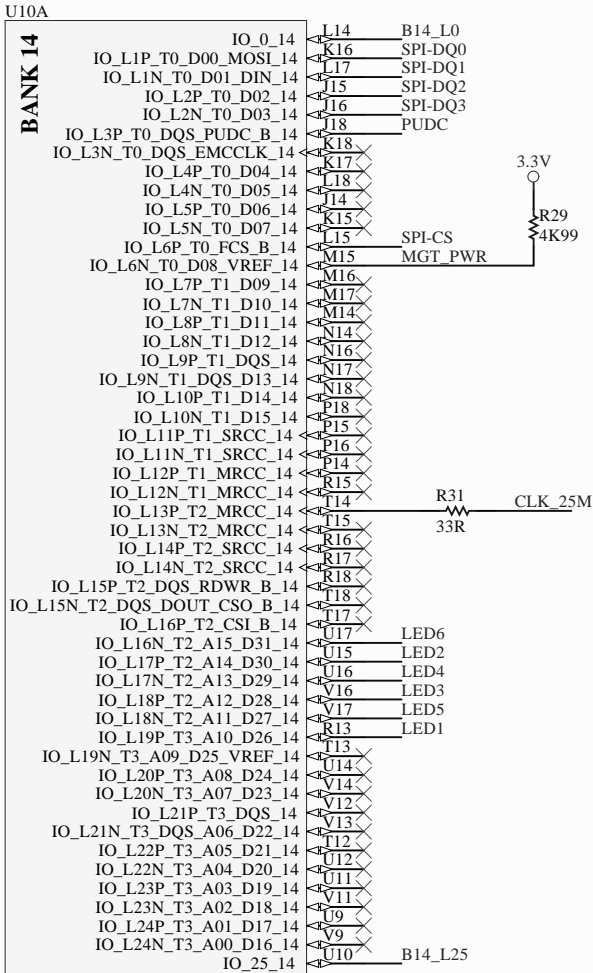
Title Clock resources		
Size A4	Number	Revision
Date:	22.03.2018	Sheet of
File:	C:\Users\...\Sheet4.SchDoc	Drawn By:

A

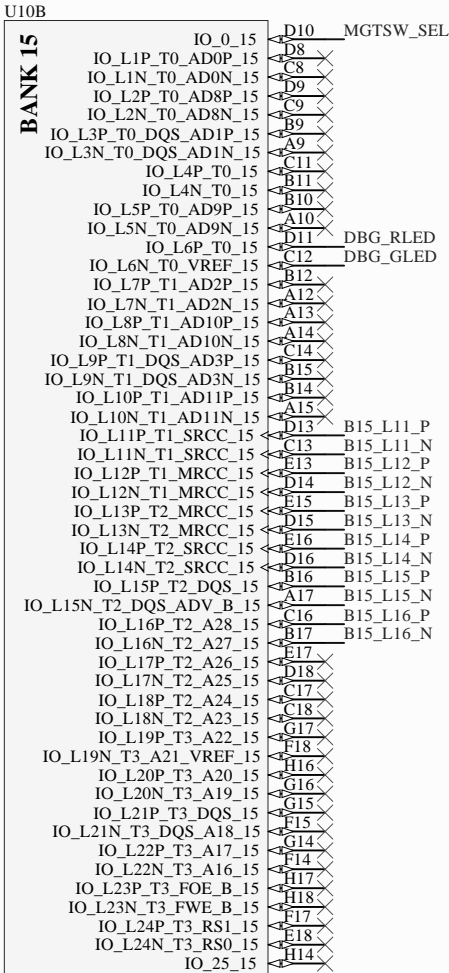
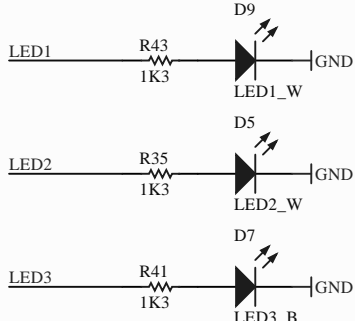
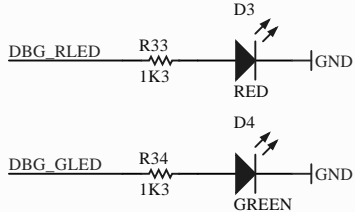
B

C

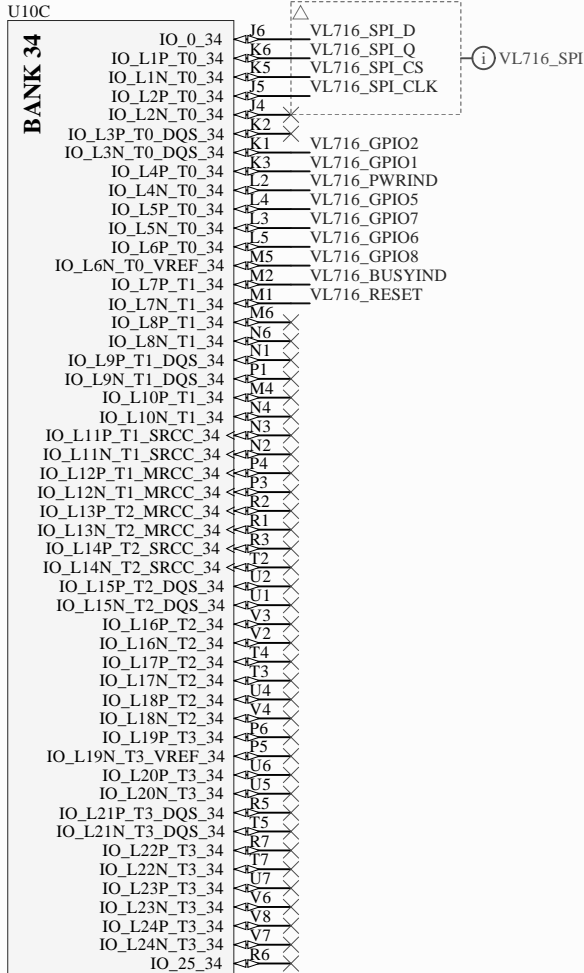
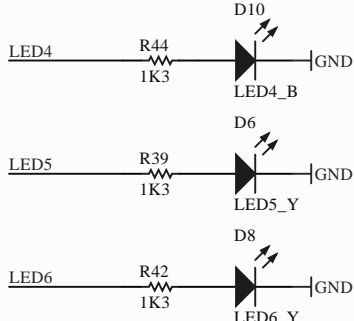
D



XC7A35T-2CSG3251



XC7A35T-2CSG3251



XC7A35T-2CSG3251

Title FPGA IO banks		
Size A4	Number	Revision
Date: 22.03.2018	Sheet of	
File: C:\Users\...\Sheet5.SchDoc	Drawn By:	

A

A

B

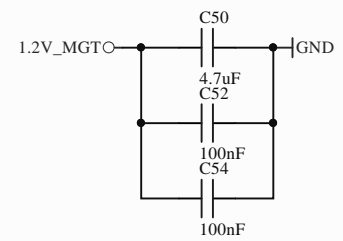
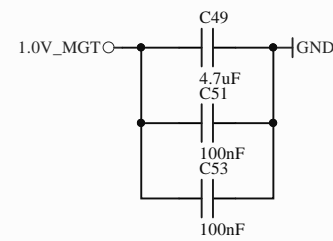
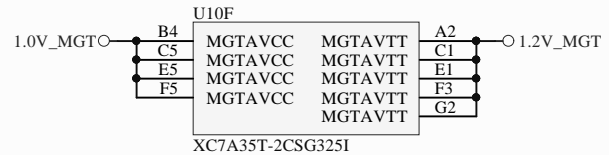
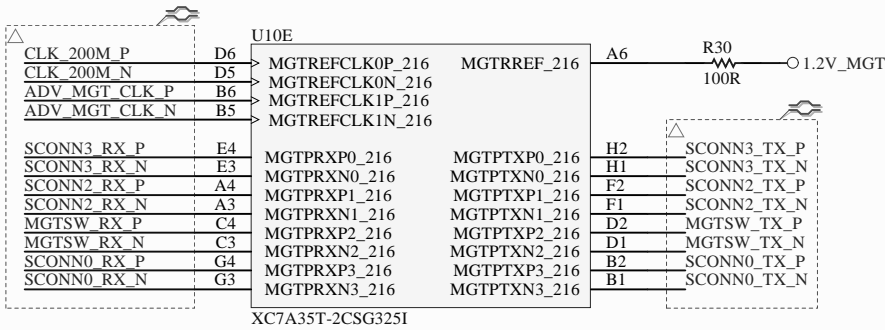
B

C

C

D

D



Title FPGA MGT resources		
Size A4	Number	Revision
Date: 22.03.2018	Sheet of	
File: C:\Users\...\Sheet6.SchDoc	Drawn By:	

A

B

C

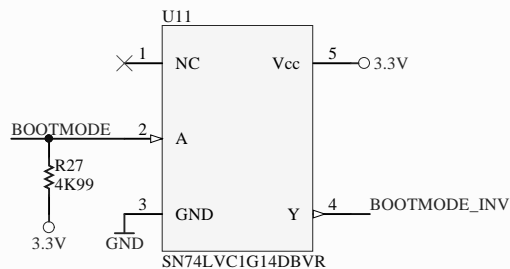
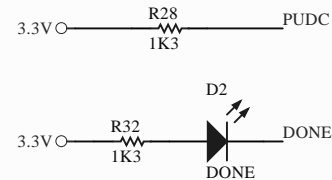
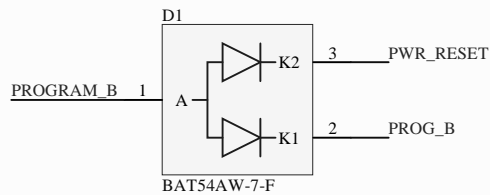
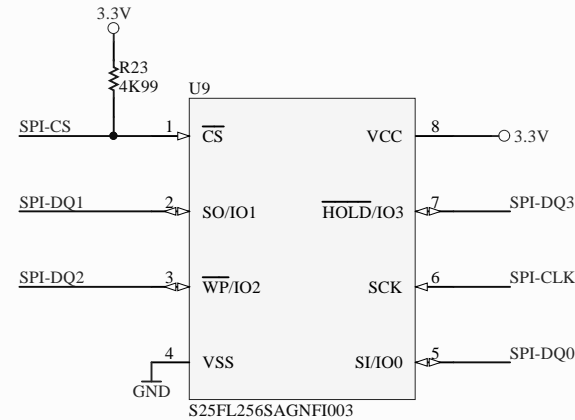
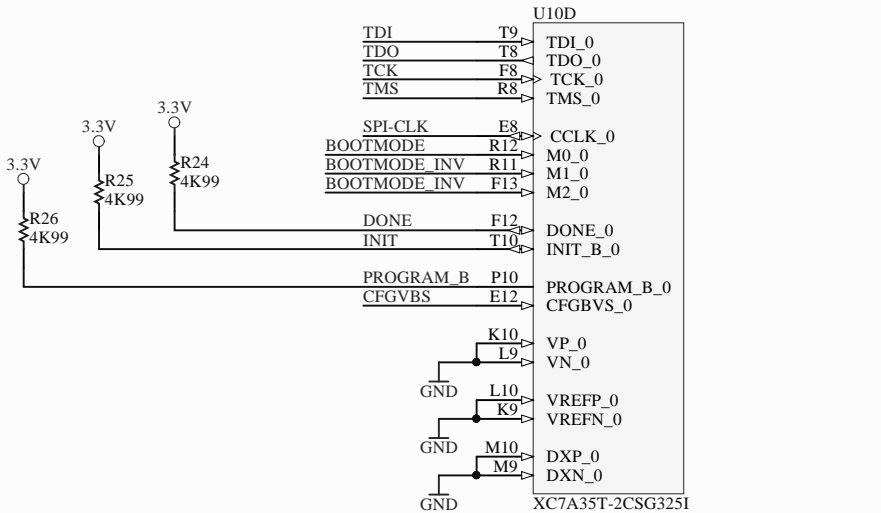
D

A

B

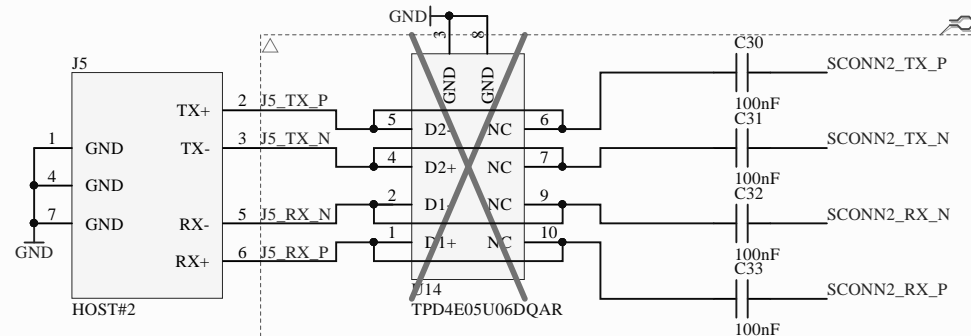
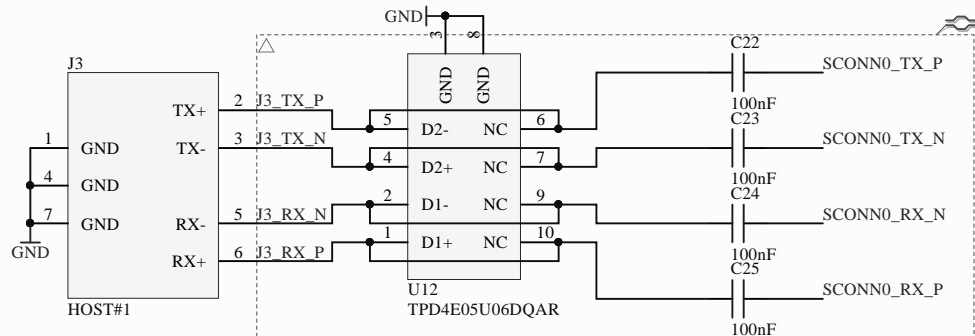
C

D



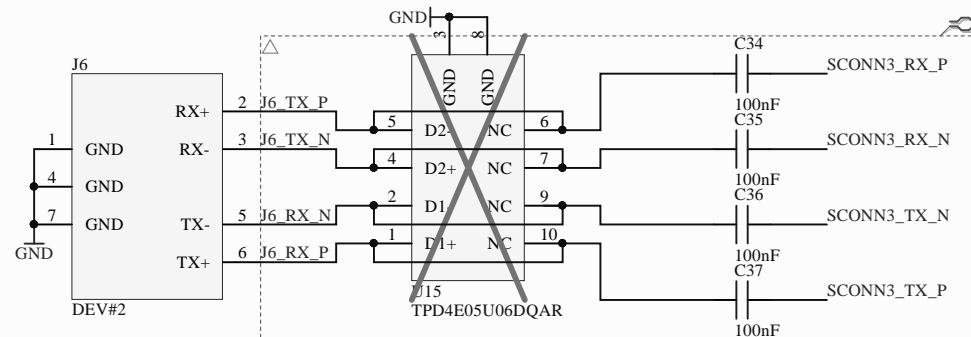
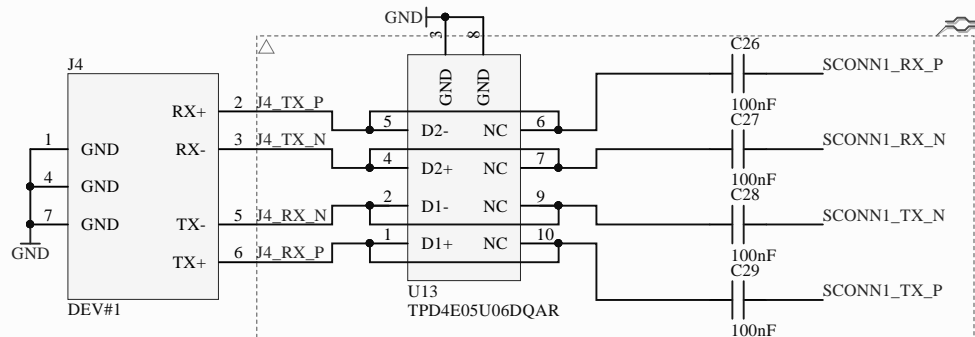
Title FPGA configuration scheme		
Size A4	Number	Revision
Date: 22.03.2018	Sheet of	
File: C:\Users\...\Sheet7.SchDoc	Drawn By:	

A



A

B



B

C

C

D

D

Title SATA connections		
Size A4	Number	Revision
Date: 22.03.2018	Sheet of	
File: C:\Users\...\Sheet9.SchDoc	Drawn By:	