Progress Report Checkpoint

For this checkpoint, Yvonne worked on the data and control hazard detection designs.

For this checkpoint, Matthew worked on the design of the arbiter and the forwarding logic.

- the functionalities you implemented
- the testing strategy you used to verify these functionalities
- the timing and energy analysis of your design: fmax & energy report from Quartus

Testing Strategies

We started out by using the given test code to make sure our datapath worked correctly.

Road map

The features that must be completed for the next checkpoint are the Integration of L1 caches, Arbiter, Hazard detection & forwarding, and static branch predictor.

- Yvonne will work on implementing and verifying the static branch predictor.
- Shunfan will work on Arbiter design with the given cache.
    - The arbiter sits between CPU and cache.
    - The arbiter will communicate with both instruction and data cache.
    - The arbiter handles memory requests and determines priority.
- Matthew will work on implementing the forwarding and hazard control.

Timing and Energy Analysis

- Slow 900mV 100C Model Fmax: 123.49 MHz