

SHUO LI

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OBJECTIVE	Seeking an entry-level full-time or intern position as a software engineer	
EDUCATION	University of Illinois at Urbana-Champaign	Urbana, IL
	M.S. in Electrical and Computer Engineering , GPA: 3.45/4.00	May 2015
	University of Illinois at Urbana-Champaign	Urbana, IL
	B.S.(Honors) in Electrical Engineering , GPA: 3.58/4.00	May 2013
WORK EXPERIENCE	University of Illinois at Urbana-Champaign	Urbana, IL
	<i>Research Assistant, advised by Prof. Jose Schutt-Aine</i>	Mar. 2014 - Present
	<ul style="list-style-type: none">Implemented a Traditional Digital Direct Synthesizer (DDS) on FPGASimulated in ModelSim and investigated the sources of spurious signals in theoryDesigned and implemented a Truncation Spurs-Free Structure of DDS on FPGA and verified the spurs reduction with oscilloscope and spectrum analyzer	
	<i>Teaching Assistant, ECE 385 Digital Systems Laboratory</i>	Aug. 2013 - Present
PROJECT EXPERIENCE	Database: Web-based CS Course Registration System	Sep. - Dec. 2014
	<ul style="list-style-type: none">Analyzed client requirements, specified system functionalities, identified integrity constraints and designed the conceptual database with E-R diagramsNormalized database schemas to 3NF, which reduced redundancies in the databaseWrote a parser with Python scripts to read and extract raw data from UIUC course website; documented data into XML files, then populated the MySQL database; wrote PHP scripts to query databaseDeveloped the user interface and webpage with HTML/CSS and JavaScript	
	Real-Time Systems: Android App-Remote Robot Control	Sep. - Dec. 2013
	<ul style="list-style-type: none">Programmed an iRobot (Roomba) control commands prototype with PythonDeveloped an application with Java on an android phone to control the robotImplemented voice control function in the android application	
	VLSI Design: Microprocessor Design and Layout	Sep. - Dec. 2012
	<ul style="list-style-type: none">Designed, implemented, simulated, and laid out a 16-bit microprocessor datapath (Am2901 250nm) with Cadence Virtuoso and designed the controller in VerilogDeveloped test benches for functional verification with NC-Verilog simulatorMinimized the layout area by optimizing logic design, floorplanning, and routingPerformed physical verification (DRC and LVS) for each layout with Cadence	
SKILLS	Languages	proficient: C++, Java, Python; basic: C
	Web Prog	proficient: JavaScript/jQuery, HTML/CSS; basic: SQL
	HDL/HVL	proficient: Verilog/SystemVerilog; basic: VHDL
	Tools	Eclipse, Visual Studio, Xcode, Git
	Softwares	Cadence, Quartus II, ModelSim
	academic and teaching experience in FPGA, Oscilloscope, Spectrum Analyzer	
COURSES & INDEPENDENT STUDIES	Data Structures, Database Systems, Real-Time Systems, Web Programming, VLSI System Design, System on Chip Design, Digital Systems Laboratory, IC Device Theory and Fabrication, Digital Signal Processing, Predictive Data Analytics	