Shuo Li

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Objective

Seeking an entry-level **full-time** or **intern** position as a software engineer

Education

University of Illinois at Urbana-Champaign Urbana, IL
M.S. in **Electrical and Computer Engineering**, GPA: 3.45/4.00 May 2015

University of Illinois at Urbana-Champaign Urbana, IL
B.S.(Honors) in **Electrical Engineering**, GPA: 3.58/4.00 May 2013

Work Experience

University of Illinois at Urbana-Champaign Urbana, IL
Research Assistant, advised by Prof. Jose Schutt-Aine Mar. 2014 - Present

- Implemented a Traditional Digital Direct Synthesizer (DDS) on FPGA
- Simulated in ModelSim and investigated the sources of spurious signals in theory
- Designed and implemented a Truncation Spurs-Free Structure of DDS on FPGA and verified the spurs reduction with oscilloscope and spectrum analyzer

Teaching Assistant, ECE 385 Digital Systems Laboratory Aug. 2013 - Present

Project Experience

Database: Web-based CS Course Registration System Sep. - Dec. 2014

- Analyzed client requirements, specified system functionalities, identified integrity constraints and designed the conceptual database with E-R diagrams
- Normalized database schemas to 3NF, which reduced redundancies in the database
- Wrote a parser with Python scripts to read and extract raw data from UIUC course website; documented data into XML files, then populated the MySQL database; wrote PHP scripts to query database
- Developed the user interface and webpage with HTML/CSS and JavaScript

Real-Time Systems: Android App-Remote Robot Control Sep. - Dec. 2013

- Programmed an iRobot (Roomba) control commands prototype with Python
- Developed an application with Java on an android phone to control the robot
- Implemented voice control function in the android application

VLSI Design: Microprocessor Design and Layout Sep. - Dec. 2012

- Designed, implemented, simulated, and laid out a 16-bit microprocessor datapath (Am2901 250nm) with Cadence Virtuoso and designed the controller in Verilog
- Developed test benches for functional verification with NC-Verilog simulator
- Minimized the layout area by optimizing logic design, floorplanning, and routing
- Performed physical verification (DRC and LVS) for each layout with Cadence

Skills

Languages	**proficient**: Python, Java; **basic**: C/C++
Web Prog	**proficient**: JavaScript/jQuery, HTML/CSS, SQL
HDL/HVL	**proficient**: Verilog/SystemVerilog; **basic:** VHDL
Tools	Eclipse, Visual Studio, Xcode, Git
Softwares	Cadence, Quartus II, ModelSim

academic and **teaching** experience in FPGA, Oscilloscope, Spectrum Analyzer

Selected Courses

Data Structures, Database Systems, Real-Time Systems, Web Programming, VLSI System Design, System on Chip Design, Digital Systems Laboratory, IC Device Theory and Fabrication, Digital Signal Processing, Wireless Communication Systems