Department of Computer Science and Engineering

NITK, Surathkal

CO202 – Design of Digital Systems [B. Tech, 3rd Semester]

(Syllabus and Assessment)

Semester: III [S1 & S2] **Academic Year:** 2017-18 **Credits:** (3-1-0) 4

I. Syllabus [Total No. of Hours: 40]

Sl. No.	Topic	Detail	No. of Hrs.
1	Switching algebra and logic circuits.	Binary System, Boolean Algebra and Logic Gates, Simplification of Boolean Functions	10
2	Combinational and sequential circuits and their algorithmic synthesis.	Combinational Logic, Combinational Logic with MSI and LSI, Synchronous Sequential Logic, Registers, Counters, Memory Unit Register Transfer Logic, Asynchronous sequential logic	10
3	Logic optimization: two level, multi level, circuits.	Digital Integrated Circuits	5
4	Computer aided synthesis and optimization. (introduction)	-	5
5	Hardware modelling using VHDL.	-	2
6	Introduction to VLSI design: MOS devices, system level design.	-	5
7	Introduction to VLSI testing: fault models, testing combination and sequential circuits.	-	3

Text Books:

Morris Mano, Digital Logic and Computer Design.

Alan B. Marcovitz, Intro. To Logic Design, TMH, 2002.

Giovanni De Micheli, Synthesis and Optimization of Digital circuits, 2000.

Zvi Kolavi, Switching and finite automata theory, Tata McGraw Hill 2000.

II. Assessment

Sl. No.	Item	% of Marks	Remarks
1	End-Sem Examination	45 %	-
2	Mid-Sem Examination	20 %	-
3	Surprise Test	10 %	2 Test for 10 marks each and average is the final marks.
4	Mini-Project	25 %	5 % - Abstract, 10 % - Regular Progress and 10% - Final Demo.

Course Instructor
B. R. Chandavarkar [S1]
Sushmita Kamble [S2]

Secretary
(DUGC)

Chairman
(DUGC)

Department of Computer Science and Engineering

NITK, Surathkal

CO204 – Design of Digital Systems Lab [B. Tech, 3rd Semester]

(Syllabus and Assessment)

Semester: III [S1 & S2] **Academic Year:** 2017-18 **Credits:** (0-0-3) 4

A. Syllabus

Module I (Venue: Computer Lab)

(Number Systems Using C Programming)

1. Write a C program to perform $(input)_x$ to $(output)_y$.
2. Write a C program to find 'x' and 'y' with respect to $(number1)_x = (number2)_y$, where, number1 and number2 are the inputs.
3. Write a C program to perform addition, subtraction, multiplication and division on $(number1)_x$ and $(number2)_x$.
4. Write a C program to perform 'x' and 'x-1'complemention of $(number)_x$.
5. Write a C program to prove the self-complementing property a weighted number system.

Module II (Venue: Digital Lab)

(Combinational and Sequential Circuits Using **Hardware**)

1. Verify the truth table for Basic (AND, OR, NOT), Universal (NAND, NOR) and Advanced logic gates (EXOR, EXNOR) using a digital IC trainer kit.
2. Implement – (i) Basic gates using universal gates. (ii) NAND gate using NOR gate and (iii) NOR gate using NAND gate.
3. Implement to find r's and (r-1)'s complement of a given number using Universal gates only.
4. Implement a given Boolean function using (i) 1 or 2 input basic gates (ii) universal gates, after simplification using Boolean algebra, K-map.
5. Implement
   (i) Grey code to Binary code and vice versa.
   (ii) Excess-3 to BCD code and vice versa.
   (iii) Output binary number equal to the square of the input number.
   (iv) 9's complement of decimal equivalent of BCD.
   and so on.

6. Implement – (i) Half Adder (ii) Half Subtractor (iii) Full Adder (iv) Full Subtractor

7. Implement, (i) 4-bit adder using decoder
   (ii) 4-bit adder using multiplexer
   (iii) 4-bit subtractor using decoder
   (iv) 4-bit subtractor using multiplexer
   and so on.

8. Flip-flops truth table verification.

9. Implement, (i) synchronous and asynchronous counter
   (ii) Johnson counter
   (iii) Ripple counter
   (iv) Register

10. Hardware implementation for the given statements.

Module III (Venue: Computer Lab)

(Combinational and Sequential Circuits Design using **Logisim** and **Verilog**)

1. Verify the truth table for Basic (AND, OR, NOT), Universal (NAND, NOR) and Advanced logic gates (EXOR, EXNOR) using a digital IC trainer kit.

2. Implement – (i) Basic gates using universal gates. (ii) NAND gate using NOR gate and (iii) NOR gate using NAND gate.

3. Implement to find r's and (r-1)'s complement of a given number using Universal gates only.

4. Implement a given Boolean function using (i) 1 or 2 input basic gates (ii) universal gates, after simplification using Boolean algebra, K-map.

5. Implement
   (i) Grey code to Binary code and vice versa.
   (ii) Excess-3 to BCD code and vice versa.
   (iii) Output binary number equal to the square of the input number.
   (iv) 9's complement of decimal equivalent of BCD.
   and so on.

6. Implement – (i) Half Adder (ii) Half Subtractor (iii) Full Adder (iv) Full Subtractor

7. Implement, (i) 4-bit adder using decoder

(ii) 4-bit adder using multiplexer

(iii) 4-bit subtractor using decoder

(iv) 4-bit subtractor using multiplexer

and so on.

8. Flip-flops truth table verification.
9. Implement. (i) synchronous and asynchronous counter

(ii) Johnson counter

(iii) Ripple counter

(iv) Register

10. Hardware implementation for the given statements.

B. Weekly Planning

Sl. No./ Week No.	Dates	To be Completed	Remarks
1	July 31 – Aug 04	Module I (C Program)	-
2	Aug 07 – Aug 11	Module I (C Program)	Lab Record
3	Aug 14 – Aug 18	Module II (1, 2 & 3)	-
4	Aug 21 – Aug 25	Module II (4 & 5)	Lab Record
5	Aug 28 – Sep 01	Module II (6 & 7)	Lab Record
6	Sep 04 – Sep 08	Module II (8 & 9)	Lab Record
7	Sep 11 – Sep 15	Theory Mid-Sem Examination	-
8	Sep 18 – Sep 22	Module II (10)	Lab Record
9	Sep 25 – Sep 29	Laboratory Mid-Sem Examination	Max. Marks: 25
10	Oct 02 – Oct 06	Module III (1, 2, 3 & 4)	-
11	Oct 09 – Oct 13	Module III (5, 6 & 7)	Lab Record
12	Oct 16 – Oct 20	Module III (8 & 9)	Lab Record
13	Oct 23 – Oct 27	Module III (10)	Lab Record
14	Oct 30 – Nov 03	Mini-Project	Progress 1
15	Nov 06 – Nov 10	Mini-Project	Progress 2
16	Nov 13 – Nov 16	Laboratory End-Sem Examination	Exam & Mini-Project

Note:

1. Module I, lab record should contain handwritten flowchart, program and output.
2. Module II, lab record should contain hand drawn circuit diagram.

3. **Module III, lab record should contain handwritten code.**

4. **Irrespective of holidays, students should strictly follow the weekly plan with the extra laboratories.**

C. Assessment Scheme

Sl. No.	Item	% of Marks	Remarks
1	End-Sem Examination	50	Viva – 10 % Question 1 – 20 % Question 2 – 20%
2	Mid-Sem Examination	25	Viva – 5 % Question 1 – 20 %
3	Surprise Test (2 Test)	15	Viva – 5 % Question 1 – 10 %
4	Regular Lab Activity	10	Best 5 Marks

Course Instructor DUGC H.O.D