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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

A Mini Project report on

"DIGITAL CLOCK USING COUNTER"

Submitted in partial fulfillment for the award of degree of Bachelor of Engineering in Electronics and Communication Engineering

Submitted by

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Under the Guidance of

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B.L.D.E. Association's

V.P Dr. P.G HALAKATTI COLLEGE OF ENGINEERING AND TECHNOLOGY, VIJAYAPUR

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is Certified that the Mini project work entitled **"Digital Clock Using Counter"** carried out by **Savitri Suresh Holakar, Shweta Benawadi, Swarnagouri S Ramapur, Swati Goudappanavar,** bonafide students of **VP Dr P.G Halakatti College of Engineering and Technology, Vijayapura** in partial fulfillment for the award of **Bachelor of Engineering** in **Electronics and Communication Engineering** of the **Visvesvaraya Technological University, Belgaum** during the year 2024-2025. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the departmental library. The Mini project report has been approved as it satisfies the academic requirement in respect of Mini project work prescribed for the said degree.

GUIDE	H.O.D	PRINCIPAL
Prof. V C SAJJANAR	Dr. UMESH DIXIT	Dr. V. G. SANGAM

B.L.D.E. Association's
VACHANA PITAMAHA Dr. P.G. HALAKATTI COLLEGE OF ENGINEERING & TECHNOLOGY, VIJAYAPURA

DEPARTMENT OF ELECTRONICS & COMMINUCATION ENGINEERING

DECLARATION

We, students of Fifth semester B.E, at the department of Electronics & Communication Engineering, hereby declare that, the Mini Project entitled " **Digital Clock Using Counter** ",embodies the report of our mini project work, carried out by us under the guidance of **Prof. V C SAJJANAR,** We also declare that, to the best of our knowledge and belief, the work reported here in does not form part of any other report or dissertation on the basis of which a degree or award was conferred on an earlier occasion on this by any student.

Place:- Vijayapura Date:-

ACKNOWLEDGEMENT

The satisfaction and euphoria that accompany the successful completion of any task would be incomplete without the mention of people who made it possible, whose consistent guidance and encouragement crowned our efforts with success. We consider it as our privilege to express the gratitude to all those who guided in the completion of our Mini Project.

First and foremost, We wish to express our profound gratitude to our respected Principal **Dr. V.G. Sangam, B.L.D.E. Association's VACHANA PITAMAHA Dr. P.G. HALAKATTI COLLEGE OF ENGINEERING & TECHNOLOGY, Vijayapura** , for providing us with a congenial environment to work in.

We would like to express our sincere thanks to **Dr. U D Dixit** , the HOD of **Electronics and Communication Engineering**, **B.L.D.E.Association's VACHANA PITAMAHA Dr. P.G. HALAKATTI COLLEGE OF ENGINEERING & TECHNOLOGY, Vijayapura**, for his continuous support and encouragement.

We are greatly indebted to our guide **Prof. V C Sajjanar**, Department of **Electronics and Communication Engineering**, **B.L.D.E. Association's VACHANA PITAMAHA Dr. P.G. HALAKATTI COLLEGE OF ENGINEERING & TECHNOLOGY, Vijayapura**, who took great interest in our work. He motivated us and guided us throughout the accomplishment of this goal. We express our profound thanks for his meticulous guidance.

ABSTRACT

This project outlines the design and implementation of a digital clock using Verilog HDL. The core functionality revolves around a synchronous counter module that increments every second. This counter is integrated with logic to generate the appropriate hour, minute, and second signals. The design incorporates features such as:

Clear Functionality: A reset signal allows for clearing the clock to an initial state.
Display Module: A separate module handles the display of the time on a suitable output device (e.g., seven-segment displays, LCD).
24-Hour Format: The clock operates in 24-hour format for accurate timekeeping.
The Verilog code is synthesized and simulated using appropriate electronic design automation tools. The project demonstrates the practical application of digital design principles, including state machines, combinational logic, and the use of counters for timekeeping applications.

The Verilog code is developed using a modular approach, promoting code reusability and maintainability. The design is simulated using ModelSim or similar simulation tools to verify its functional correctness and timing behavior. Synthesis is performed using Xilinx Vivado or other synthesis tools to generate a netlist suitable for implementation on a target FPGA or ASIC. This project provides a practical demonstration of digital design principles, including synchronous design, counter implementation, frequency division, and display interfacing using Verilog HDL. It highlights the use of hardware description languages for designing and implementing real-time embedded systems.

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CHAPTER: 1

INTRODUCTION

A digital clock is a fundamental digital system that displays time in numerical format. Implementing a digital clock using Verilog and counters is a common exercise in digital design, providing a practical application of counters and sequential logic.

Basic Structure

basic structure of a digital clock using counters involves the following components:
Clock Source: A stable clock signal provides the timing reference for the entire system.
Counters: Multiple counters are used to keep track of seconds, minutes, and hours.
Display: A display unit (e.g., seven-segment displays) to show the time.
Verilog Implementation

The Verilog code for a digital clock typically includes the following modules:

- Clock Divider (Optional): If the available clock frequency is too high, a clock divider can be used to generate a slower clock signal for the counters.
- Seconds Counter: A counter that increments from 0 to 59 and then resets to 0, generating a carry-out signal every 60 seconds.
- Minutes Counter: A counter that increments every time the seconds counter generates a carry-out signal. It counts from 0 to 59 and resets to 0, generating a carry-out signal every 60 minutes.
- Hours Counter: A counter that increments every time the minutes counter generates a carry-out signal. It counts from 0 to 23 (for a 24-hour clock) or 12 (for a 12-hour clock with AM/PM indication) and resets to 0.
- Display Module: This module takes the values of the seconds, minutes, and hours counters and drives the display units to show the time.

CHAPTER 2:

LITERATURE REVIEW

Digital Clock using counter Logic By: Sheikh Md. Rabiul Islam & Md. Jobayer Hossain

Khulna University of Engineering and Technology, Bangladesh

A digital clock has been designed at gate level and is being presented in this paper. The clock architecture consists of three major blocks SECOND,MINUTE and HOUR. The architecture is the amalgam both of synchronous and asynchronous logic. All the flip-flops at each block run synchronously. The triggering operation of a block is asynchronous in nature. It serves the design requiring lower power consumption, provides lesser noise and electromagnetic interference, lower delay and greater throughput. The clock is designed at Xilinx System Generator, synthesized with Xilinx Synthesis Tool (XST) and Simulated by Vegilogger Pro 6.5.

Digital clock with Myanmar digits: Khant Win, Alexey N Yakunin, Aung Myo San, Nyan Linn Phyo

2020 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (ElConRus), 1978- 1982, 2020

A digital clock is a type of electronic clock that displays the time digitally. This clock is more reliable, accurate,maintenance free and portable than mechanical clock. Usually, digital clocks are associated with electronic devices and widely used in everyday of human life.Although there are many digital clocks with 7-segment digits, a clock that displays Myanmar digits is very rarely.

This paper deals with circuit implementation of a digital clock that allows displaying Myanmar digits. In this work a circuit of Myanmar-digit decoder is proposed. A control scheme is designed to display Myanmar digits on 8*8-LED matrix. Schemes of 0-5, 0-9 and 0-23 up-counters are synthesized for counting the time of the clock. Using the combination of the considered devices, a digital clock with Myanmar digits is developed and its circuit is modeled in Altera Quartus-Il environment. The reliability of the result of the developed digital clock is practically confirmed by using Altera DE-1 board and 8*8-LED matrixes (1588BS).

A Study on Design and Construction of a Digital Clock System:

Dr. Sanjeev Reddy K. Hudgikar ,Dr. Prashant G. Kamble

Instead of showing the time by moving hands as in an analogue clock, this project's digital clock displays it digitally, in numerical form (i.e., in numbers). Using 555 timers, this digital timer circuit was designed and implemented, and the results are documented. The project's initial design criteria were to have a digital output, and to count from seconds to minutes and then hours. Either an op-amp or a 555 timer should be included. Research into analogue electronic circuits of a similar nature led to the discovery of a good starting point for digital circuits. A digital timer circuit was built utilising a 555 timer, 74LS90 binary counters, 74LS47 IC, and 7 segment display outputs.

A Review of Design of Digital Clock Based on Verilog HDL : Wangtingli Li , Shuhui Li , Qingyan Zeng , Chengxi Zhou

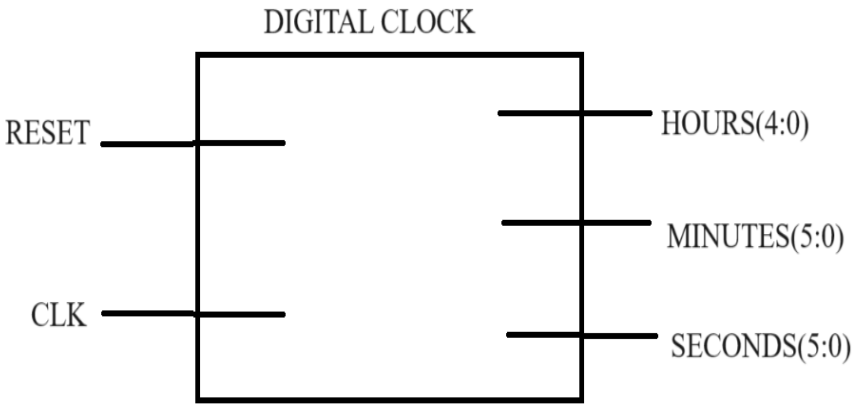
This paper mainly discusses how to use Verilog HDL to design a simple digital clock and realize the basic functions such as timing and display in the clock, as well as the platform and tools used. The circuit of the digital clock is divided into three modules, namely the frequency division module, counting module, and decoding display module. And the timing process is through the LED display, and the digital tube displays "hours", "minutes", and "seconds" which are displayed in two digits. The frequency division module divides a 50 MHz input signal to obtain a 1 Hz clock signal, and the counting time module can count and adjust the time of the clock, minutes, and seconds, and then display it on the FPGA development board through the decoding display module. After clock simulation, the system realizes the function of the digital clock and meets the design requirements.

CHAPTER: 3

BASICS COMPONENTS OF DIGITAL CLOCK

- **Timekeeping Logic**: This component keeps track of seconds, minutes, and hours.
- **Display Unit**: This component displays the current time on a suitable display like a 7-segment display or an LCD.
- **Counters**: Three counters are used to track seconds, minutes, and hours.
- **Clock and Reset**: The clk input provides the clock signal, and the reset input resets the counters to zero.
- **Counter Logic**: Each counter increments on the rising edge of the clock, provided the previous counter has reached its maximum value.
- **Rollover**: When a counter reaches its maximum value, it rolls over to zero.

BLOCK DIAGRAM:



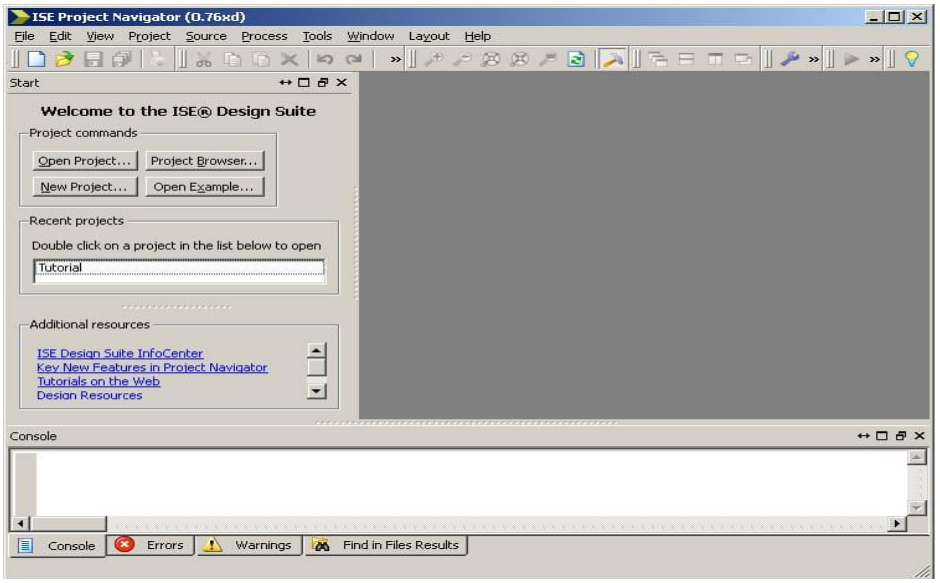
CHAPTER: 4

SOFTWARE REQUREMENT

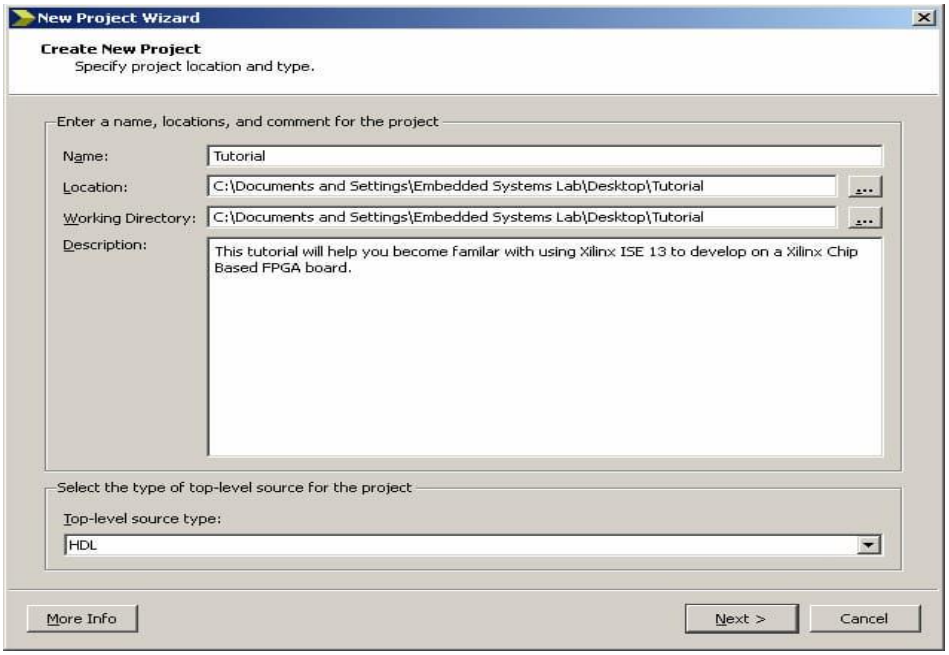
Xilinx ISE (Integrated Synthesis Environment) was a powerful software suite used for designing and implementing digital circuits on Xilinx Field Programmable Gate Arrays (FPGAs). It was a popular choice for many years, especially for educational and smaller-scale projects.

Step 1: Launch Xilinx ISE 14.7
1. Open Xilinx ISE 14.7 on your computer.
2. The Xilinx ISE 14.7 welcome screen appears.

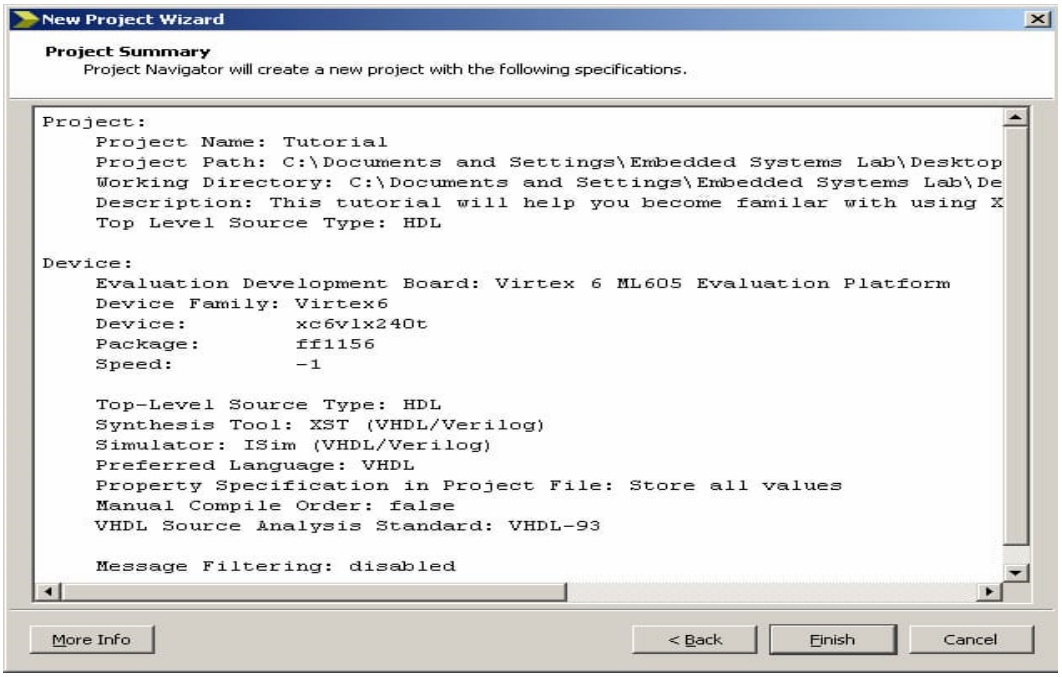
- Select a new project



- Create a New Project

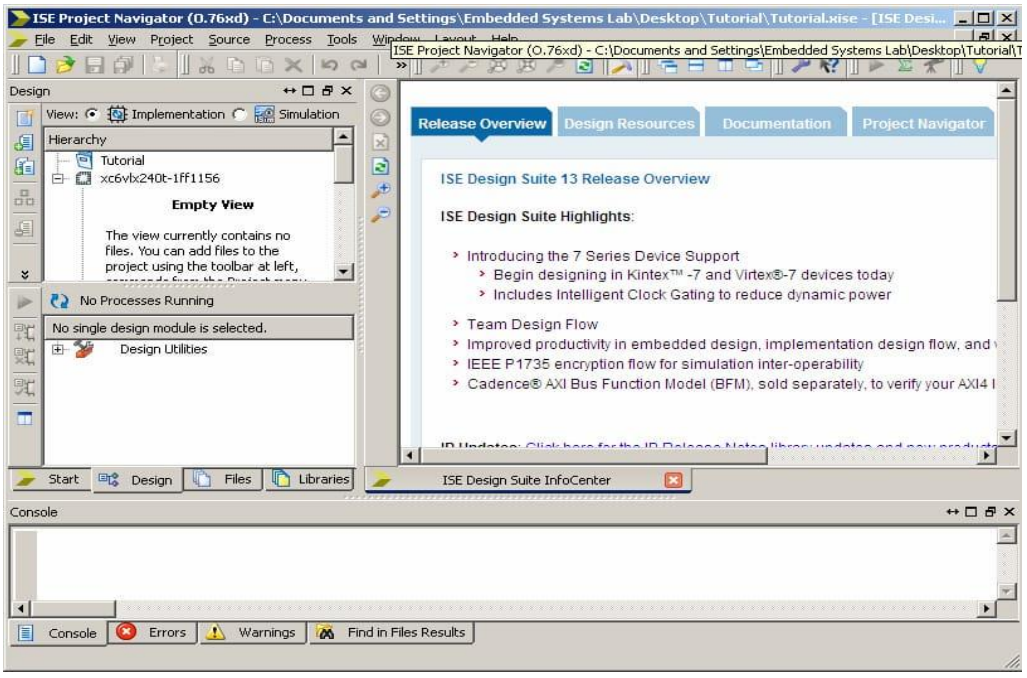


- Project setting

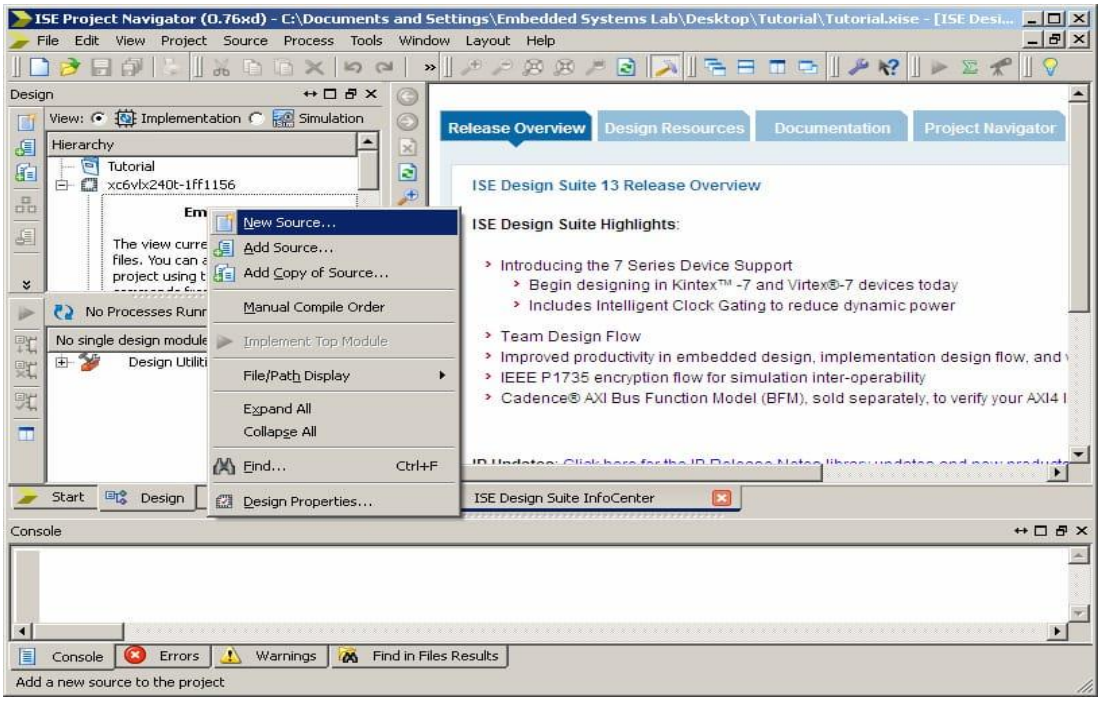


Step 2: Entity Setup

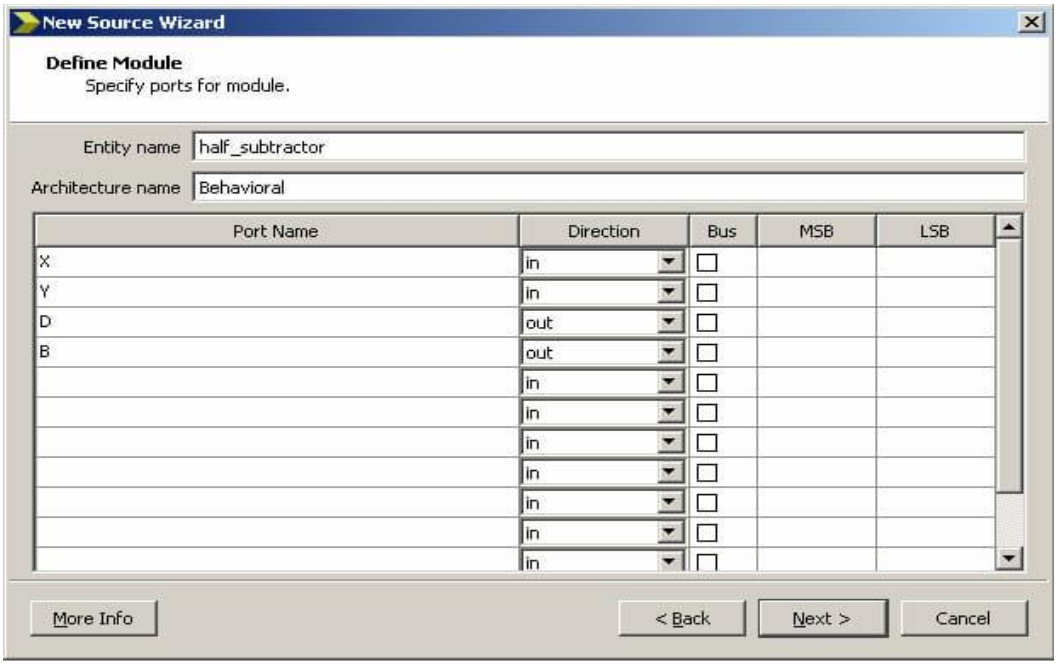
You are now viewing the Project Navigator. The Sources in the Project section will automatically organize your VHDL module tree (Top Left). The Processes for Source pane will allow you to perform various processes such as synthesis or device programming, view reports, and access useful tools (Middle Left). The bottom pane contains console output - notice the Console, Errors, Warnings tabs; these are useful in debugging (bottom section). The right are is used to display any files or documents you have opened.



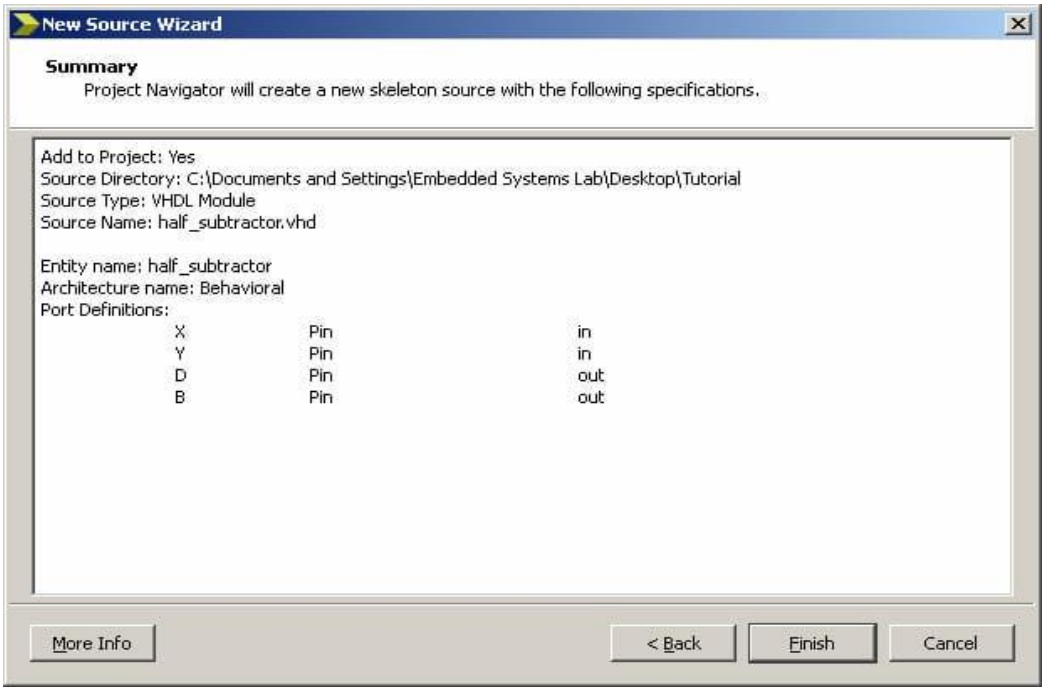
- Now you will create a new Verilog entity. Right-Click on the chip icon and select New Source. Take note that you can add already created sources. Select the Verilog module and give the module name.



- The entity name will near in its text box. In Port Name text box give the port a name button_north, since this is a single input it has no bus; do this for buttton_south, buton_west, and button_west.

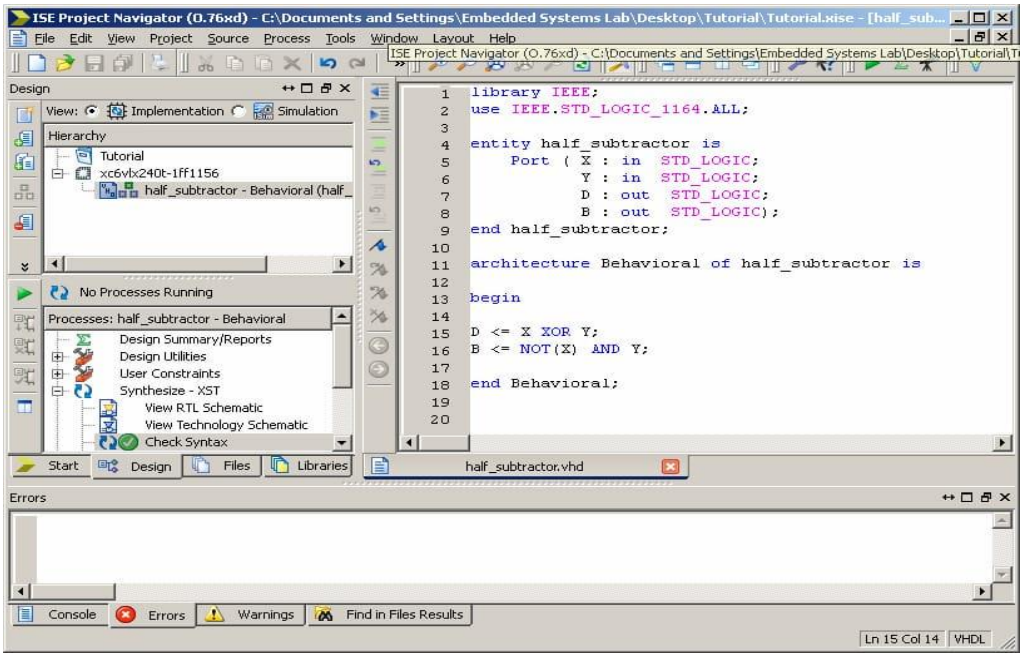


- Review the summary of the entity then Select Finish.

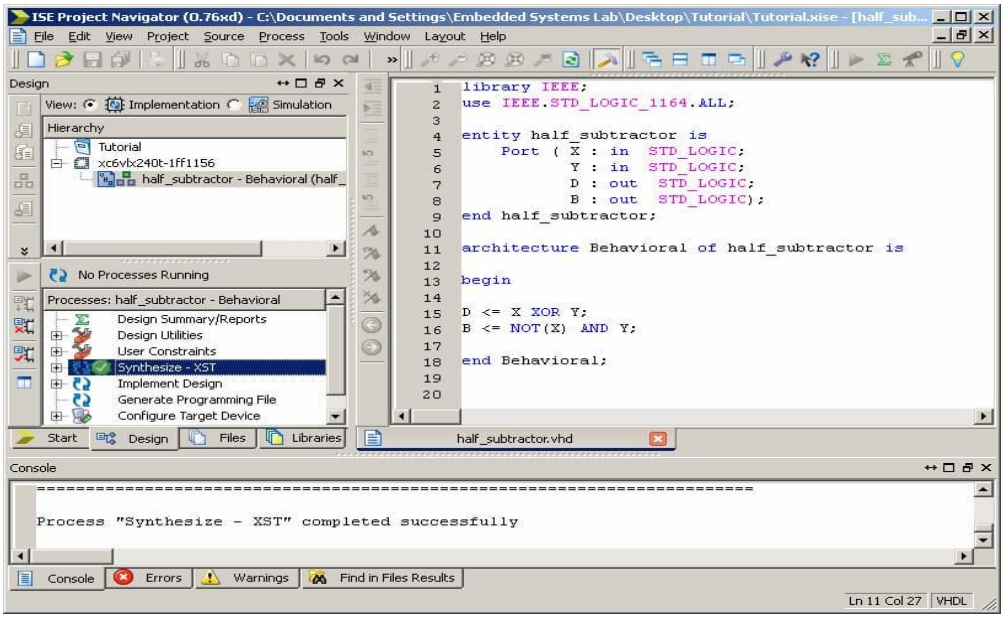


Step 3: Synthesis

- Enter the code. Once Entered, now we need to check if the VHDL syntax is correct. Expand the Synthesize - XST tree and double click Check Syntax.



- If correct, then close tree and select Synthesize - XST to check to make sure the code is synthesizable; there should not be warnings or errors.



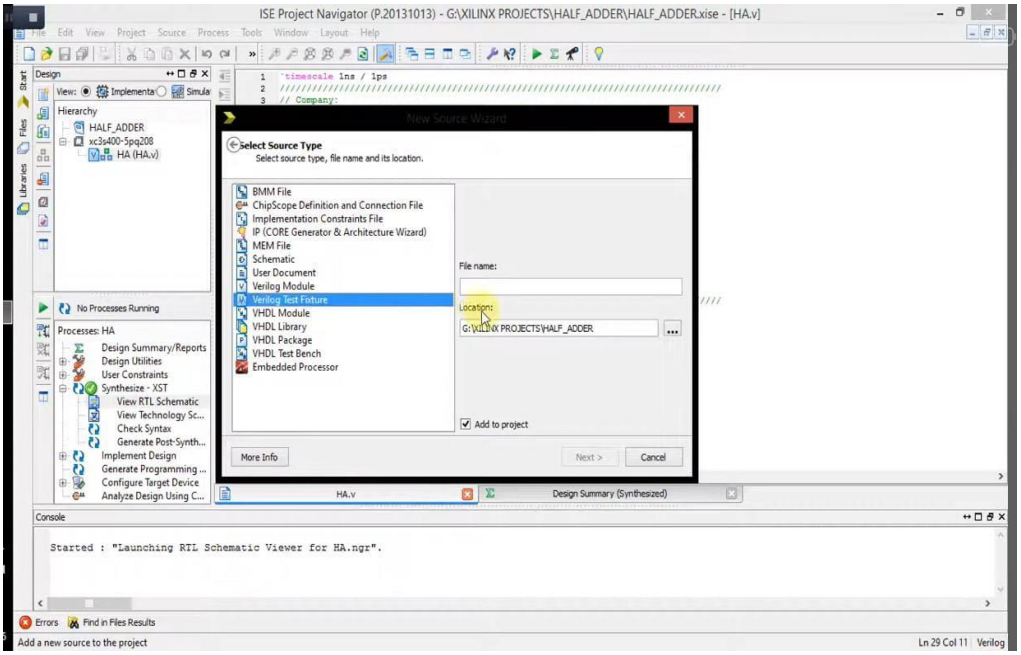
Step 4: Testbench

- Add a new source.

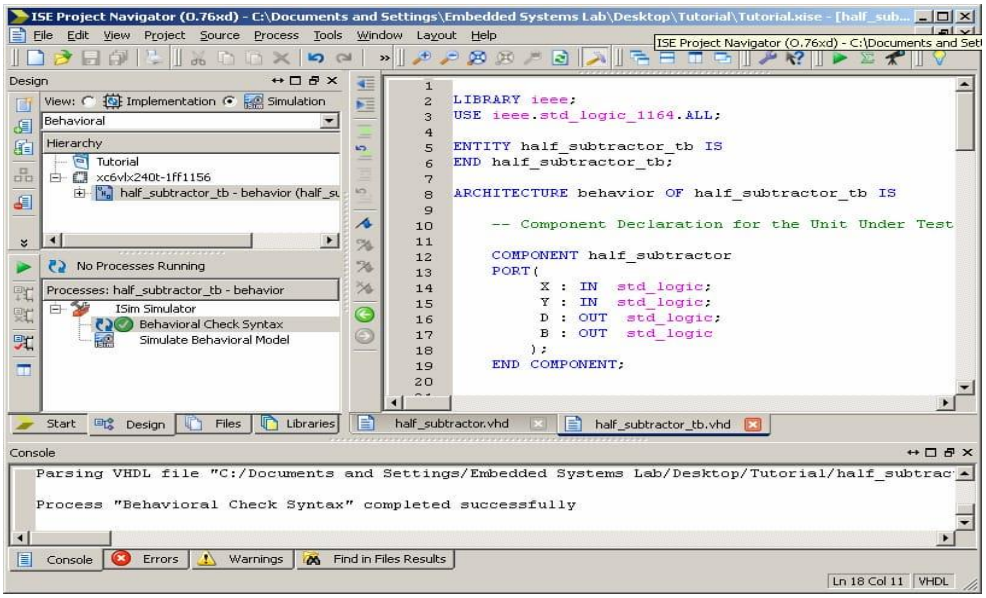
  Select Verilog Text Fixture

  File name: pass_thru_tb

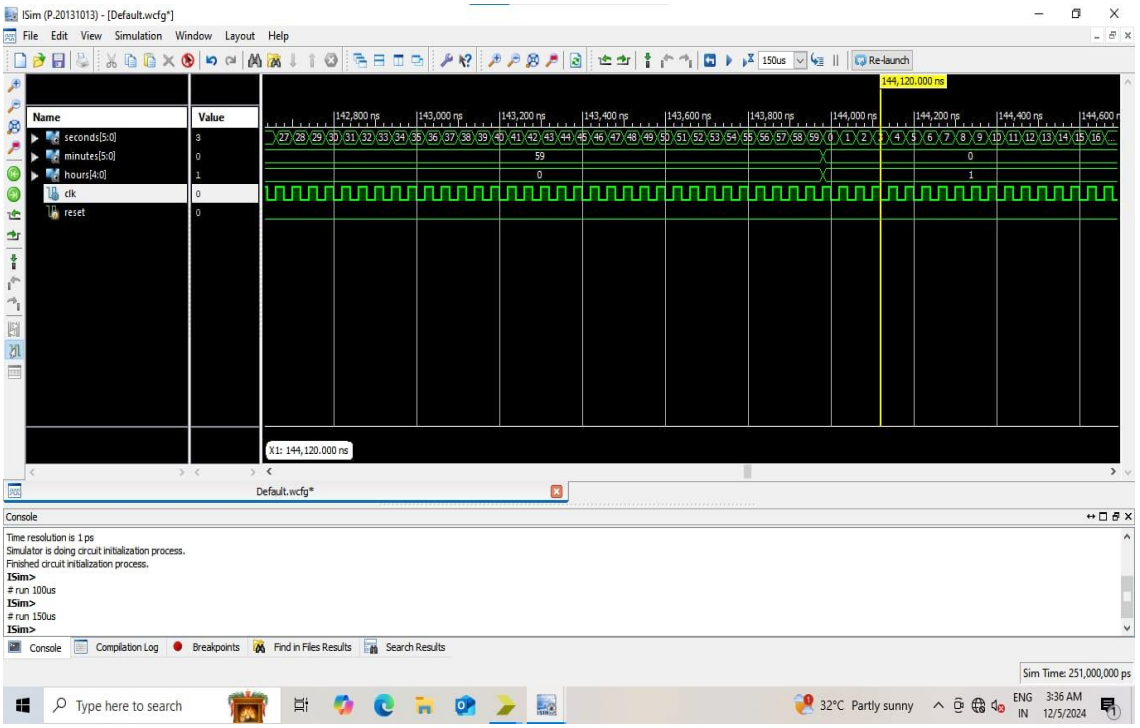
  Select Next >



- Enter the code.
  In the Processes for Source pane expand the ISim Simulator and double click the Behavioral Check Syntax. If correct then there will be no errors.



- In the Processes for Source pane double click the Simulate Behavior Model. A new window will appear showing the simulation. If the test bench completes with no errors in the command prompt then simulation was successful for the tested cases. You might have to zoom out to view the signals in ns. Zoom out by pressing F7 and zoom in by pressing F8 or use the shortcuts on the top bar. Note: the testbench does not necessarily run to the final wait statement. You might need to run the test until you get the message "Note: Done with testbench".



CHAPTER 5:
METHODOLOGY

Below is the detailed explaination of each line given in the Verilog code:

Module Declaration

verilog Copy code

```
module digital_clock(
   input clk,
   input reset,
   output [5:0] seconds,
   output [5:0] minutes,
   output [4:0] hours
);
```

Fig 1:Module Declaration

module digital_clock: Declares a new Verilog module named digital_clock.

input clk, input reset: Defines two input ports: clk (clock signal) and reset (reset signal).
output [5:0] seconds, output [5:0] minutes, output [4:0] hours:

Defines three output ports: seconds, minutes, and hours, each representing a specific time unit in binary format.

Internal Registers for Time

verilog Copy code

```
   reg [5:0] sec = 0;
   reg [5:0] min = 0;
   reg [4:0] hr = 0;
```

Fig 2: Internal registers for time

reg [5:0] sec = 0: Declares a 6-bit register sec to store the seconds value, initialized to 0.

reg [5:0] min = 0: Declares a 6-bit register min to store the minutes value, initialized to 0.

reg [4:0] hr = 0: Declares a 5-bit register hr to store the hours value, initialized to 0.

RESET LOGIC:

```verilog
if (reset) begin
    sec <= 0;
    min <= 0;
    hr <= 0;
end
```

Fig 3: reset logic

if (reset): This condition checks if the reset signal is active (likely asserted to a logic 1).

begin ... end: This block encloses the operations to be performed when the reset signal is active.

sec <= 0; If the reset is active, the sec (seconds) counter is assigned the value 0. This resets the
seconds count to zero.

min <= 0; Similarly, the min (minutes) counter is also assigned the value 0, resetting the minutes count.

hr <= 0; Finally, the hr (hours) counter is also set to 0, resetting the hours count.

TIME COUNTING LOGIC:

After the reset condition, the code starts incrementing time:

verilog Copy code

```
else begin
    if (sec == 59) begin
        sec <= 0;
        if (min == 59) begin
            min <= 0;
            if (hr == 23) begin
                hr <= 0;
            end else begin
                hr <= hr + 1;
            end
        end else begin
            min <= min + 1;
        end
    end else begin
        sec <= sec + 1;
    end
end
```

Fig 4: sequential logic

This part contains the core logic that updates the clock time. Let's break it down step by step:

1. Seconds Counting:
   On each clock cycle (triggered by the clk signal), the seconds (sec) are incremented by 1.
   If sec reaches 59 (the end of a minute), it is reset to 0, and the minute counter (min) is incremented by 1.

2. Minutes Counting:
   Similarly, when min reaches 59 (the end of an hour), it is reset to 0, and the hour counter (hr) is incremented by 1.

3. Hours Counting:
   When hr reaches 23 (the end of the 24-hour cycle), it is reset to 0, and the clock restarts from 00:00:00.

Output assignments:

```verilog
assign seconds = sec;
assign minutes = min;
assign hours = hr;
```

Fig 5:output assignment

These assign statements are used to provide the current values of sec, min, and hr as outputs. The values are passed to the corresponding output ports (seconds, minutes, hours), which represent the time

assign seconds = sec: Assigns the current value of the sec register to the seconds output port.

assign minutes = min: Assigns the current value of the min register to the minutes output port.

assign hours = hr: Assigns the current value of the hr register to the hours output port.

Here is the detailed explaination of the test bench code:

1. Module Declaration

verilog Copy code

```
module counter_test;
```

Declares the counter_test module, which is the name of the test bench. A test bench does not have inputs or outputs because it is meant for simulation only.

2. Register and Wire Declarations

verilog Copy code

```
reg clk;
reg reset;
```

clk (Clock Signal):
Declared as reg because its value is set procedurally in the test bench.
Used to drive the clk input of the digital_clock.

reset (Reset Signal):
Declared as reg because it is assigned values procedurally.
Used to reset the digital_clock module during initialization.

verilog Copy code

```
wire [5:0] seconds;
wire [5:0] minutes;
wire [4:0] hours;
```

seconds, minutes, and hours:

Declared as wire to hold the output values from the digital_clock module.

Wires are used for connections between the test bench and the module being tested.

Seconds and minutes are 6 bits wide, while hours is 5 bits wide, matching the expected output sizes.

3. Instantiation of the Digital Clock Module

verilog Copy code

```
digital_clock uut (
    .clk(clk),
    .reset(reset),
    .seconds(seconds),
    .minutes(minutes),
    .hours(hours)
);
```

The digital_clock module is instantiated with the instance name uut (Unit Under Test).

The ports of the digital_clock are connected to the test bench signals:
clk connects to the test bench clock signal.
reset connects to the test bench reset signal.

seconds, minutes, and hours are outputs from digital_clock that connect to the test bench wires.

4. Initial Block

verilog Copy code

```
initial begin
    clk = 0;
    reset = 1;
    #10 reset = 0;
end
```

The initial block executes once at the start of the simulation.

clk = 0; Initializes the clock signal to logic 0.

reset = 1; Sets the reset signal to logic 1 to initialize the digital_clock module.

#10 reset = 0; After 10 time units, the reset signal is deasserted (set to 0), allowing the digital_clock to begin normal operation.

5. Always Block

verilog Copy code

```
always
    #20 clk = ~clk;
```

The always block is used to generate a periodic clock signal.

Every 20 time units (#20), the clock signal is inverted using ~clk.

This creates a clock signal with a period of 40 time units (20 units high and 20 units low), corresponding to a frequency for the simulation.

6. End of the Test Bench

verilog Copy code

```
endmodule
```

Marks the end of the counter_test module definition.

➢ RTL Schematic:

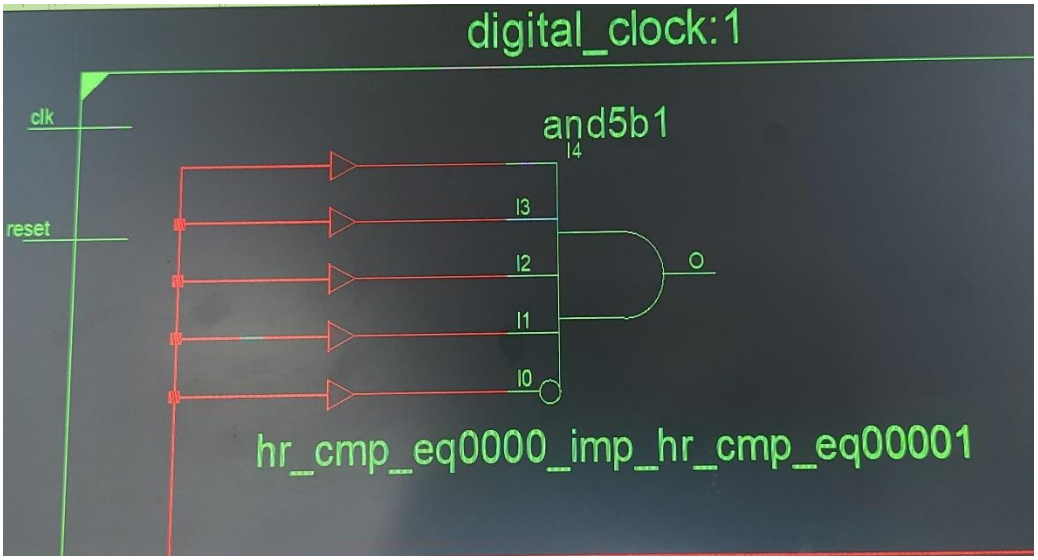


Fig: hour schematic for RTL

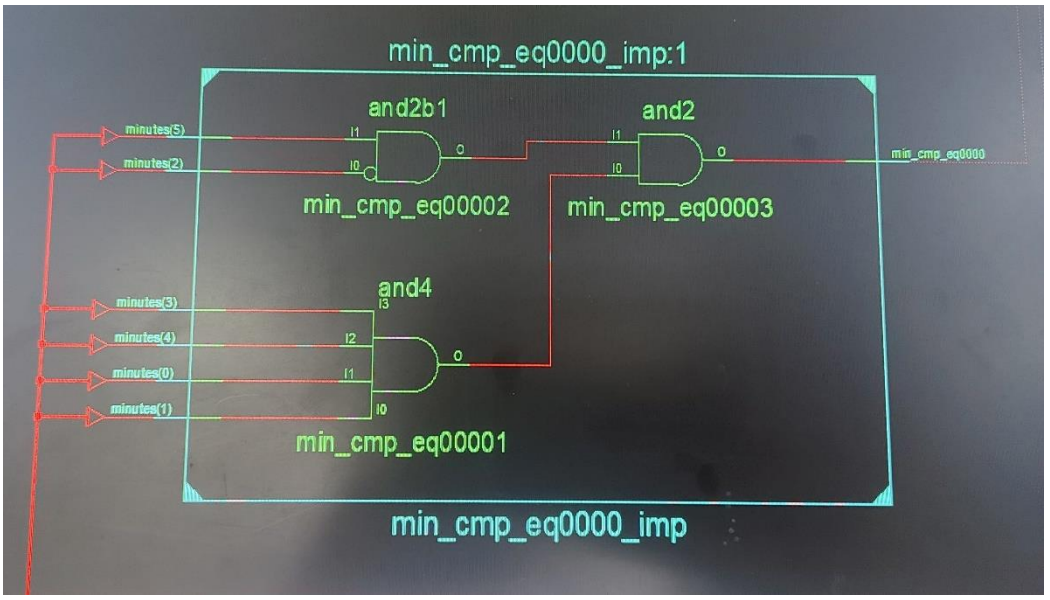


Fig: minute schematic for RTL

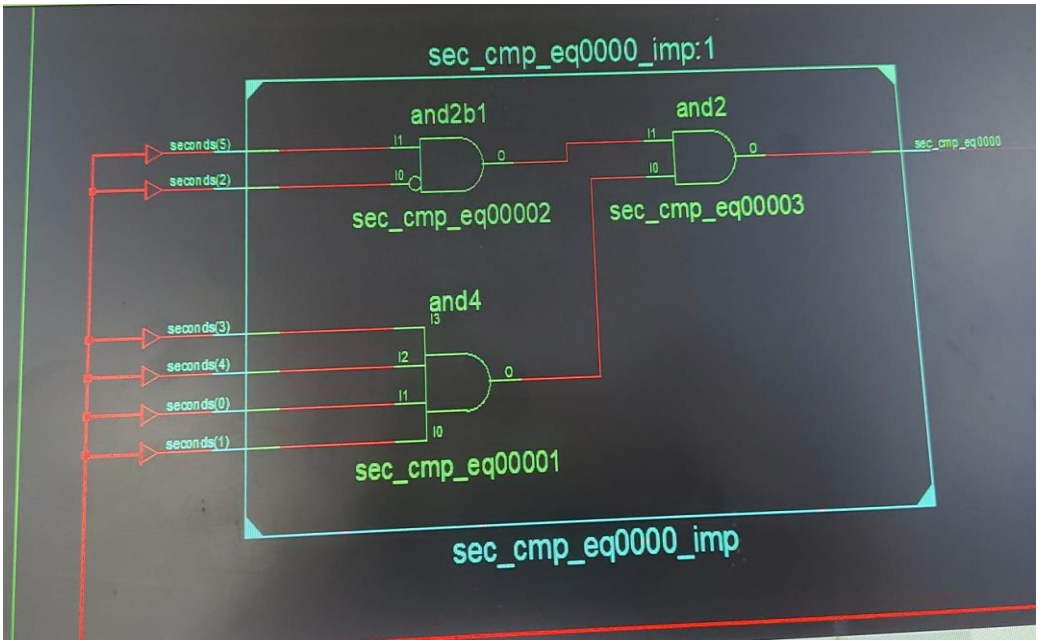


Fig: second schematic for RTL

➢ Technological Schematic:

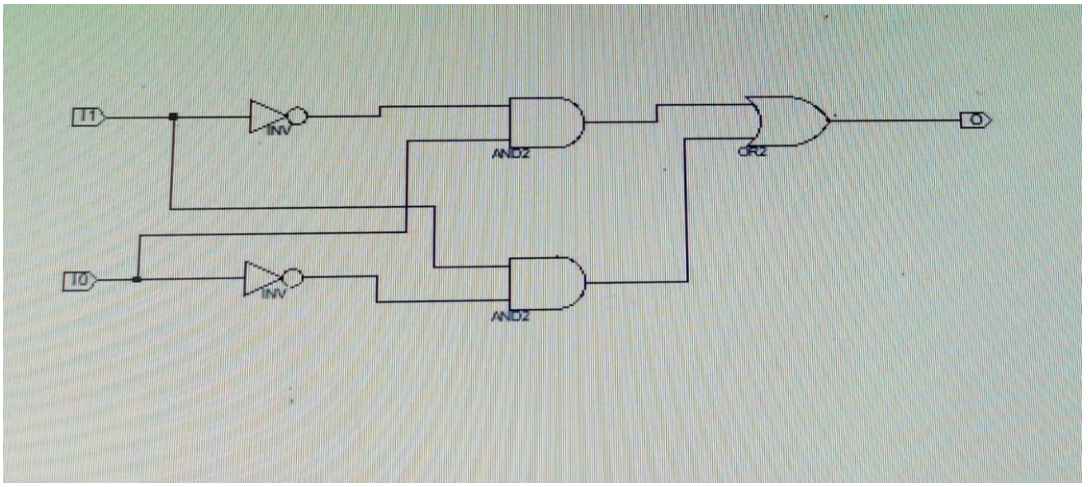


Fig: hour technological schematic

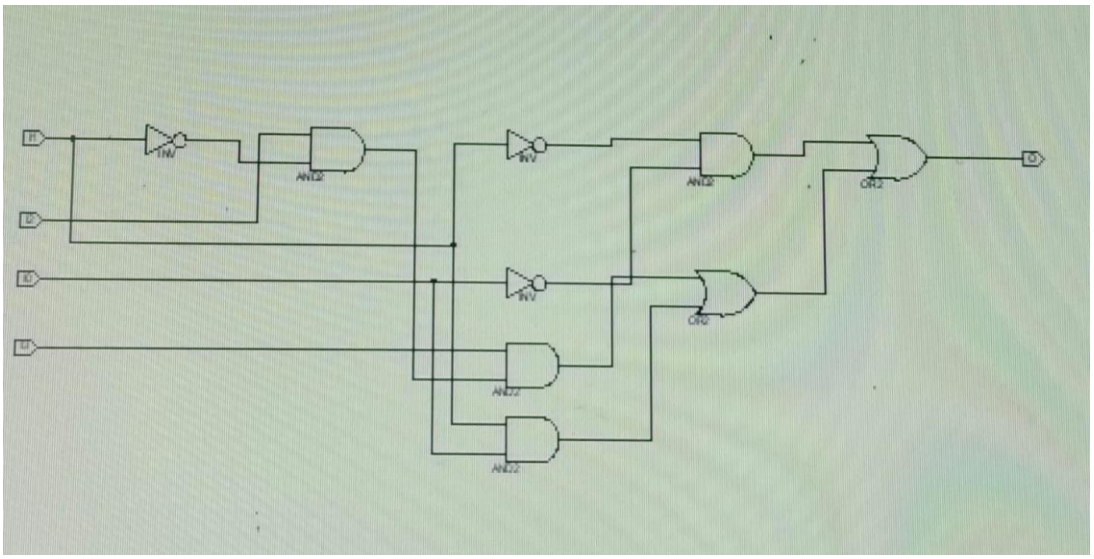


Fig: minute technological schematic

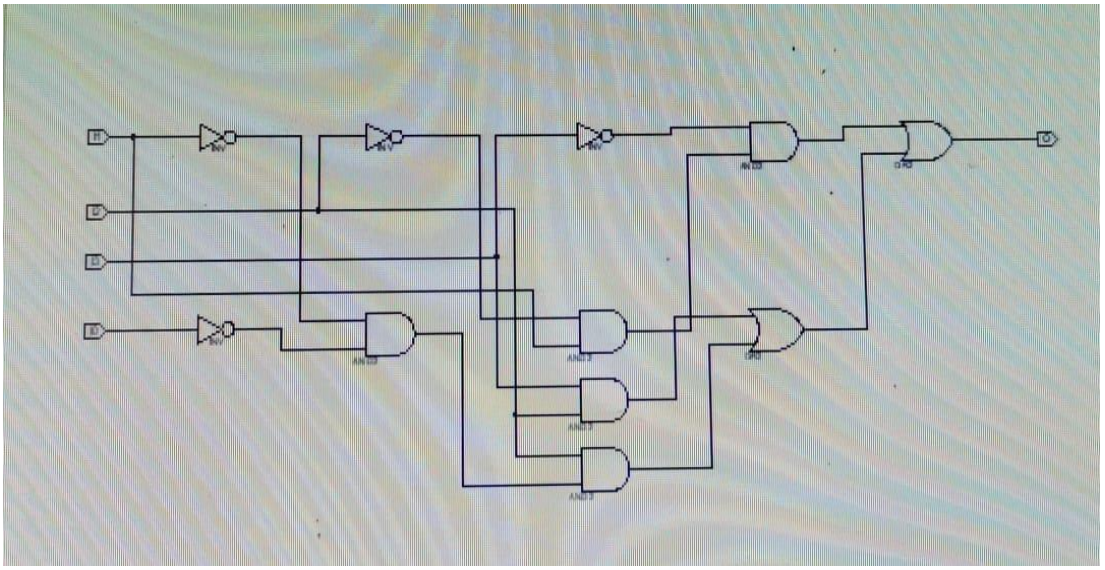


Fig: second technological schematic

➢ K-MAP REPRESENTATION FOR HOUR, MINUTE, SECOND:

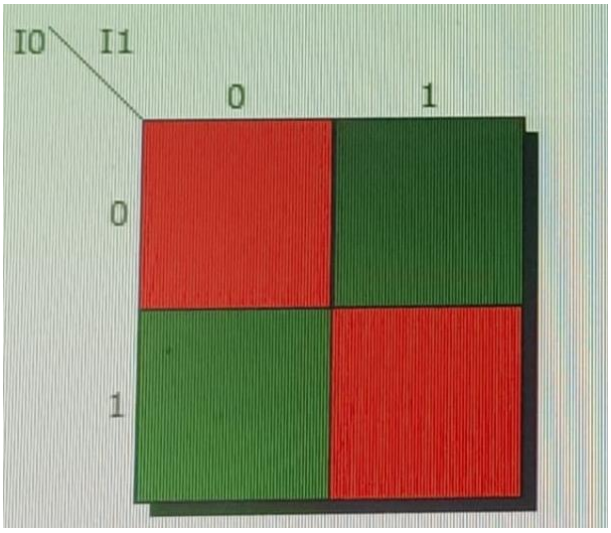


Fig: k-map for hour

Equation:

O=((!I0*I1)+(I0*!I1))

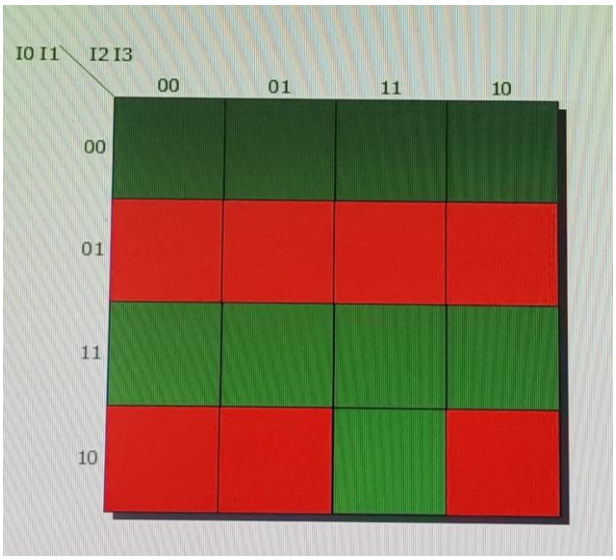


Fig: k-map for minute

Equation:

O=((!I0*!I1)+(I0*I1)+(I0*I2*I3))

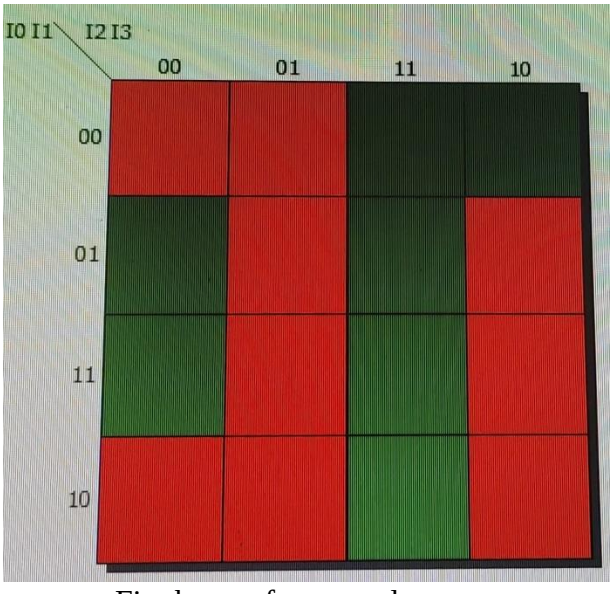


Fig: k-map for second

Equation:

O=((!I0*!I1*I2)+(I2*I3)+(I1*!I2*!I3))

➢ COMPARISION BETWEEN RTL AND TECHNOLOGY SCHEMATIC:

FEATURE	RTL SCHEMATIC	TECHNOLOGY SCHEMATIC
Abstraction level	High level	Low level
Component representation	Generic symbols	Device specific symbols
Focus	Functional behaviour	Physical implementation
Purpose	Design verification and debugging	Timing analysis and resource optimization

RTL Schematics provide a conceptual view of the design, aiding in understanding the overall functionality and logical flow.

- It verifies the intended behavior of the design before synthesis.
- It identifies potential design errors or inefficiencies early in the design flow.
- It helps to understand the design's architecture and modularity.

Technology Schematics offer a detailed view of the physical implementation, enabling optimization and timing analysis.

- It Analyzes the resource utilization and timing performance of the synthesized design.
- Identifies potential timing critical paths and resource bottlenecks.
- Understands how the design is mapped to the target device architecture.

By effectively utilizing both schematic views, designers can efficiently debug, optimize, and verify their Xilinx FPGA designs.

CHAPTER: 6

ADVANTAGES

- **Precision and Accuracy**:
  Counters ensure precise timing by incrementing at regular intervals, eliminating the potential for human error or mechanical inaccuracies.

- **Flexibility and Customization**:
  Digital clocks can be easily programmed to display time in various formats (12-hour, 24-hour, military time).
  They can incorporate additional features like alarms, timers, and date displays.

- **Energy Efficiency:**
  Digital clocks typically consume less power than analog clocks, especially those with LCD displays.

- **Durability and Reliability:**
  Digital clocks are generally more durable and reliable than analog clocks.

- **Clear Readability:**
  Digital displays are easy to read, even in low-light conditions.

- **Cost-Effective:**
  Digital clocks, especially those using integrated circuits, are often more affordable to produce and maintain than analog clocks.

- **Versatility:**
  Digital clocks can be integrated into various devices, such as computers, smartphones, and other electronic gadgets.

Overall, digital clocks using counters offer a reliable, accurate, and versatile solution for timekeeping needs, making them a popular choice in modern industries.

APPLICATIONS

Digital clocks, implemented using Verilog and counter circuits, find widespread applications in various domains. Here are some of the applications:

➢ Consumer Electronics:

- Clocks Wall: These are common household items that display time accurately.
- Wristwatches: Digital watches use similar principles to display time on a small screen.
- Alarm Clocks: These devices can be programmed to wake users at specific times.

Timers: Used for setting specific durations for cooking, workouts, or other tasks.

➢ Industrial Applications:

- Real-Time Systems: Industrial control systems often require precise timing for synchronization and control of processes.
- Data Acquisition Systems: These systems need accurate timestamps for data logging and analysis.
- Embedded Systems: Microcontrollers often incorporate digital clocks for timing-critical operations.

➢ Educational and Research:

- Laboratory Equipment: Oscilloscopes, function generators, and other lab instruments use digital clocks for timing measurements.
- Research Projects: Researchers may use digital clocks for precise timing experiments in fields like physics and biology.

➢ Specialized Applications:

- Medical devices: Timing drug administration, monitoring vital signs, and controlling medical equipment.
- Scientific research: Precise timing for experiments and data acquisition.
- Military and aerospace: Timekeeping and synchronization in critical systems.
- Telecommunications: Network timing and synchronization.
- GPS systems: Accurate timekeeping for precise positioning.

CHAPTER: 7

RESULT

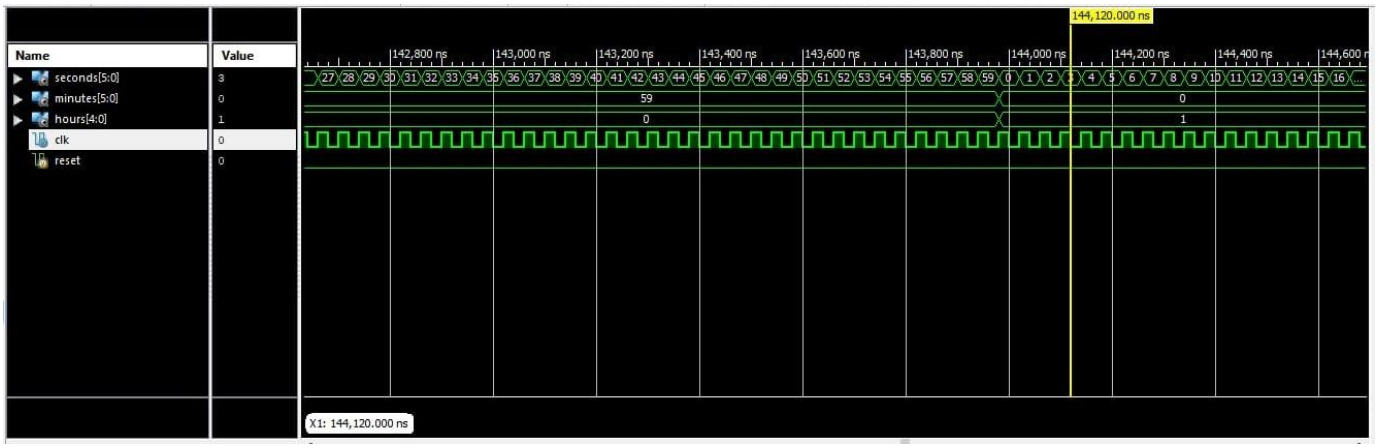


Fig: simulation output

- **Simulation Output:**

The simulation shows the values of the counters changing over time.

The seconds counter increments every clock cycle, reaching 59 and then resetting to 0.

The minutes counter increments after the seconds counter reaches 59, and resets after 59 minutes.

The hours counter increments after the minutes counter reaches 59, and resets after 11 hours (or 23 hours for a 24-hour clock).

- **Observations and Analysis:**

The simulation seems to be working correctly, showing the expected behavior of a digital clock.

The clock signal appears to have a frequency of 1 Hz.

The reset signal is not shown in the simulation, so it's assumed to be inactive during the simulation.

The hours counter is configured for a 12-hour clock, as it only counts up to 11.

- **Possible Enhancements**:

We can add a display unit to visualize the time in a readable format (e.g., 7-segment displays).

You could implement a 24-hour clock by changing the hours counter to a 5-bit counter.

You could add features like AM/PM indication, alarm functionality, or real-time clock synchronization.

CHAPTER: 8

CONCLUSION

This project successfully demonstrates the design and implementation of a digital clock using counter Verilog. The design incorporates a counter module to accurately track time in hours, minutes, and seconds. The output is displayed on seven-segment displays, providing a clear and intuitive visual representation.

The Verilog code effectively utilizes sequential logic to increment the time values at a specified rate, ensuring precise timing. The modular design approach enhances code readability, maintainability, and potential for future modifications.

Through this project, we have gained practical experience in digital design principles and the synthesis and simulation processes. This knowledge can be applied to various digital systems, including timers, counters, and other time-based applications.

CHAPTER: 9

FUTURE SCOPE

The future scope of a digital clock using a counter is broad, as it serves as a foundational concept in digital systems, electronics, and embedded design. Below are potential areas of advancement and applications.

- **High Precision Timekeeping**

Atomic Clock Integration: Developing digital clocks that interface with atomic clocks for ultra-precise timing in research labs, GPS systems, and scientific instruments.

- **IoT Devices**

They can be integrated into IoT devices to provide timekeeping and synchronization capabilities, enabling features like data logging, scheduling, and remote control.

- **Medical and Biometric Applications**

Healthcare Monitoring: Embedding digital clocks with counters in medical devices for precise monitoring of patients' vitals and therapy schedules.

Biometric Sensors: Synchronizing biometric data collection with digital counters for accurate health assessments.

- **Smart Automation Systems**

Robotics: Employing counters in robotic systems for time-sensitive tasks and process control.

- **Integration with Advanced Technologies**

AI-Powered Scheduling: Combining the digital clock with artificial intelligence to predict user schedules and optimize time management.

Blockchain Time Stamping: Using counters in digital clocks for secure and precise time-stamping in blockchain and digital ledger technologies.

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