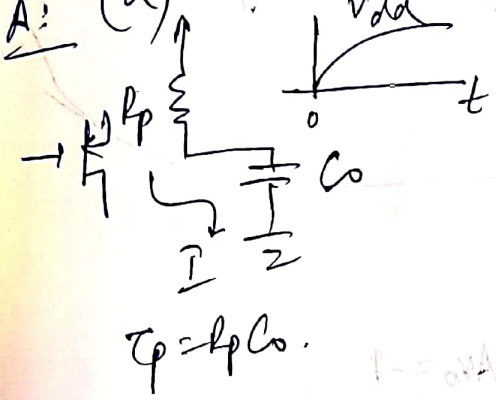
Tut - 28/8/25 (Tut - 3)

(1) Derive exp. for (a) rise time, (b) fall time, (c) propagation delay using transient analysis of basic RC networks, where the nFETs & pFETs are approx. as linear resistors with resistances $R_n = \frac{1}{\beta_n V_{ov}}$ & $R_p = \frac{1}{\beta_p V_{ov}}$. ~~As this~~

Derive exp. using both diff. eqns and L T formulations.

A: (a)



$\tau_p = R_p C_o$.

$$\frac{V_{dd} - V_o}{R_p} = + C_o \frac{dV_o}{dt}$$

$$1 - \frac{V_o}{V_{dd}} = e^{-t/\tau_p}$$

$$V_o(t) = V_{dd}(1 - e^{-t/\tau_p})$$

$$p'(x) + q(x) e^{\int} = r(x)$$

$$\frac{V_{dd}}{s} - V_o(s) = + R_p C_o \left[s V_o(s) - \underbrace{V_o(t=0)}_{V_0} \right]$$

$$\frac{V_{dd}}{s} = V_o(s)\left[1 + s R_p C_o\right]$$

$$\int_0^{V_{dd}} \frac{dV_o}{V_o - V_{dd}} = \frac{-1}{R_p C_o} \int_0^t dt \quad \ln\left(\frac{V_o - V_{dd}}{-V_{dd}}\right) = +\frac{t}{R_p C_o}$$

$$\frac{V_{dd}}{s} = V_o(s)\left[1 + s R_p C_o\right]$$

$$V_o(s) = V_{dd}\left(\frac{1}{s} - \frac{1}{s + \frac{1}{R_p C_o}}\right)$$

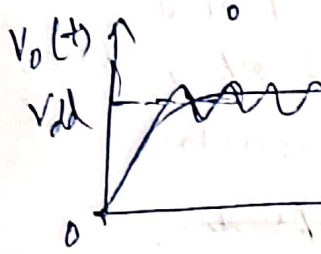
Operational calc.

$$V_o(s) = \frac{V_{dd}}{s\left(s + \frac{1}{R_p C_o}\right)} \cdot \frac{1}{R_p C_o}$$

$$V_o(t) = V_{dd}\left(1 - e^{-t/\tau_p}\right)$$

$$F(j\omega) = \int_0^\infty f(t)\, e^{-j\omega t}\, dt \qquad L(s) = \int_0^\infty f(t)\, e^{-st}\, dt$$

($s = \sigma + j\omega$)



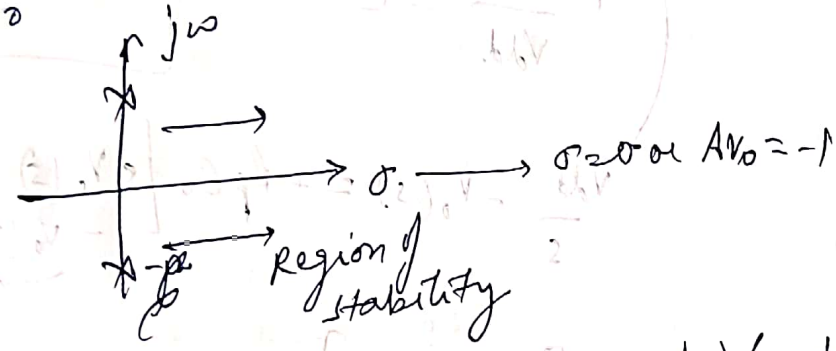
$A_{V0} = \frac{V_0}{V_i} = -1$ (goes on forever if $A_{V0} = -1$)

To decrease amplitude, multiply it with $e^{-\sigma t}$. it dies down.

We use σ & not $j\omega$ cause $+j\omega$ means lead & $-j\omega$ means lag

(σ damping factor)

$$L(s) = \int_0^\infty f(t)\, e^{-(\sigma + j\omega)t}\, dt$$



$$f_{max} = \frac{1}{t_r + t_f}$$

If ϕ is very high, t_r & t_f are very high & f_{max} becomes very low.

(b) $V_0(t) = V_{dd}\, e^{-t/R_n C_0}$ (pull down n/w)

$V_0(t) = V_{dd} \to 0$

$$\frac{V_0}{R_n} = -C_n \frac{dV_0}{dt}$$

$$\Rightarrow V_0(s) = -R_n C_0 \left[s V_0(s) - \underbrace{V_0(t=0)}_{V_{dd}} \right]$$

$$= -R_n C_0 \left[s V_0(s) - V_{dd} \right]$$

$$\Rightarrow V_0(s)\left[1 + sR_nC_0\right] = R_n C_0 V_{dd}$$

$$\Rightarrow V_0(s) = \frac{V_{dd}}{s + \frac{1}{R_n C_0}} \Rightarrow \boxed{V_0(t) = V_{dd}\, e^{-t/R_n C_0}}$$

~~Put 0.9 Vdd~~ for fall time)

$$0.9 V_{dd} = V_{dd}\, e^{-t_1/R_n C_0}$$

$$0.1 V_{dd} = V_{dd}\, e^{-t_2/R_n C_0}.$$

$$9 = e^{(t_2 - t_1)/R_n C_0}$$

$$t_p = t_2 - t_1 = \tau_n \ln 9$$

For propagation delay take 0.5 & 0.1.

$$0.5 V_{dd} = V_{dd}\, e^{-t_1/R_n C_0}$$

$$0.1 V_{dd} = V_{dd}\, e^{-t_2/R_n C_0}$$

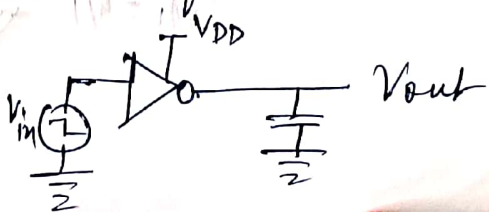
$$5 = e^{(t_2 - t_1)/R_n C_0}$$

$$t_p = t_2 - t_1 = \tau_n \ln 5$$

Q2. The transistors in the static CMOS inverter can be modeled as constant linear resistors (when turned on) $V_{DD} = 2.5V$, $C_L = 25pF$. As usual, assume input signal has a very steep slope and is stable before the ckt starts to switch.

(a) For a 1→0 transition at the i/p, determine the transistor resistances that will result in a 10% → 90% of V_{DD} transition of the o/p within 5ns.

(b) Draw rough sketch of current drawn from the power supply as a function of time during this low-to-high transition & derive the appropriate eqns. that describe the behavior.



A: $V_{DD} = 2.5V$, $C_L = 25pf$.

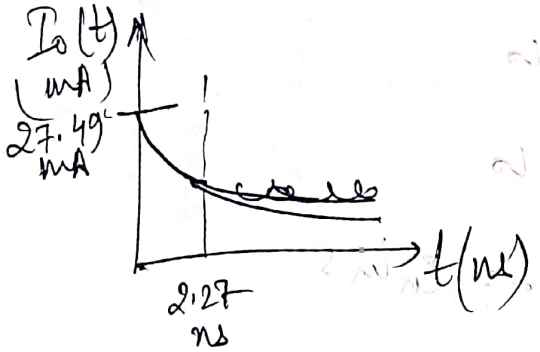
(a) $t_{r} = t_p (\ln 9)$ $\quad 5n = R_p \times 25p \times 2.2$

$\Rightarrow R_p = \underline{90.91\,\Omega}$

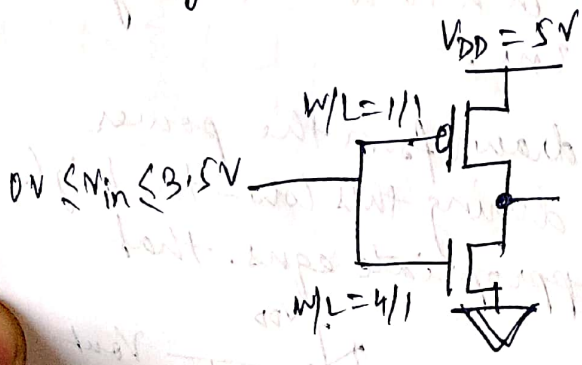
(b) $V_o(t) = V_{dd}(1 - e^{-t/\tau_p})$

$$I_o(t) = \frac{V_{dd} - V_o}{R_p} = \frac{V_{dd}}{R_p} e^{-t/\tau_p} = \frac{2.5}{90.91} e^{-t/(5n/2.2)}$$

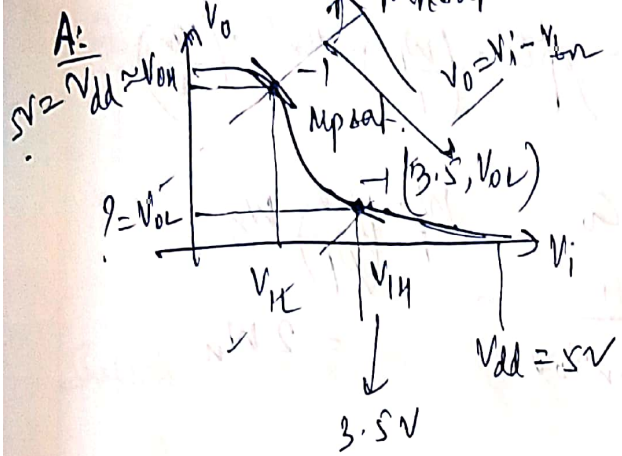
$$= 27.49\, e^{-t(2.27n)}\ mA$$



(Q3) In the adjoining static CMOS inverter, assume $V_{OH} \approx V_{DD} = 5V$, $\mu_n C_{ox} = 500\,\mu A/V^2$, $\mu_p C_{ox} = 200\,\mu A/V^2$, $V_{TN} = -V_{TP} = 1V$. If V_{in} is varied within the range $0 \le V_{IN} \le 3.5V$. Compute the value of V_{OL}.



A:



@ (V_{IH}, V_{OL}), Mn lin., Mp sat.

$$\beta_n \left(V_{ov_n} - \frac{V_{dsn}}{2}\right) V_{dsn} = \frac{\beta_p}{2} V_{ovp}^2$$

$$\beta_n \left(V_{IH} - V_{tn} - \frac{V_{OL}}{2}\right) V_{OL} = \frac{\beta_p}{2}\left(V_{DD} - V_{IH} - |V_{tp}|\right)^2$$

Sub values -

$$500\mu \times 4 \times \left(3.5 - 1 - \frac{V_{OL}}{2}\right) V_{OL} = 200\mu \times 1 \left(5 - 3.5 - 1\right)^2$$

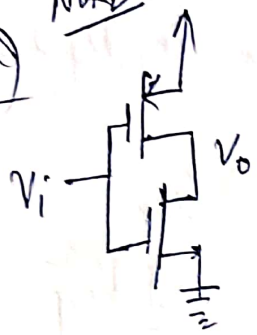
$$\Rightarrow 0 = V_{OL}^2 - 2.5 V_{OL} + 0.0125$$

$$\Rightarrow V_{OL} = \begin{cases} 4.99\,V \\ 5\,mV \end{cases} \longrightarrow \text{supposed to be very close to 0.}$$

(Q4) Design (a) NOR$_2$ gate and (b) NAND$_3$ gate with rise & fall times same as the symmetrical static CMOS inverter at the same tech. node with min delay.

Take $\mu_n = 2\mu_p$.

A1 (a) NOR



$\beta_p = \beta_n \longrightarrow \mu_p C_{ox} \left(\frac{W_p}{L}\right) = \mu_n C_{ox} \left(\frac{W_n}{L}\right)$

$\tau_p = \tau_n$

$R_p C_o = R_n C_o$

$\frac{1}{\beta_p V_{ov}} = \frac{1}{\beta_n V_{ov}}$

$W_p = \left(\frac{\mu_n}{\mu_p}\right) W_n$

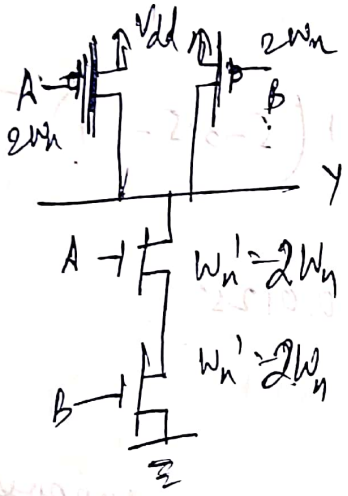
$= 2W_n$

$t_f = 2.2\,\tau_p$

$t_f = 2.2\,\tau_n$

(b)

NAND2 $Y = \overline{A \cdot B}$ = series



$\frac{2}{\beta_n' V_{ov}} = \frac{1}{\beta_n V_{ov}}$

$\Rightarrow \beta_n' = 2\beta_n$

$\Rightarrow \frac{2}{\mu_n C_{ox} W_n'} = \frac{1}{\mu_n C_{ox} W_n}$

$\Rightarrow W_n' = 2W_n$

$\therefore R_p' = R_p$

$\beta_p' = \beta_p \quad \mu_p (W_p') = \mu_p (W_p)$