Analog & Digital VLSI Design

EEE/INSTR F313

Dept. of Electrical & Electronics Engineering (EEE)

Birla Institute of Technology & Science (BITS) Pilani

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Problem 01

Draw a stick diagram layout for a typical (a) NOR_2 & (b) $NAND_2$ gates implemented in static CMOS technology.

Problem 02

Draw the physical layout corresponding to the stick diagrams for the (a) NOR_2 & (b) $NAND_2$ gates implemented in previous problem.

Problem 03

Draw a stick diagram layout for a typical (a) NOR_3 & (b) $NAND_3$ gates implemented in static CMOS technology.

Problem 04

Draw a stick diagram layout for a static CMOS implementation of $Y=\overline{(A+B+C)\cdot D}$.

Problem 05

Draw a stick diagram layout for a typical XOR_2 gate implemented in static CMOS technology.