

Tut-2 (21/8/25)

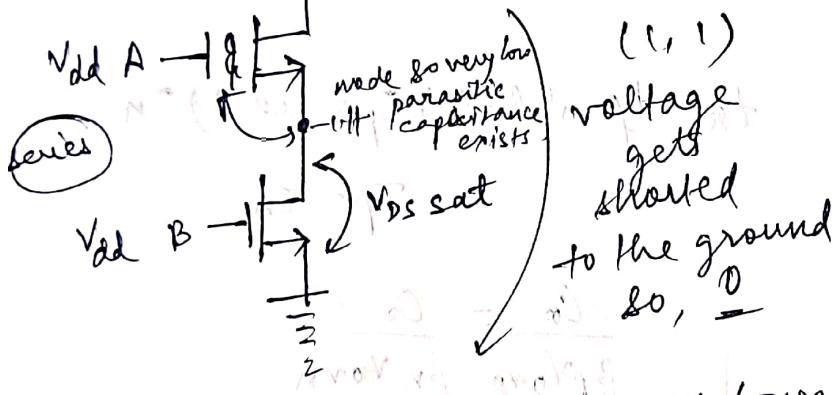
- (Q1) Using NMOS & resistors, implement (a) inverter (b) ~~NAND~~²,
 (c) NOR_2 & the func. (d) $\overline{A + BC}$ & (e) $\overline{AB + CD}$.
 Disadvantages of passive loaded logic circuits?

A: (a) lecture

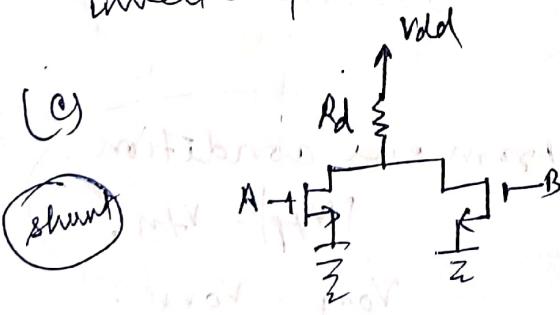


A	B		γ
0	0	1	→ Vdef
0	1	1	→ C Vdef
1	0	1	→ CC Vdef
1	1	0	→ O.

over-taking
a hit

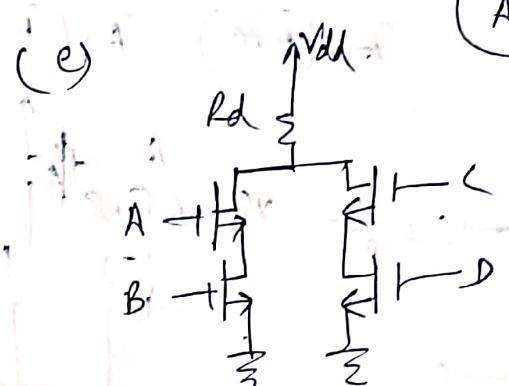
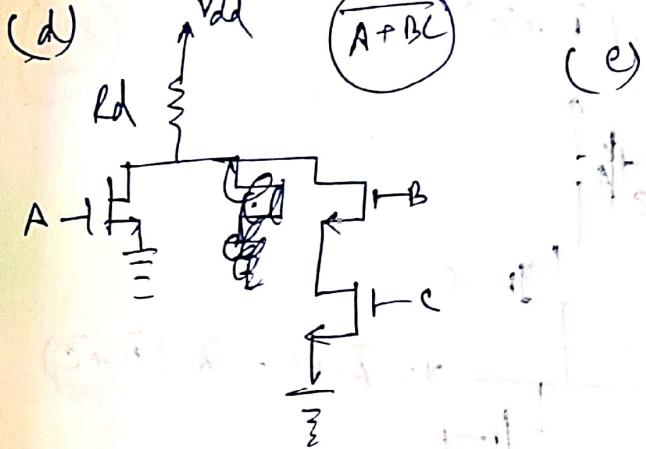


④ anything we do with pull down network will result in inverted form.



A	B	C
0	0	0
0	1	0
1	0	0
1	1	0

Performance taking a hit



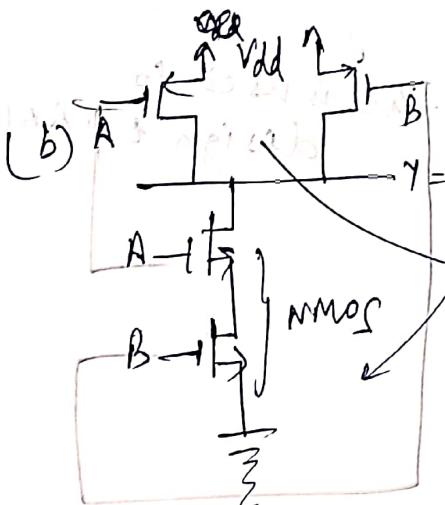
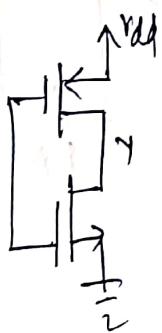
means series
+ means shunt

Disadv: poor performance.

- Q2 In prev. prob, replacing passive load with pmos active load, we get static CMOS logic. Implement (a) inverter, (b) NAND_2 , (c) NOR_2 , (d) $A + BC$, (e) $A \cdot BC$. How does static CMOS resolve the issues with passive loads?

Ans:

(a)



inverted variables.

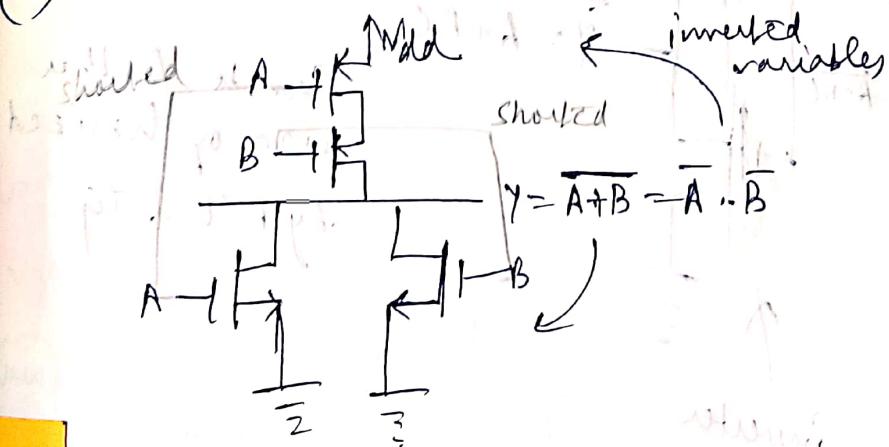
$Y = \overline{AB} = (\overline{A} + \overline{B})$

Both are PMOS.

So, A & B are started with -ve voltages.

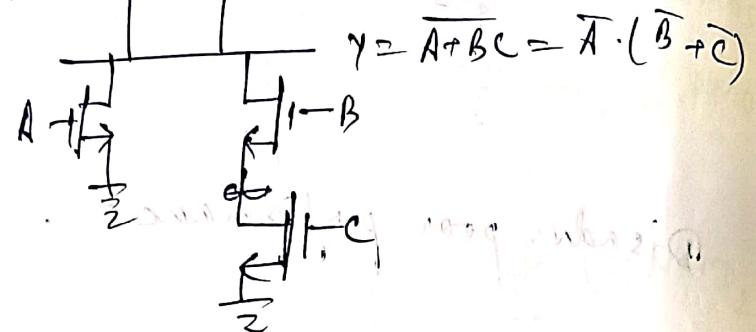
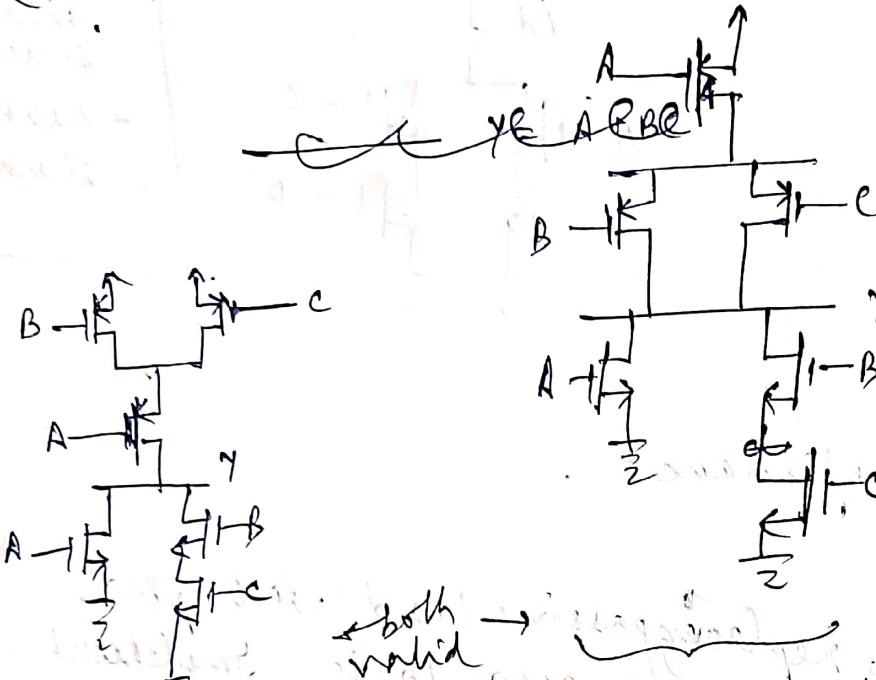
so, $\overline{A} \rightarrow A$ & $\overline{B} \rightarrow B$

(c) $Y = \overline{A + B} = \overline{A} \cdot \overline{B}$



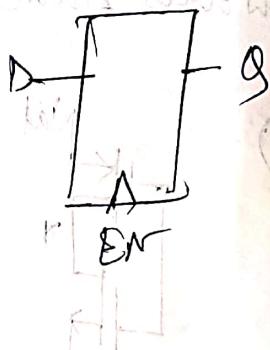
NAND is preferred b/w the universal gates (NAND & NOR) because of better performance due to lower passive capacitance.

$$(d) \overline{A+BC} = \overline{A} \cdot (\overline{B} \cdot \overline{C}) \quad \overline{A} \cdot (\overline{B} + \overline{C})$$

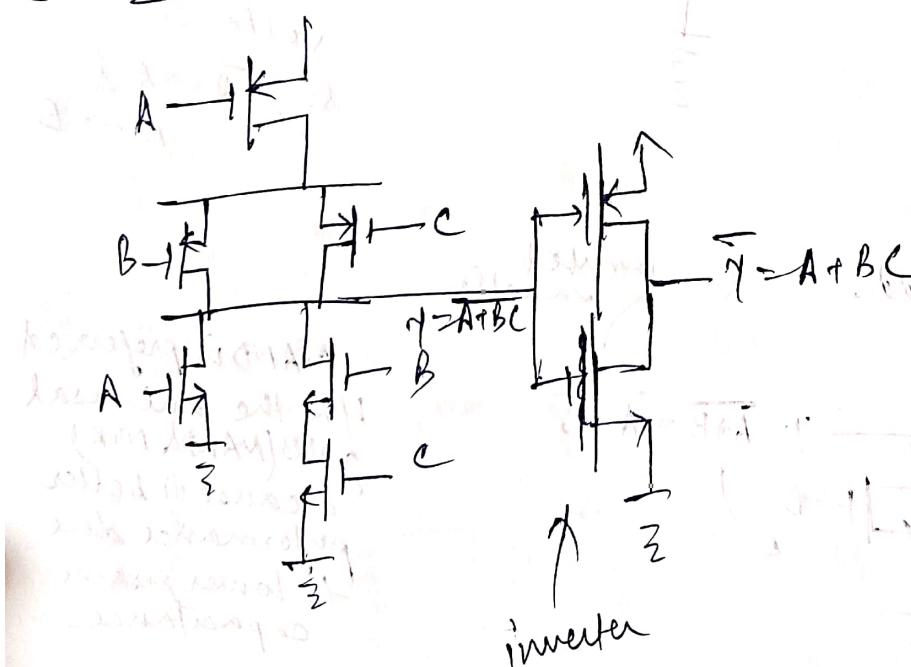


this is better because as long as A is 0 , no power to conduct to other nodes. (so more efficient)

this is used to design ENABLE

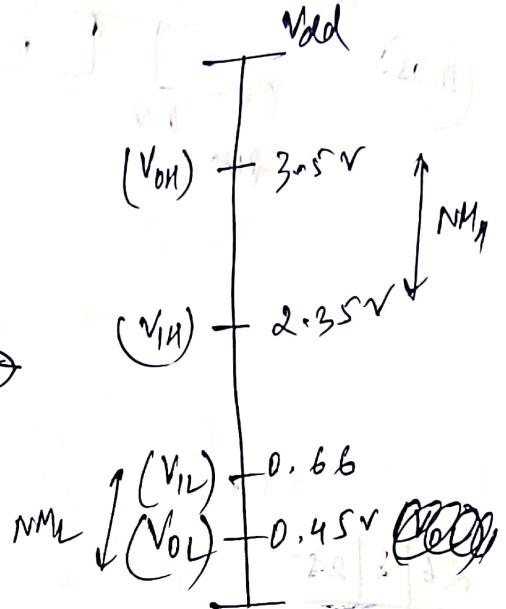
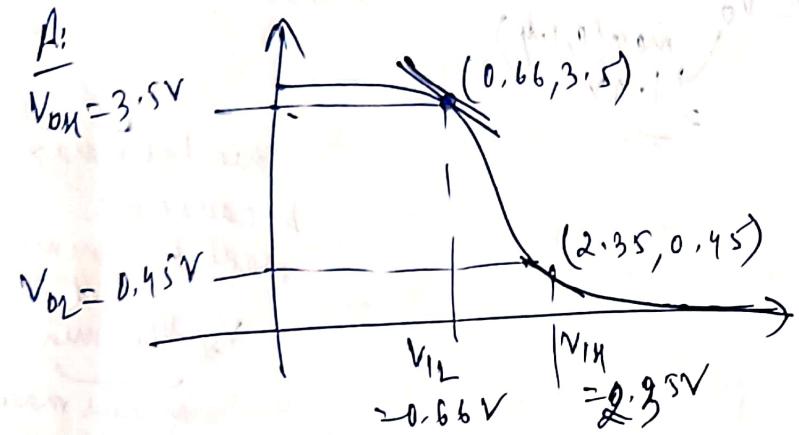


$$(e) \underline{A+BC}$$



Can be further optimised by PTL & TG

(Q3.) Compute NM of static CMOS inverter whose gain $A_{vo} = \frac{dV_o}{dV_i}$ = -1 at (0.66, 3.5)V & (2.35, 0.45)V on its transfer char.



$$NM_H = (3.5 - 2.35)V = 1.15V$$

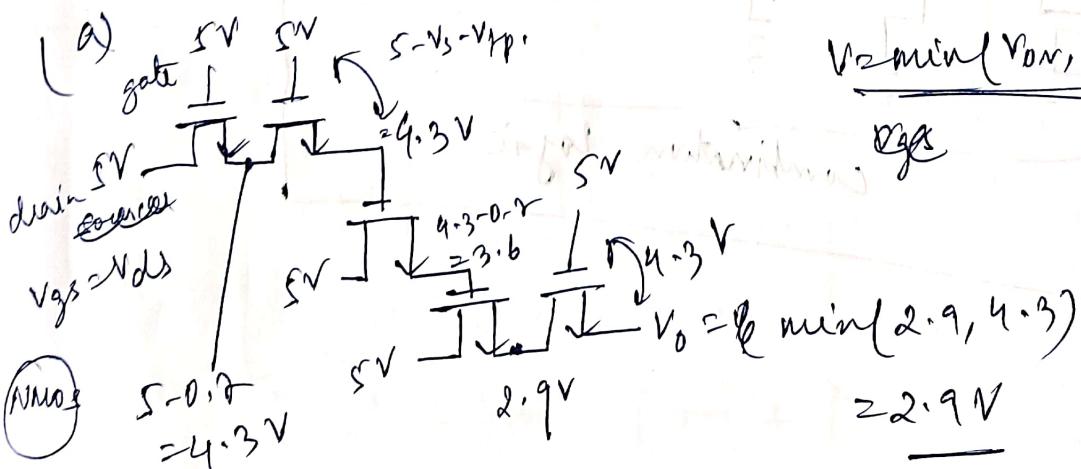
$$NM_L = (0.66 - 0.45)V = 0.21V$$

This is not a robust circuit as NM_L is too low.
Ideally it should be close to $V_{dd}/2$.

$$\text{Overall } NM = \min(NM_L, NM_H) = 0.21V$$

(Q4.) What are the values of V_o in the adjoining circuits?

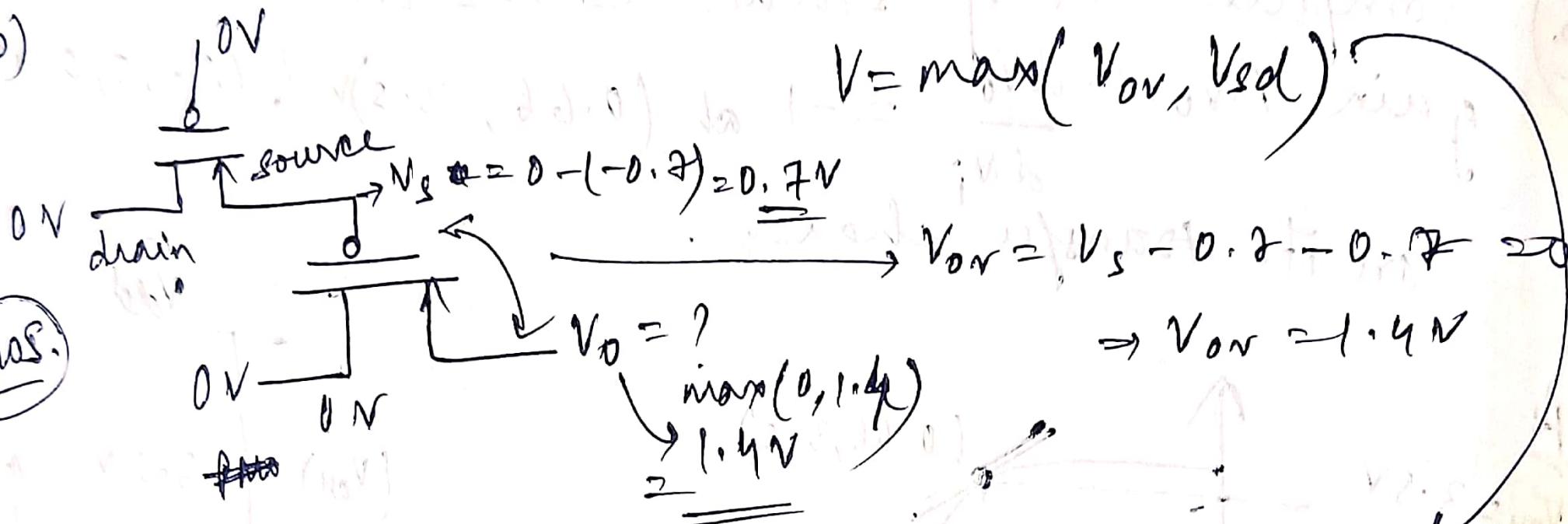
$$V_{ds} = 0.7V, V_{tp} = 0.7V, V_{tp} = -0.7V$$



$$V_o = \min(V_{on}, V_{ds})$$

$$= 2.9V$$

(b)



$$V = \max(V_{ov}, V_{sd})$$

$$V_{ov} = V_s - 0.2 - 0.7 = 0$$

$$\Rightarrow V_{ov} \approx 1.4V$$

we take max
because we
want to minimise
 V_d .

$$V_{sd} = V_{dd} - \underbrace{\min}_{\text{means max.}}$$

26/8/25