Analog & Digital VLSI Design

EEE/INSTR F313

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Problem 01

Using NMOS and resistors, implement (a) inverter, (b) $NAND_2$ gate, (c) NOR_2 gate, (d) $\overline{A+BC}$, and (e) $\overline{AB+CD}$. What are the disadvantages of the passive loaded logic circuits?

Problem 02

In the previous problem, replacing the passive load with a PMOS active load, we get the static CMOS logic. Using static CMOS, implement (a) inverter, (b) $NAND_2$, (c) NOR_2, (d) $\overline{A+BC}$, and (e) A+BC. How does the static CMOS resolve the issues with the passive loaded logic?

Problem 03

Compute the noise margins of a static CMOS inverter whose gain $A_{VO} = dV_{OUT}/dV_{IN} = -1$ at (0.66, 3.5) V and (2.35, 0.45) V on its transfer characteristics.

Problem 04

What are the values of V_{OUT} in the adjoining circuits? Given: $V_{TN} = -V_{TP} = 0.7$ V.