

Notation if \rightarrow nmos
if \rightarrow pmos

Tut-2 (21/8/25)

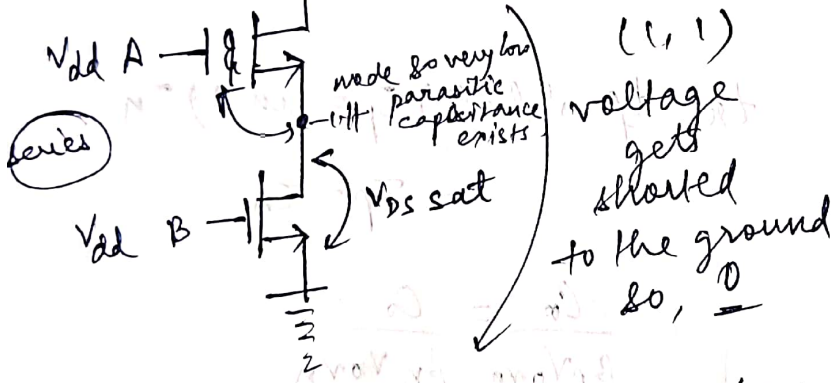
- Q1 Using nmos & resistors, implement (a) inverter (b) NAND₂ (c) NOR₂ & the func. (d) $A + BC$ & (e) $AB + CD$.
Disadvantages of passive loaded logic circuits?

A: (a) lecture



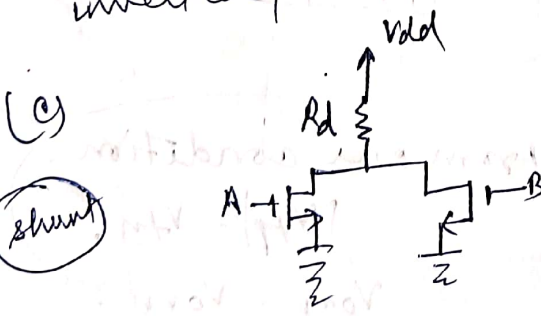
A	B	Y
0	0	1 $\rightarrow V_{dd}$
0	1	1 $\rightarrow < V_{dd}$
1	0	1 $\rightarrow < V_{dd}$
1	1	0 $\rightarrow 0$

Power taking a hit



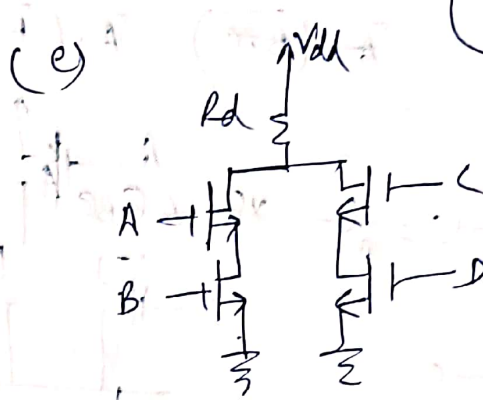
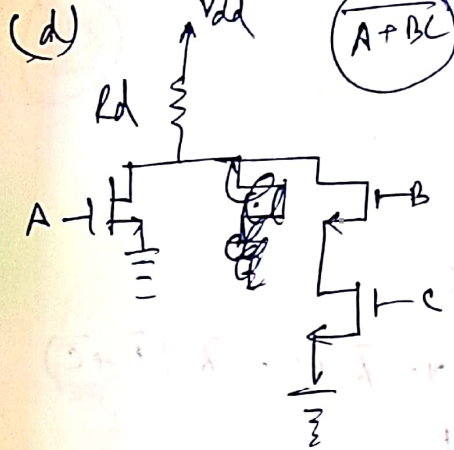
means pull down network

anything we do with pull down network will result in inverted form.



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

performance taking a hit

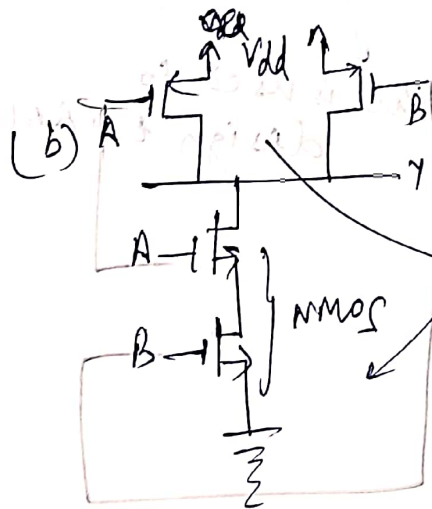


• means series
+ means shunt

Disadv: poor performance.

Q2 In prev. prob, replacing passive load with pmos active load, we get static CMOS logic. Implement (a) inverter, (b) NAND₂, (c) NOR₂, (d) $A + BC$, (e) $A + BC$. How does static CMOS resolve the issues with passive load logic?

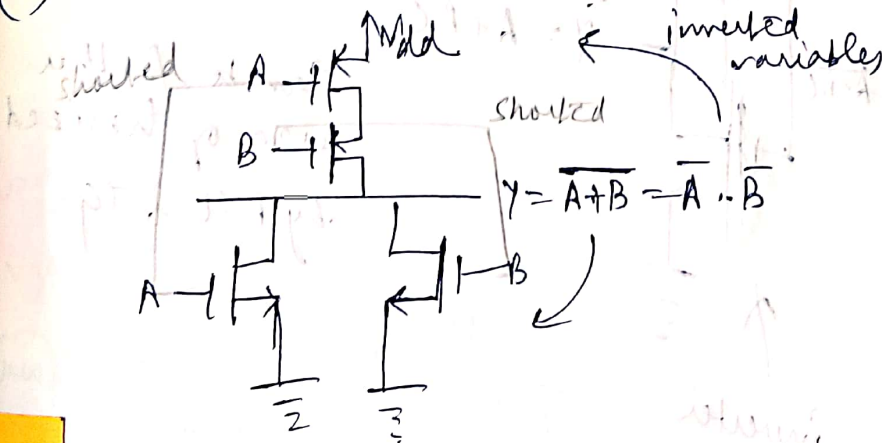
Ans: (a)



← inverted variables.

Both are PMOS.
So, ~~the~~ A & B are started with -ve voltages.
So, $\bar{A} \rightarrow A$ & $\bar{B} \rightarrow B$

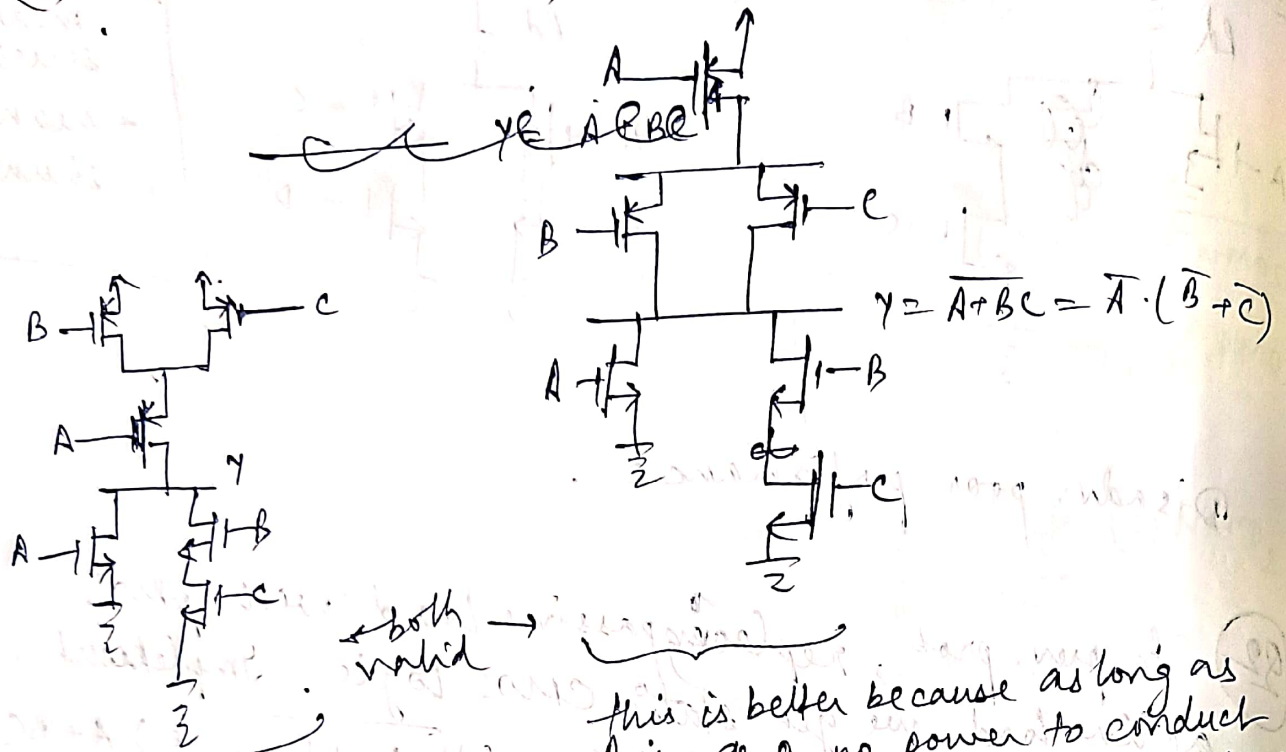
(c) $Y = \overline{A+B} = \bar{A} \cdot \bar{B}$



← inverted variables

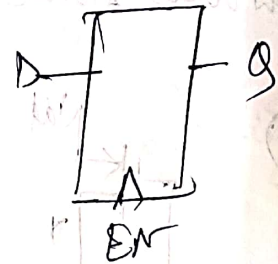
NAND is preferred b/c is the universal gates (NAND & NOR) because of better performance due to lower passive capacitance.

(d) $\overline{A+BC} = \overline{A \cdot (B+C)}$

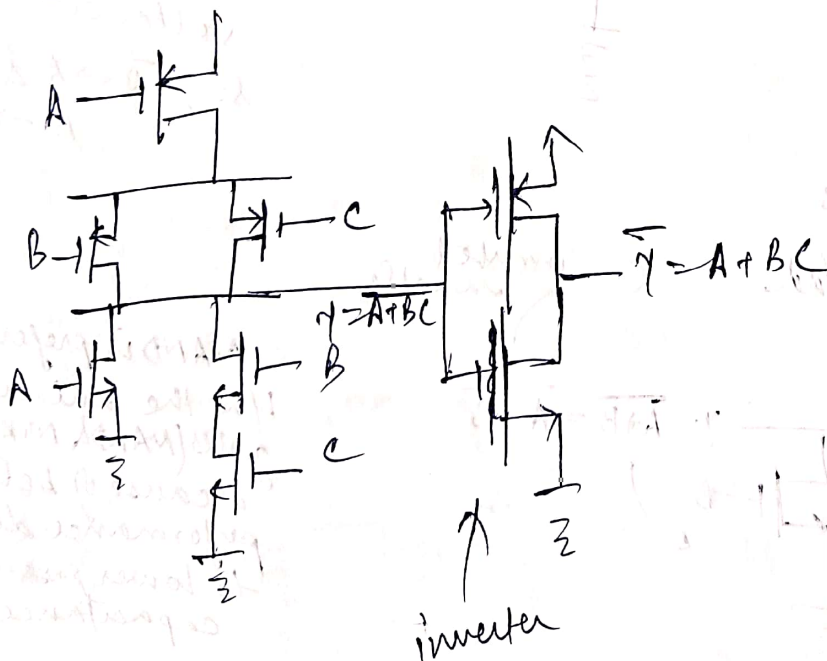


this is better because as long as A is not 0, no power to conduct to other nodes. So more efficient

this is used to design ENABLE

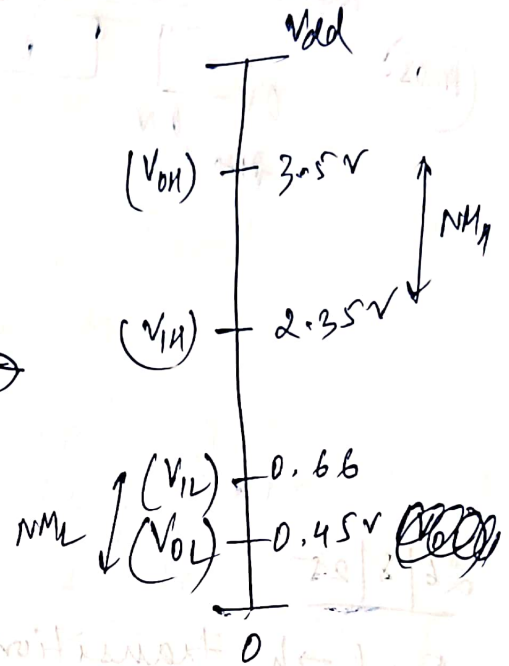
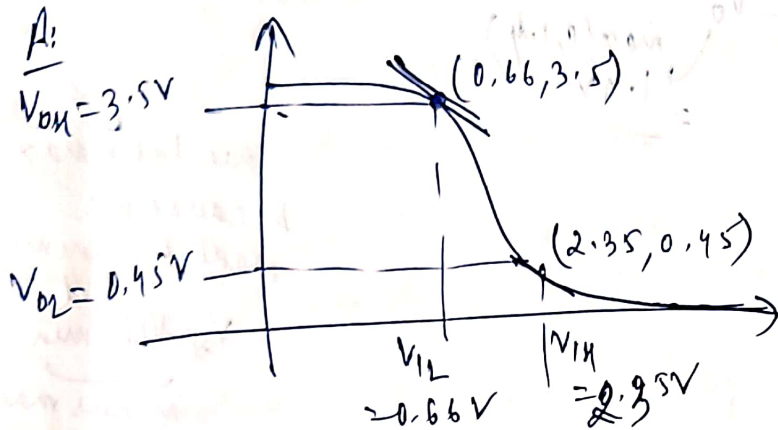


(e) $A+BC$



Can be further area optimized by PTL & TG

(Q3.) Compute NM of static CMOS inverter whose gain $A_{vo} = \frac{dV_o}{dV_i} = -1$ at $(0.66, 3.5)V$ & $(2.35, 0.45)V$ on its transfer char.



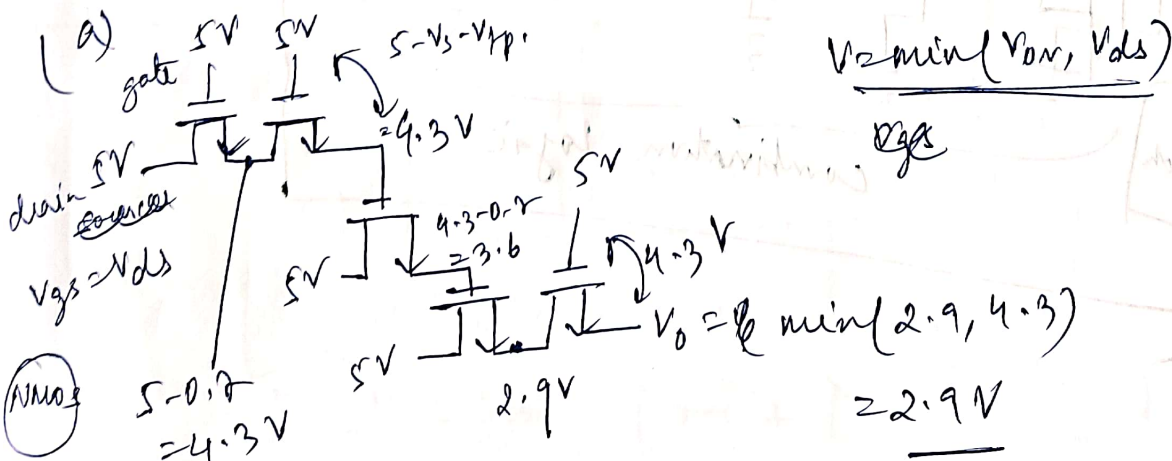
$$NM_H = (3.5 - 2.35)V = \underline{1.15V}$$

$$NM_L = (0.66 - 0.45)V = \underline{0.21V}$$

This is not a robust circuit as NM_L is too low. Ideally it should be close to $V_{dd}/2$.

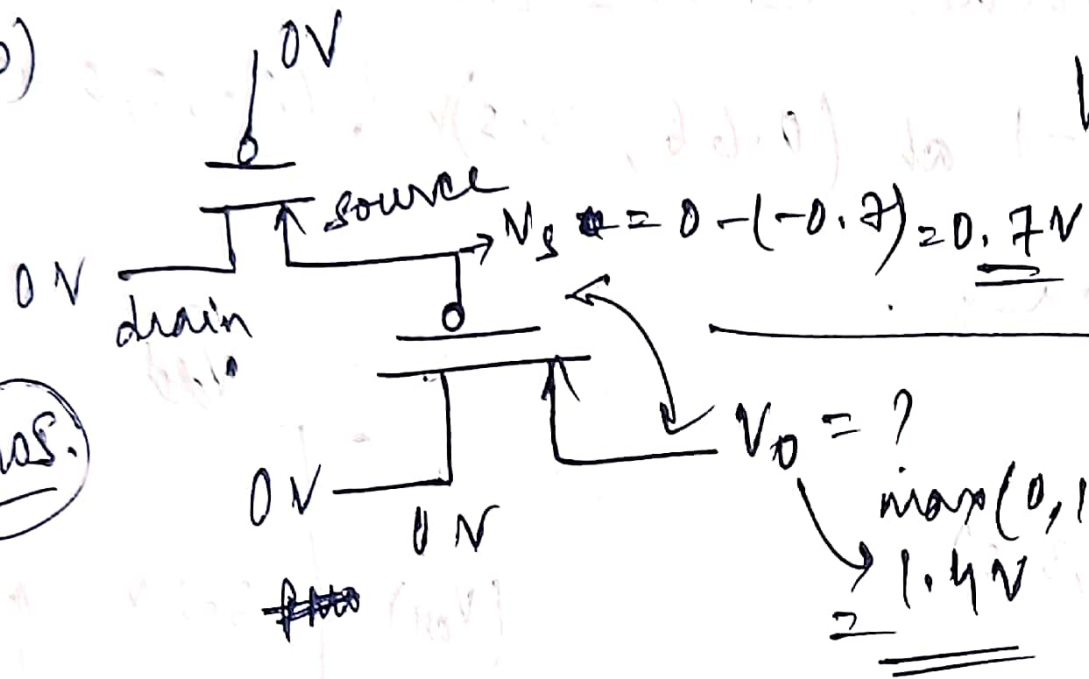
$$\text{Overall } NM = \min(NM_L, NM_H) = \underline{0.21V}$$

(Q4.) What are the values of V_o in the adjoining circuits?
 $V_{tn} = 0.7V$, $V_{thp} = -0.7V$



(b)

(PMOS)



$$V = \max(V_{ov}, V_{sd})$$

$$V_{ov} = V_s - 0.7 - 0.7 = 0$$
$$\Rightarrow V_{ov} = 1.4V$$

$$V_{out} = ?$$
$$\max(0, 1.4)$$
$$\underline{\underline{1.4V}}$$

we take max
because we
want to minimise
 V_{sd}
 $V_{sd} = V_{dd} - \min$
means max.

26/8/25