Analog & Digital VLSI Design

EEE/INSTR F313

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Tutorial 01

Problem 1

List the VLSI industry technology nodes below 1 μm, following the ITRS roadmap.

Problem 2

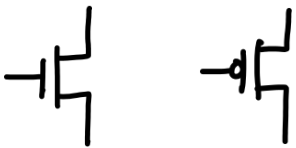
Find the on resistance of an nMOS transistor if $V_{ds} = 1.8$ V, $V_{gs} = 1.2$ V, and $V_{bs} = -1$ V. Assume $W/L = 10$, $V_{t0} = 0.45$ V, body effect coefficient $\gamma = 0.4$, $\mu_n C_{ox} = 300$ μA/V^2, and the Fermi potential of the Si substrate is $|\phi_F| = 0.3$ V.

Problem 3

For an nMOS transistor with $R_{on} = 600\ \Omega$ and the load resistance $R_L = 6\ \text{k}\Omega$, find out the output voltage when the input is high ($V_{dd} = 5\ \text{V}$). Comment on the values of R_L.

Problem 4

Under what conditions will the following pMOS and nMOS transistors turn on?

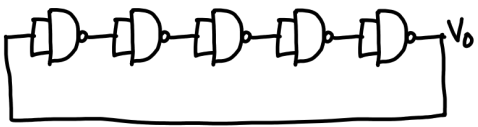


(a) (b)

Problem 5

(a) Estimate the frequency of the output signal V_{out} of the oscillator circuit shown below, given that the propagation delay $t_p = 30$ ns.

(b) What will be the frequency if we add another inverter to the chain?



Problem 6

Determine the modes of operation (saturation, linear, or cutoff) and the corresponding drain current I_D for each of the following biasing configurations: (a) Given: nMOS $k_n' = 115\ \mu A/V^2$, $V_{tn0} = 0.43$ V, $\lambda_n = 0.06$ /V, pMOS $k_p' = 30\ \mu A/V^2$, $V_{tp0} = -0.4$ V, $\lambda_p = -0.1$ /V. Assume $W/L = 1$ for all devices.

(a) nMOS $V_{gsn} = 2.5$ V, $V_{dsn} = 2.5$ V, pMOS $V_{gsp} = -0.5$ V, $V_{dsp} = -1.25$ V

(b) nMOS $V_{gsn} = 3.3$ V, $V_{dsn} = 2.2$ V, pMOS $V_{gsp} = -2.5$ V, $V_{dsp} = -1.8$ V

(c) nMOS $V_{gsn} = 0.6$ V, $V_{dsn} = 0.1$ V, pMOS $V_{gsp} = -2.5$ V, $V_{dsp} = -0.7$ V