Analog & Digital VLSI Design

EEE/INSTR F313

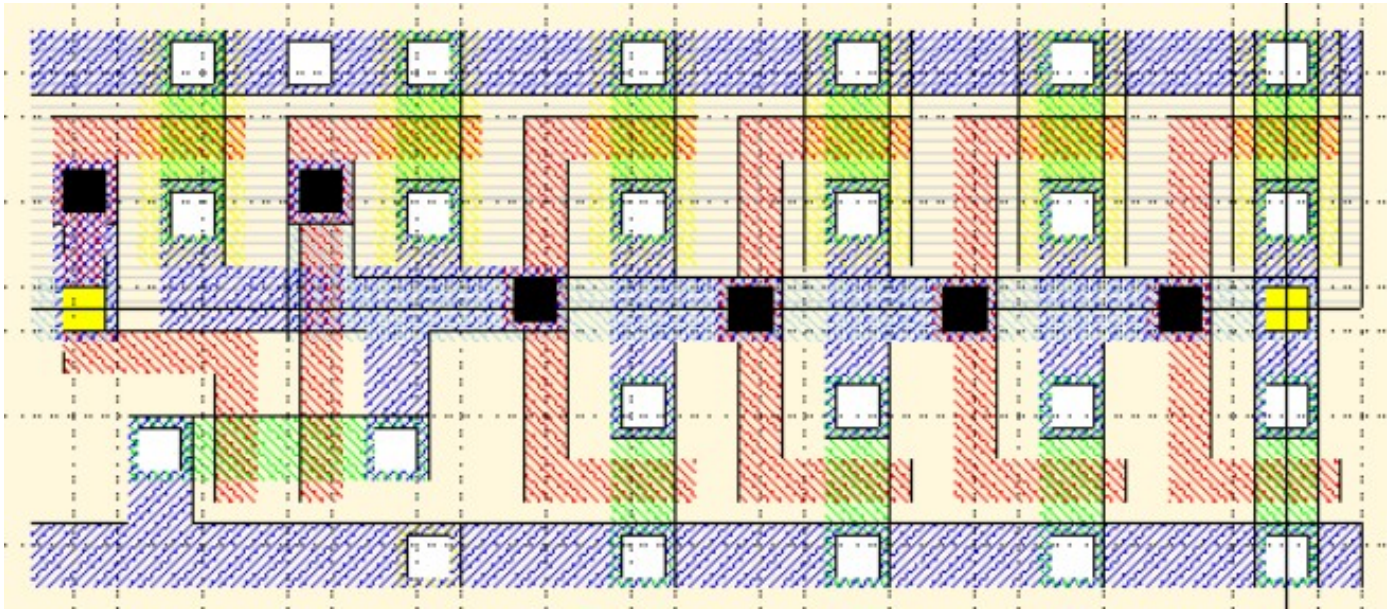
Dept. of Electrical & Electronics Engineering (EEE)

Birla Institute of Technology & Science (BITS) Pilani

Hyderabad Campus

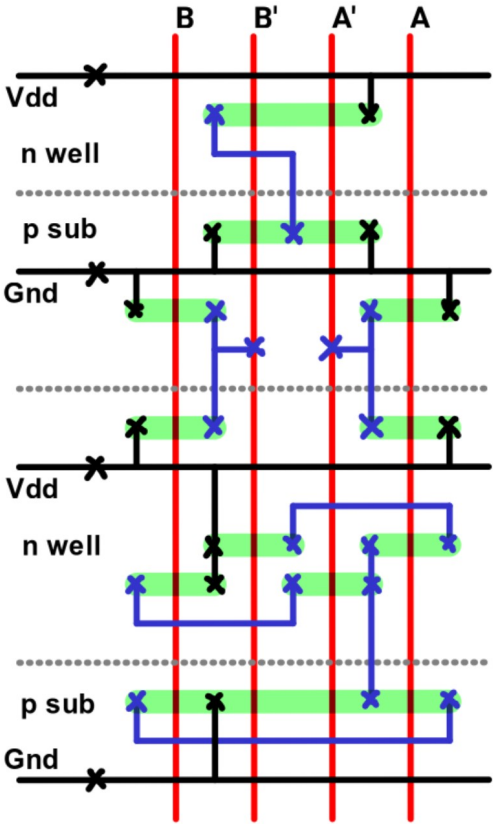
Problem 01

Draw the circuit schematics of the following physical layout and determine the function implemented by it.



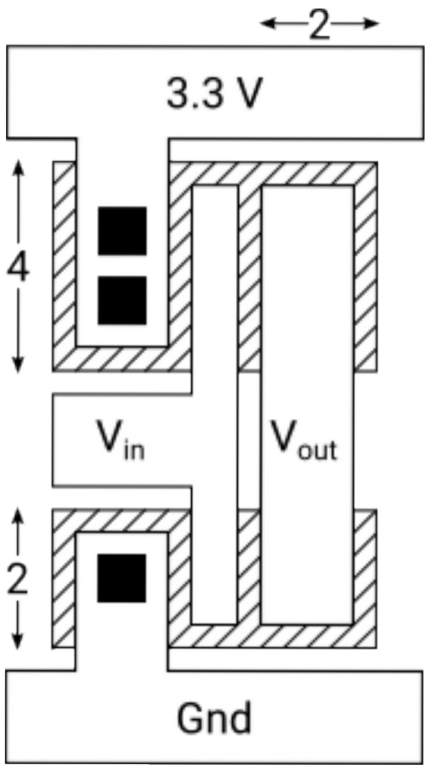
Problem 02

Draw the circuit schematics of the following stick diagram and determine the function implemented by it.



Problem 03

Consider the adjoining physical layout. All dimensions are in μm. L_G=1 μm, $L_{S/D}$=2 μm, L_{OV}=0.1 μm on each of S/D regions, V_{DD}=3.3 V, C_{OX}=2.5 fF/μm^2, C_{JP}=1 fF/μm^2, C_{JSWP}=0.3 fF/μm, C_{JN}=0.8 fF/μm^2, C_{JSWN}=0.2 fF/μm. Estimate the net parasitic capacitances (a) C_{DP} for the pFET (b) C_{DN} for the nFET and the (c) overall C_{OUT} for an FO_4 load.

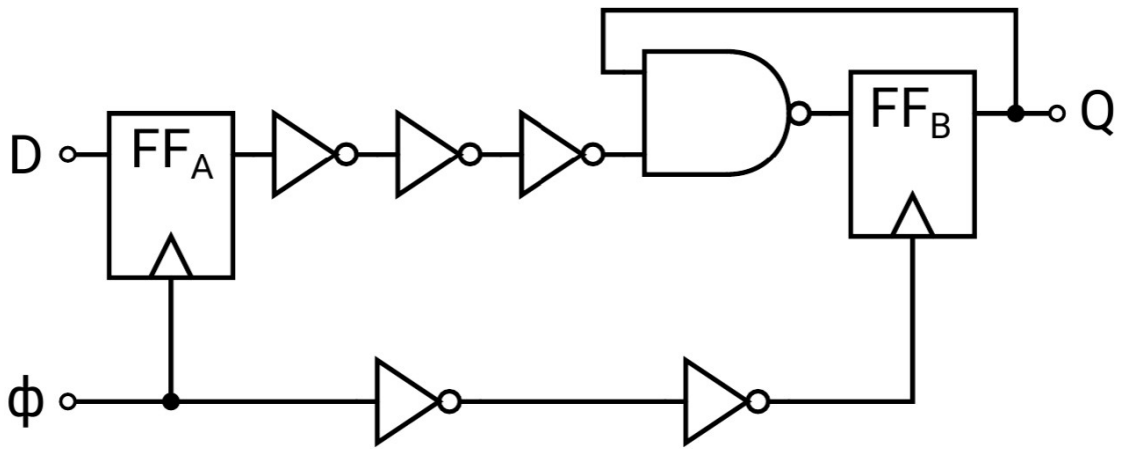


Problem 04

In a certain technology, assume that $\beta_N=\beta_P$, $V_{DD}=1.8$ V, and $V_{TN}=|V_{TP}|=0.6$ V. What are the values of the equivalent inverter thresholds of (a) 2-input $NAND_2$ and 3-input $NAND_3$ gates? (b) 2-input NOR_2 and 3-input NOR_3 gates?

Problem 05

The timing specifications for the circuit shown in the adjoining figure are: $t_{\Phi 2Q}$=2 ns, t_{sk}=1 ns, f_{Φ}=500 MHz, t_S=3 ns, t_H=6 ns, t_{PD}(INV)=1 ns, t_{PD}($NAND_2$)=2 ns. (a) If there is any hold violation, resolve the issue, and draw the rectified circuit. (b) If there is any setup violation, recommend the maximum operating frequency of the circuit, so that there will be no violations of any kind, under any circumstances.



Problem 06

Consider the function F=∑m(3, 4x, 5, 7, 9, 10, 11, 13, 14x, 15x), where x denotes the don't care terms. Using minimum number of FETs, realize the static CMOS implementation of function F with the appropriate sizing that will ensure the worst case performance equates that of the standard static CMOS inverter in the same technology node.