Analog & Digital VLSI Design

EEE/INSTR F313

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Tutorial 11

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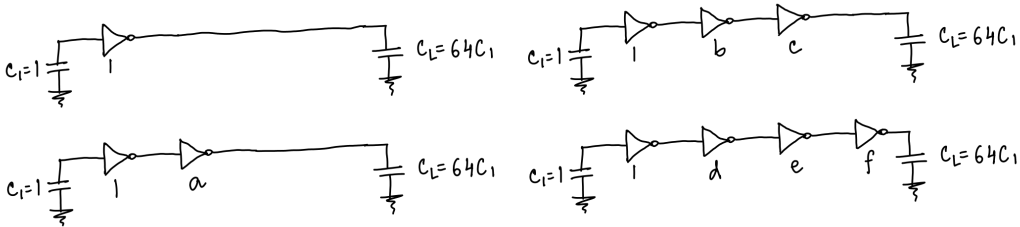
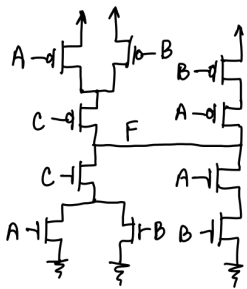
Problem 1

For the following arrangements calculate sizing (a, b, c, d, e, and f) to get least delay. Compute the delays for each of the arrangements. Also find the optimum number and compare with the results (given: $\gamma = 1$, $t_{P0} = 1$ ns).



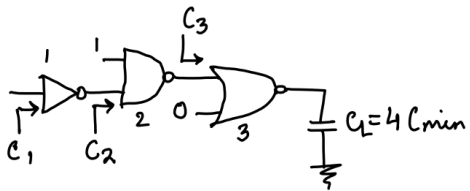
Problem 2

For the following circuit, find the widths of all the transistors so that the rise time and fall time delays will be the same as of the minimum sized symmetrical inverter in the worst case. Also, find the logical efforts of A and C inputs (given: $\mu_N = 2\mu_P$).



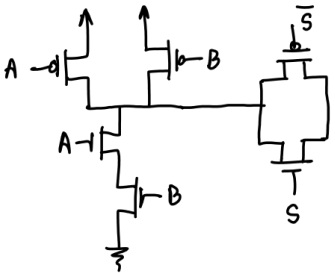
Problem 3

Estimate the overall chain delay of the circuit shown below:



Problem 4

In the adjoining circuit, at what sizing of the transmission gate will the logical effort of the select line equate the input signals?



Problem 5

Analyze the cascade shown below and find the size of each of the gates for the minimum path delay. Given: C_{IN} = 20 fF, C_{OUT} = 500 fF, $r = \mu_N/\mu_P$ = 2.5, calculate the (a) path effort, (b) optimal stage effort, (c) minimum path delay, (d) individual loads of every stage, and the (e) minimum capacitance in the technology node.