Analog & Digital VLSI Design

EEE/INSTR F313

Dept. of Electrical & Electronics Engineering (EEE)

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Problem 01

Derive the expressions for (a) rise time, (b) fall time, and (c) propagation delay using the transient analysis of basic RC networks, where the NFETs and PFETs are approximated as linear resistors with resistances $R_N = 1/\beta_N V_{OV}$ and $R_P = 1/\beta_P V_{OV}$. As discussed in the lecture, this approach, though simpler to handle than the actual situation, overestimates the delays, leading to benchmarking the “worst-case maximum frequency” popular in the industry.

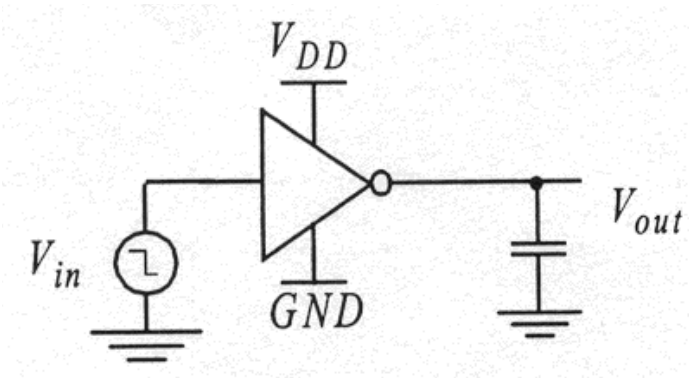
Derive the expressions using both differential equations as well as Laplace Transforms formulations.

Problem 02

In the adjoining figure, the transistors in the static CMOS inverter can be modeled as constant linear resistors (when turned on) V_{DD} = 2.5 V, C_L = 25 pF. As usual, assume that the input signal has a very steep slope and is stable before the out starts to switch.

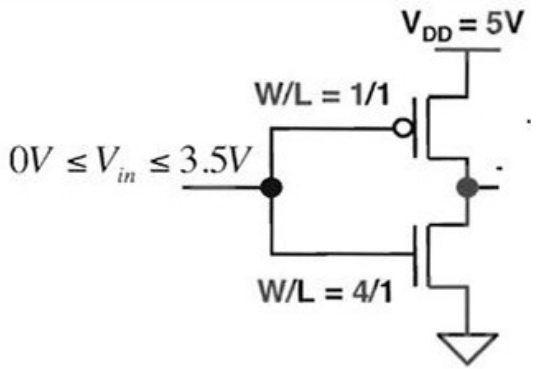
(a) For a 1 → 0 transition at the input, determine the transistor resistances that will result in a 10% → 90% of V_{DD} transition on the output within 5 ns.

(b) Draw a rough sketch of the the current drawn from the power supply as a function of time during this low-to-high transition, and derive the appropriate equations that describe that behavior.



Problem 03

In the adjoining static CMOS inverter, assume $V_{OH} \approx V_{DD} = 5$ V, $\mu_N C_{OX} = 500\ \mu A/V^2$, $\mu_P C_{OX} = 200\ \mu A/V^2$, $V_{TN} = -V_{TP} = 1$ V. Input is varied within the range $0 \le V_{IN} \le 3.5$ V. Compute the value of V_{OL}.



Problem 04

Design (a) NOR_2 gate, and (b) $NAND_3$ gate with rise and fall times same as the symmetrical static CMOS inverter at the same technology mode with minimum delay. Take $\mu_N = 2\mu_P$.