Analog & Digital VLSI Design

EEE/INSTR F313

Dept. of Electrical & Electronics Engineering (EEE)

Birla Institute of Technology & Science (BITS) Pilani

Hyderabad Campus

Problem 01

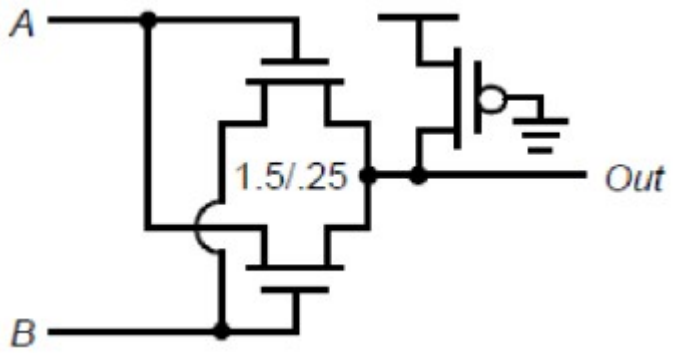
Implement the logic function F = ABD + CD using pseudo-nMOS logic?

Problem 02

Implement $F = A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot C \cdot D$ (and $\overline{F}$) in Differential Cascode Voltage Switch Logic (DCVSL). Assume A, B, C, and D, and their complements are available as inputs. Use the minimum number of transistors.

Problem 03

Determine the truth table for the adjoining circuit. What logic function does it implement?

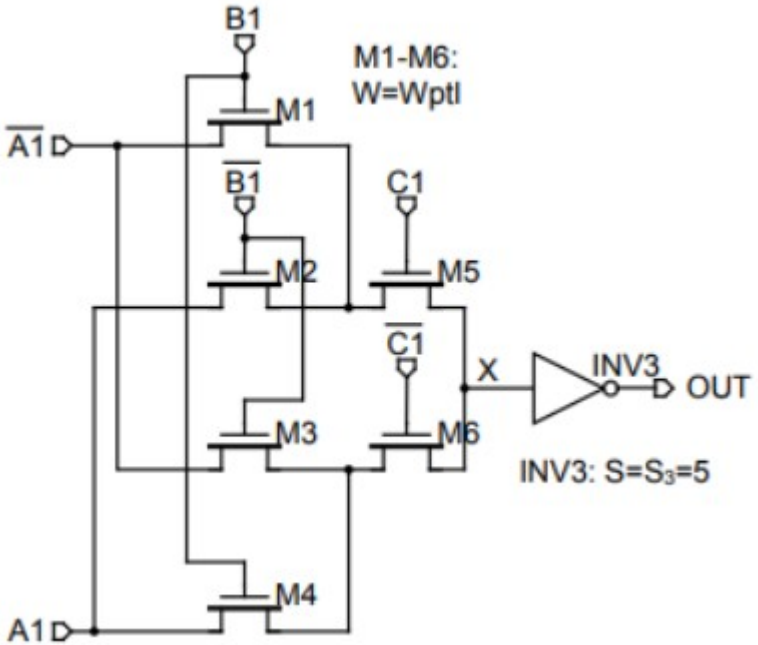


Problem 04

Implement the function $S = A \cdot B \cdot C + A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot \overline{C}$, which gives the sum of two inputs with a carry bit, using nMOS pass transistor logic. Design a DCVSL gate which implements the same function. Assume A, B, C, and their complements are available as inputs.

Problem 05

What is function OUT of the adjoining circuit as a function of the A, B and C inputs?



Problem 06

Assume the inverter in the adjoining circuit switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance throughout this problem.

(a) What is the logic function performed by this circuit?
(b) Explain why this circuit has non-zero static dissipation.
(c) Using only a single transistor, design a fix so that there will not be any static power dissipation. Explain how you chose the size of the transistor.
(d) Implement the same circuit using transmission gates.
(e) Replace the PTL network with another PTL network that computes X = ABC, given that both true and complementary forms of A, B and C are available.