Analog & Digital VLSI Design

EEE/INSTR F313

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Problem 01

A static CMOS inverter with minimum sized FETs has $\beta_N = 0.2\ \text{mA/V}^2$, $\beta_P = 0.1\ \text{mA/V}^2$, $V_{TN} = -V_{TP} = 0.6\ \text{V}$, and $V_{DD} = 3.3\ \text{V}$.

(a) What is the inverter switching threshold V_M?
(b) What is the resistance for each FETs?
(c) What are the rise and fall times of the circuit if the output node parasitic capacitance is 9 fF, ignoring any load?
(d) As a consequence, estimate the maximum operating frequency of the circuit.
(e) What are the propagation delays for an additional load of 25 fF?

Problem 02

A certain circuit has a datapath (5, 4) and a clockpath (4.5, 4.1). Find the setup and hold times of the circuit, given that the (max, min) denote the maximum and minimum propagation delays in ns.

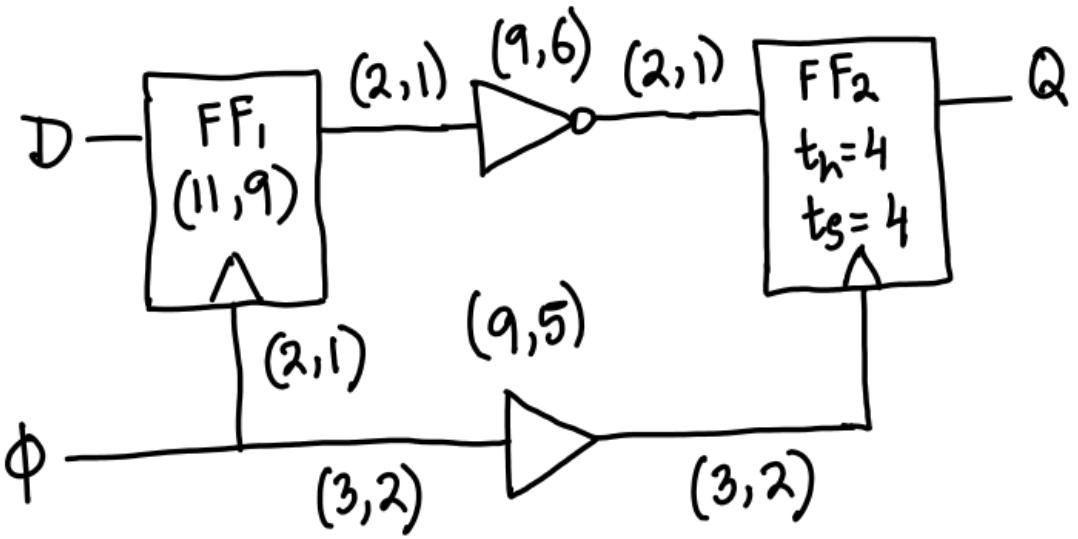
Problem 03

Perform the static timing analysis of the following circuit to

(a) Determine the setup & hold violations, if the f_{Φ} = 66.7 MHz and the $t_H = t_S$ = 4 ns at the capture FF.

(b) What should be the maximum allowable t_H to prevent the hold violation?

(c) What are the measures to resolve the setup violation?



Problem 04

(a) Complete the PDN.
(b) Identify the function F.
(c) Size all the transistors so that the worst case delay is same as that of the symmetrical static CMOS inverter. Take $\mu_N = 2\mu_P$.