→ Ideally if, $V_{tn} = |V_{tp}| = \frac{V_{dd}}{2}$ → NM_H =

→ $V_o < V_{OL}$ or $V_o > V_{OH}$ ✓ Good

$V_{IL} < V_o < V_{IH}$ × Bad

→ We need R_L load for gain

R_C load for performance with

Tut-1 (14/8/25)

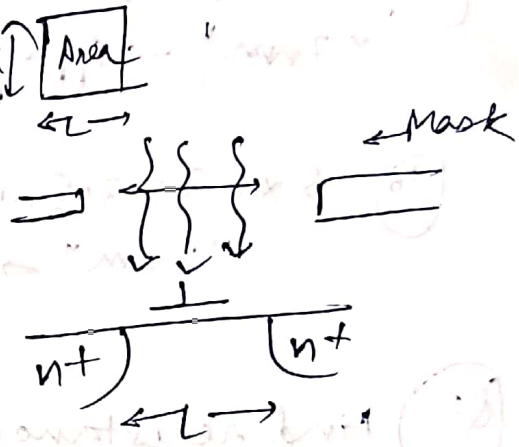
(1) List the VLSI industry tech nodes below 1 μm following I.T.R.S:

Soln: International Tech Roadmap for semiconductor

area → $A_{new\ node} = \frac{A_{prev\ node}}{2}$

L = Effective channel length.

$L_{new\ node} = \frac{L_{old\ node}}{\sqrt{2}} = 0.7 L_{old\ node}$



(1) 1000 × 0.7 = 700 nm

↓ "0.7 μm"

"1 μm"

(2) 700 × 0.7 = 490 nm

called "0.5 μm"

(3) 500 × 0.7 = 350 nm

"(0.35 μm)"

$V_{dd} = 5V$

(4) 350 × 0.7 = 245 nm

"0.25 μm"

$V_{dd} = 2.5V$

(5) 250 × 0.7 = 185 nm

"180 nm"

Intel Pentium III

(6) 180 × 0.7 = 126 nm

= "0.13 μm"

(7) $130 \times 0.7 = 91$ nm
"90 nm" Intel P4 – first nano-electric device

(8) $90 \times 0.7 = 63$ nm $\Rightarrow$ "60 nm" $\rightarrow$ Qualcomm SD;

(9) $65 \times 0.7 = 45.4$ nm $\Rightarrow$ "45 nm" $\rightarrow$ Intel i7

(10) $45 \times 0.7 = 31.5$ nm $\Rightarrow$ "32 nm"

(11) $32 \times 0.7 = 22.4$ nm $\approx$ "22 nm"
Beyond 22nm, no more MOSFETs.
$\Rightarrow$ Now FinFETs below 22nm

(12) $22 \times 0.7 = 15.4$ nm
"16 nm or 14 nm".
Apple A9

(13) $14 \times 0.7 = 9.8$ nm
"10 nm"
intel i9 (Tiger Lake Pro)

(14) $10 \times 0.7 = 7$ nm
"7 nm" $\rightarrow$ Apple A12 Bionic

(15) $7 \times 0.7 = 4.9$ nm
"5 nm" (Apple M1)

(16) $5 \times 0.7 = 3.5$ nm
"3 nm" $\rightarrow$ Apple A17/M4 $\rightarrow$ Iphone 15 Pro. (Current Tech)
Pro

(Q2) Find resistance of NMOS trans. if $V_{DS} = 1.8V$, $V_{GS} = 1.2V$, $V_{BS} = -1V$. Assume $\frac{W}{L} = 10$, $V_T = 0.45V$, body effect $\Rightarrow \gamma = 0.4$, $\mu_n C_{ox} = 300 \mu A/V^2$.
Fermi pot. of Si substrate is $|\phi_F| = 0.3V$

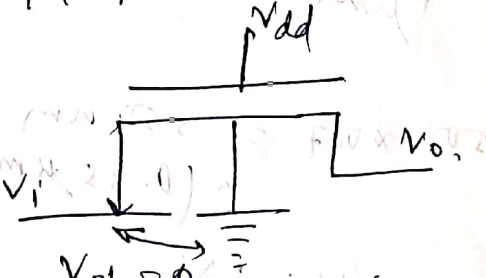
A: $V_{sb} = V_s - V_b = 0$

$V_{sb} = V_0$

$V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_F}\right)$

$= 0.45 + 0.4\left(\sqrt{2 \times 0.3 + 1} - \sqrt{2 \times 0.3}\right)$

$= 0.646V$



$\Rightarrow$ NMOS is worst to pass on "strong" signal

$V_o(\text{"1"}) = 1 - 0.65 = 0.35\,V$ less than $\frac{V_{dd}}{2}$ so NM useless.

$\Rightarrow$ passes "0".

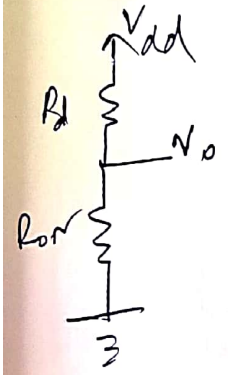
$$R_{on} = \frac{1}{\beta V_{ov}} = \frac{V_{ds}}{I_d}$$

$$I_d = \beta\left(V_{ov} - \frac{V_{DS}}{2}\right) V_{DS}$$

$$R_{on} = \frac{1}{30\mu \times 10 \times (1.2 - 0.646)} = 601.68\ \Omega$$

Q3 For NMOS trans with $R_{ON} = 600\ \Omega$, $R_L = 6k\Omega$. Find o/p voltage when input is high ($V_{DD} = 5V$). Comment on values R_L

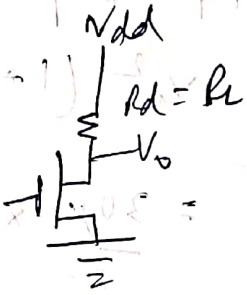
A: R_{ON} → transistor behaves like linear resistor



$$V_o = \frac{R_{ON}}{R_{ON} + R_L} V_{dd}$$

$$= \frac{0.6}{0.6 + 6} \cdot 5$$

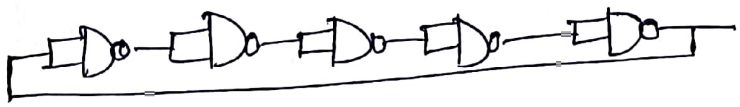
$$= 0.45V$$

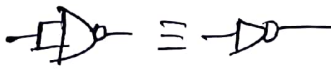


We don't want gain to depend on R_L $\Rightarrow$ we increase R_{ON}

Q4 (a) Freq. of V_{OUT} of oscillator circuit, given propagation delay $t_p = 30ns$.

(b) what will be f_2 if we add another inverter.





Ans:

add no. of inverter $\Rightarrow$ toggle

even no of " $\Rightarrow$ remains same $\Rightarrow$ memory.

(b) $f = 0$.

(a)  $f = \frac{1}{5 \cdot 2 \cdot 30 \cdot 10^{-9}}$ → 3.33 MHz

Q6: NMOS

$K_n' = 115\,\mu A/V^2$, $V_{TN_0} = 0.43V$, $\lambda_N = 0.06/V$, $\frac{W}{L} = 1$

$K_p' = 30\,\mu A/V^2$, $V_{TP_0} = -0.4V$, $\lambda_P = -0.1/V$, $\frac{W}{L} = 1$

(a) NMOS $V_{gs} = V_{ds} = 2.5V \Rightarrow$ Deep sat.

$$I_d = \frac{\beta}{2} \times V_{ov}^2 (1 + \lambda V_{DS})$$

$$= \frac{115\mu}{2} \times 1 \times (2.5 - 0.43)^2 (1 + 0.06 \times 2.5)$$

$$= 283.3\,\mu A$$

PMOS

$V_{sg} = 0.5V$, $V_{sp} = 1.25V$

$V_{ov} = 0.5 - 0.4 = 0.1V$

MP = Deep sat.

$$I_s = \frac{\beta_p}{2} V_{ov}^2 (1 + |\lambda| V_{sp})$$

$$= \frac{30\mu}{2} \times 1 \times (0.1)^2 (1 + 0.1(1.25))$$

$$= 0.17\,\mu A$$