Analog & Digital VLSI Design

EEE/INSTR F313

Dept. of Electrical & Electronics Engineering (EEE)

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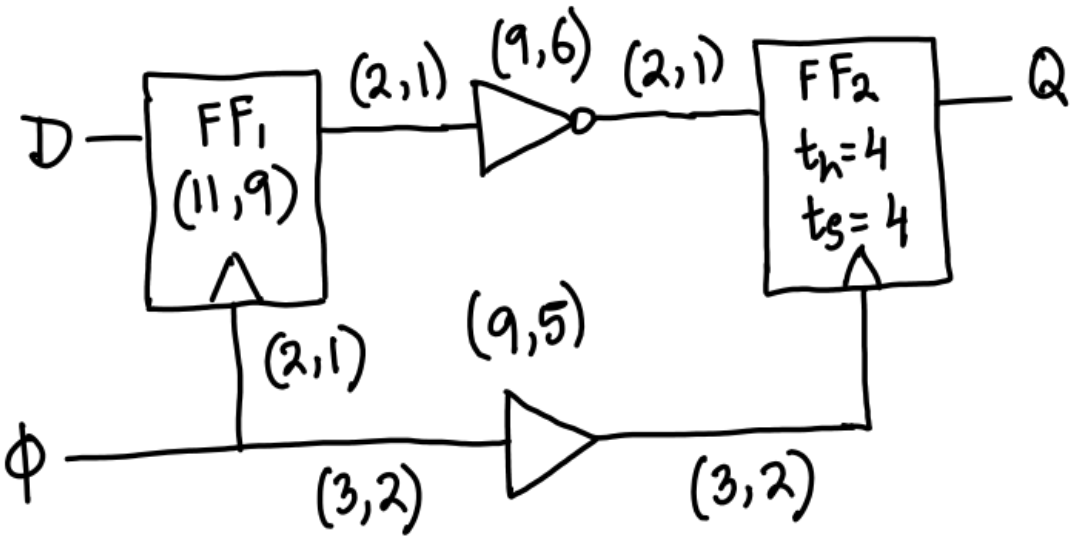
Problem 01

Perform the static timing analysis of the following circuit to

(a) Determine the setup & hold violations, if the f_{Φ} = 66.7 MHz and the $t_H = t_S$ = 4 ns at the capture FF.

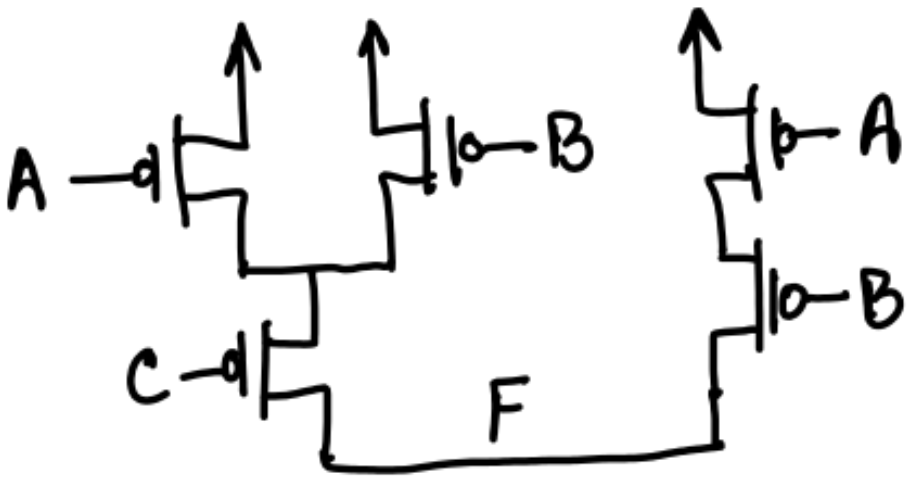
(b) What should be the maximum allowable t_H to prevent the hold violation?

(c) What are the measures to resolve the setup violation?



Problem 02

(a) Complete the PDN.
(b) Identify the function F.
(c) Size all the transistors so that the worst case delay is same as that of the symmetrical static CMOS inverter. Take $\mu_N = 2\mu_P$.

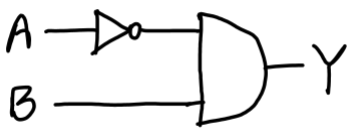


Problem 03

Implement the function $\overline{Y} = (A + B)\cdot C\cdot D$. Size the NFET and PFET devices such that the propagation delays are the same as the CMOS inverter with an NMOS with $(W/L)_N = 4$ and a PMOS with $(W/L)_P = 8$.

Problem 04

Calculate the switching activities of the following combinational functions, assuming equiprobable inputs:



Problem 05

Consider a processor which can operate in two different modes: (i) Mode 1: a high voltage mode (1 V, 3 GHz), and (ii) Mode 2: a low voltage mode (0.75 V, 2 GHz). What is the ratio of switching power consumption of mode 1 : mode 2?