Analog and Digital VLSI Design

EEE/INSTR F313

Tutorial 10

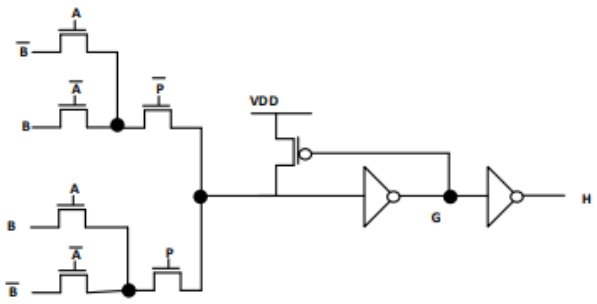
Surya Shankar Dan

Department of Electrical and Electronics Engineering (EEE)
Birla Institute of Technology and Science (BITS) Pilani, Hyderabad Campus

Thu 6th Nov, 2025

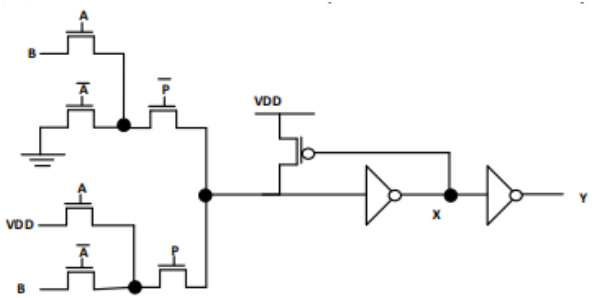
Problem 01

For the adjoining circuit, the inverters are realized using static CMOS logic. Write the Boolean equation for G and H.



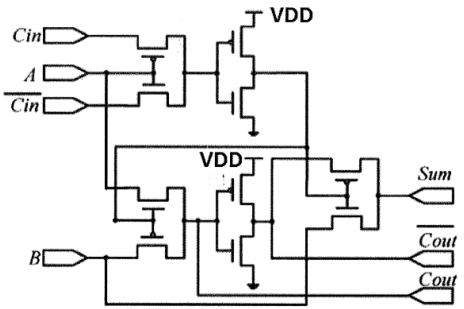
Problem 02

For the below circuits, the inverters are realized using static CMOS logic. Write the Boolean equation for X, Y.



Problem 03

For the circuit shown below, write the expression for SUM is $C_{out} = (A \oplus C_{in})\, B + (A \odot C_{in})\, Y$. The value of Y is _____. Assume pass transistors as ideal switches.

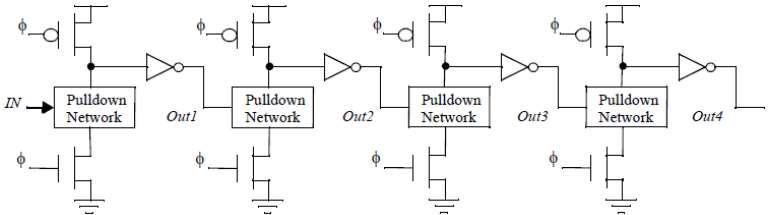


Problem 04

Design a 4-bit look-ahead-carry adder using multiple-output domino CMOS logic (MODL).

Problem 05

Consider a conventional 4-stage domino logic circuit as shown in the adjoining figure in which all precharge and evaluate devices are clocked using a common clock ϕ. For this entire problem, assume that the pull-down network is simply a single nMOS device, so that each domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all $T/2$. Assume that the transitions are ideal (zero rise/fall times). Complete the timing diagram for signals OUT_1, OUT_2, OUT_3, and OUT_4, when the IN signal goes high before the rising edge of the clock ϕ. Assume that the clock period is $10T$ time units.



Problem 06

For the adjoining circuit, the maximum clock frequency for reliable operation is _____ GHz. NAND2 gate delay=20 ps, NOR2 gate delay=30 ps, XOR2 gate delay=50 ps, NOT gate delay=15 ps, FF1: $t_{\phi q}$ = 50 ps, t_{setup} = 30 ps, t_{hold} = 10 ps, FF2 : $t_{\phi q}$ = 35 ps, t_{setup} = 50 ps, t_{hold} = 10 ps.