Analog & Digital VLSI Design

EEE/INSTR F313

Dept. of Electrical & Electronics Engineering (EEE)

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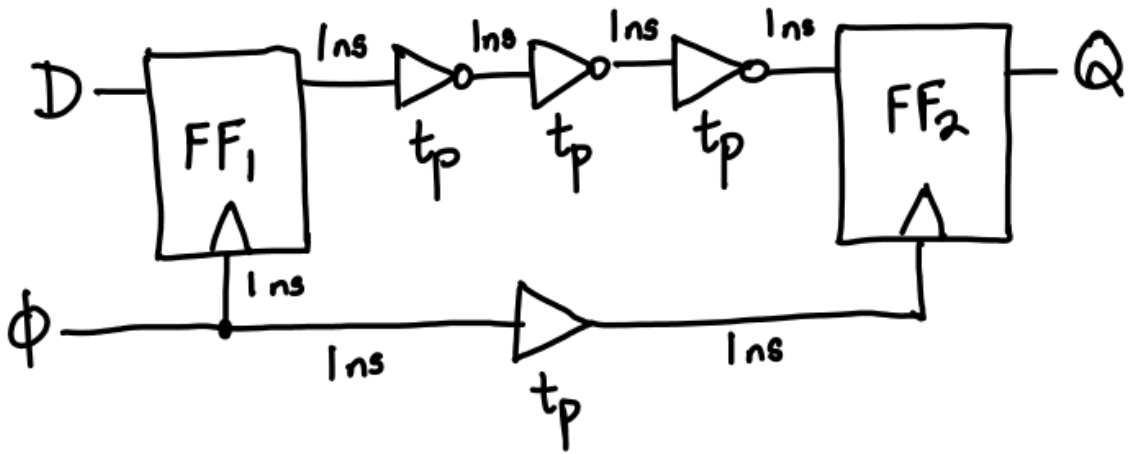
Problem 01

In a certain circuit with C_{OUT}=1 pF, R_N=R_P=100 kΩ, the maximum voltage level that is registered as logic “0” is 25% of the power supply V_{DD}, while the minimum voltage level that is registered as logic “1” is 85% V_{DD}. (a) What is the rise time t_R? (b) What is the fall time t_F? (c) What is the maximum operating frequency f_{MAX} of the circuit?

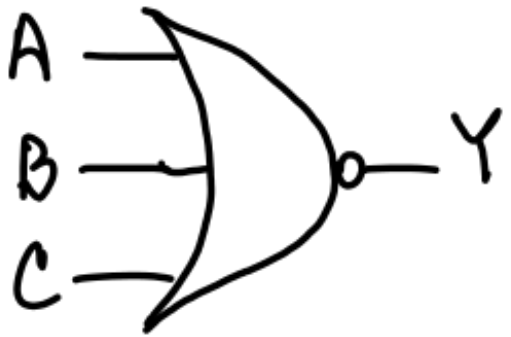
Problem 02

In the combinational logic block of the adjoining circuit, each of the inverters and the buffer have the same time constant τ=0.1 µs, and the identical flip-flops FF_1 and FF_2 have the same clock-to-Q delay $t_{\Phi 2Q}$=6 ns, setup and hold times t_S=2 ns & t_H=3 ns. (a) What is the propagation delay t_P of the combinational logic block? (b) What is the maximum delay in the data path t_D(max)? (c) What is the minimum delay in the clock path t_Φ(min)? (d) What is the maximum operating frequency f_Φ(max) for the overall front-end system that will ensure no setup violations at all?



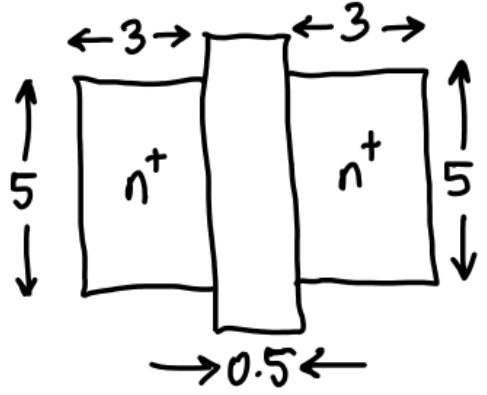
Problem 03

Consider a 3-input NOR_3 gate with transistors having τ=0.1 µs, β=1 µA/V^2, f=1 GHz, V_{DD}=1 V, V_T=0.35 V. (a) What is the switching activity α of the gate? (b) What is the risetime of the gate t_R? (c) What is the switching power P_{SW} while driving a 1 pF load and the (d) short circuit power P_{SC} dissipation of the gate?



Problem 04

The dimensions in the adjoining NMOSFET layout are in µm. Calculate the net terminal capacitances in fF. Given: L_{OV}=50 nm, C_{OX}=2.7 fF/µm^2, C_J=0.86 fF/µm^2, C_{JSW}=0.24 fF/µm from the technology library.



Problem 05

Draw a stick diagram layout for a typical NOR_3 gate implemented in static CMOS technology.