Manual for Communication Systems Laboratory (EEE/ECE F311)

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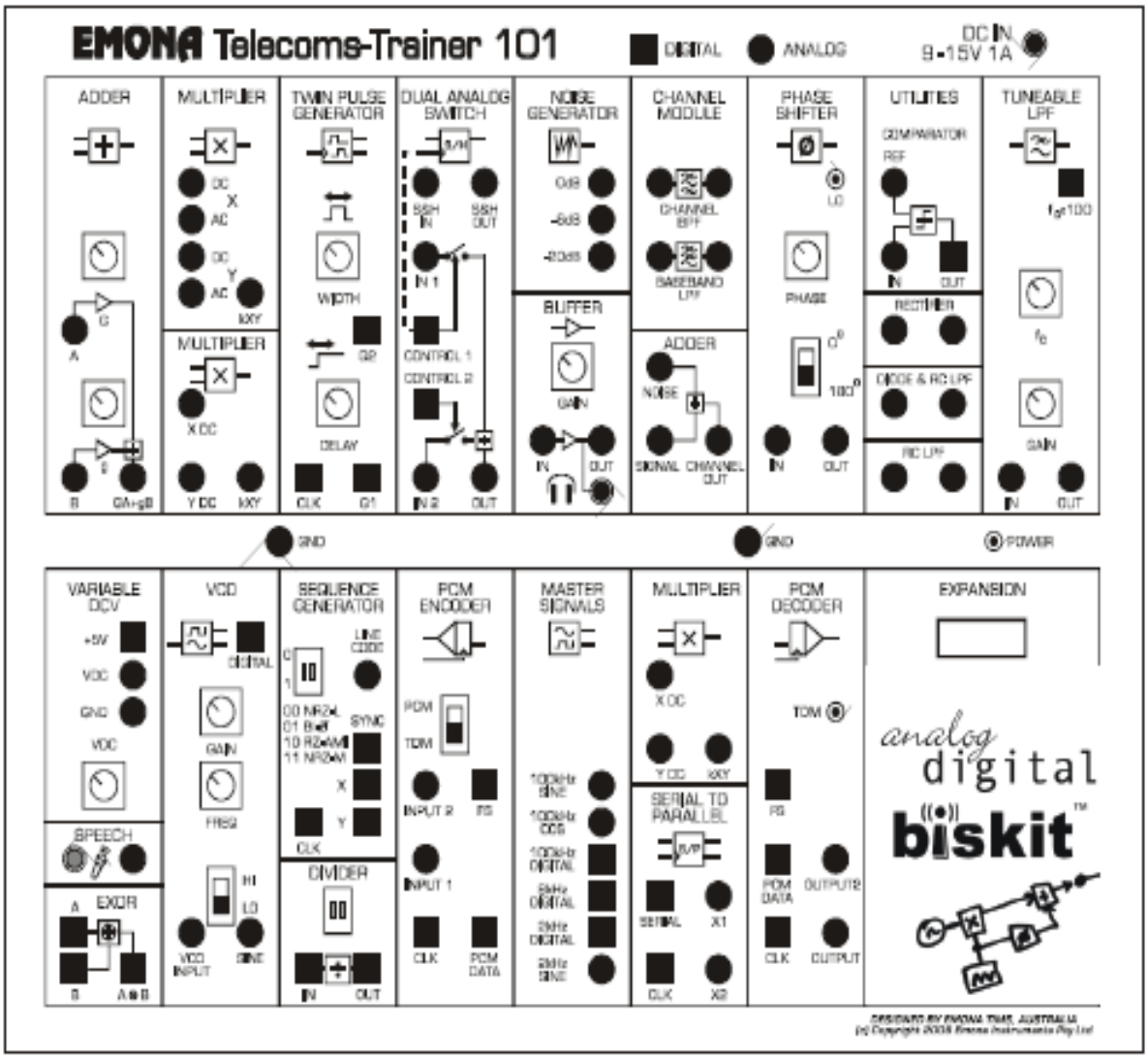
Experiment 6: PLL Characterization and FM Demodulation

Aim: This experiment is intended to make the student to perform experiments based on Phase Locked Loop (PLL) using Emona Telecoms-Trainer 101 kit and 101-21 extension kit.

Equipment Required: Emona Telecom Trainer Kit 101,101-21 Extension Kit, Oscilloscope, connecting patch cards etc.



A. Introduction to PLL:

A phase-locked loop (PLL) is an electronic circuit with a voltage- or current-driven oscillator that is continuously adjusted to match in phase, and thus lock on to frequency of an input signal.See Figure 1. It consists of a combination of phase detector, low pass filter and a VCO which is used in a combination involving negative feedback such that such that the output signal can be driven at a frequency equal to input signal. Suppose the input signal is $x_1 = A_1\sin(\omega t + \theta_1)$ and the other signal is $x_2 = A_2\cos(\omega t + \theta_2)$ then, as shown in Figure 1, we can see the inputs x_1 and x_2 applied at points A and B. At point C we have the output after multiplication and by the trigonometric simplification we get $(A_1A_2 / 2)$ $[\sin(2\omega t + \theta_1 + \theta_2) + \sin(\theta_1 - \theta_2)]$, which after passing through the low pass filter, appears as$K \sin(\theta_1 - \theta_2) = K \sin\theta_e$at D, where K is a constant dependent on A_1A_2 and gain / attenuation factors of the LPF. This voltage signal is fed to the VCO which generates a signal, whose frequency is altered in proportion to the phase difference θ_e. When the phase at points A and B are equal then$\theta_e=0$ and both the signals are in phase and thus frequency and phase locking is achieved.

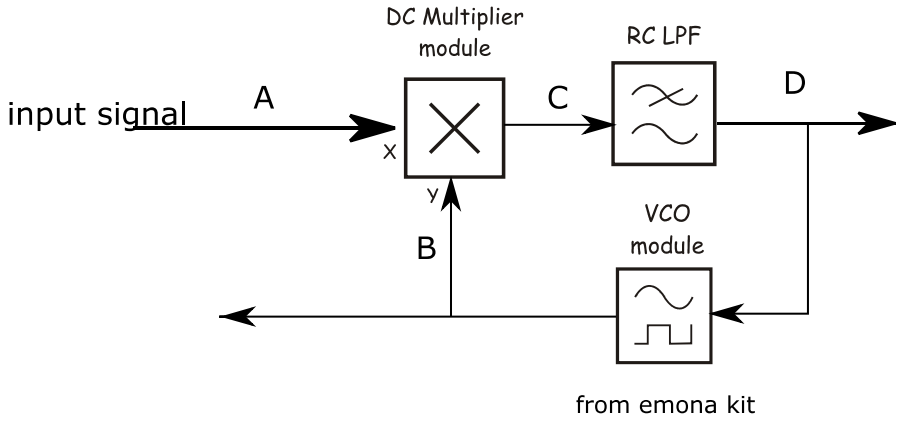


Figure 1- PLL Block Diagram

B – Demonstration of PLL

In this section, we will be observing how a PLL works. See Figure 2. It consists of two major groups of blocks, one is the PLL circuit and the other is the one that generates signal with varying frequency. ***The PLL uses the VCO present on the Emona Kit. The VCO for the signal generator block is taken from the extension board, plugged onto the Emona kit.***

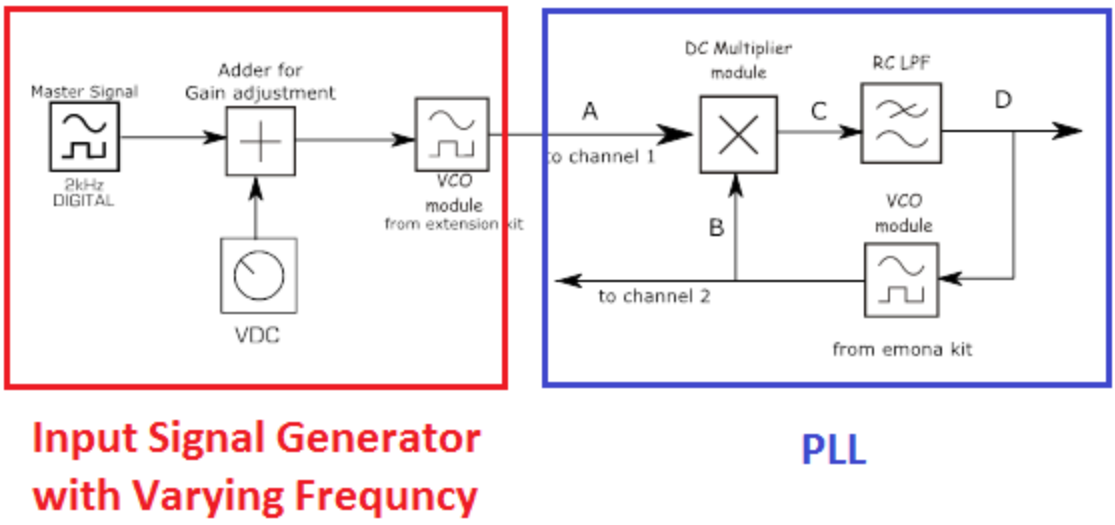


Figure 2- Block Diagram to Observe PLL Locking

As you can deduce from Figure 2, if we feed a square wave signal with peak to peak voltage of + V to –V to the ***VCO in the input signal generator block***, the input signal to the PLL will have a sinusoid whose frequency switches between two values, based on the initial settings of the VCO frequency and the VCO gain. We expect the PLL to track these changes in the input frequency and at Point B in the Figure 2, one should have a signal that closely follows the signal at Point A.

To demonstrate this, you may follow the steps given below:

a) Use the Gain in the adder module and Master Signal's module to obtain a square wave with excursion from -2 to 2V. You may take the help of Variable DC voltage module of the Emona kit to adjust the voltages and get a mean value of 0V.

b) ***The settings that you are making in this step are for both the VCOs***.

   i. Set the VCO module's Range control to the **LO** position.
   ii. Turn the VCO module's Frequency Adjust control so as to have a nominal frequency of 10 KHz.
   iii. Turn the VCO module's Gain Adjust control to the middle position.
   iv. Make sure that both the VCO's in the EMONA kit have these settings. ***Do not disturb these settings.***

c) Complete the connections as in Figure 2.

d) Initially, connect the square wave signal to Channel 1 and the ***output of the VCO on extension board, to Channel 2 of the DSO***. Trigger the DSO with Channel 1 and adjust the frequency scale control knob of DSO to display one LOW and one HIGH portions of the square wave, with transition from LOW to HIGH at the middle of the screen. Observe the display. You will have a signal whose frequency is different during low portion of the square wave to the High portion of the square wave. Is this expected and if so why?

e) Now, connect the points A and B to ***Channel 1*** and ***Channel 2*** of the DSO respectively. Observe the waveforms at points A and B in the DSO. If you are not able to trigger the waveforms, you can use the RUN/STOP feature of the DSO to observe a clear waveform. (Figure 3 is given for reference). Comment on your observations.

f) Do both the signals at A and B have the similar behavior? If yes, does this mean that the PLL is locking and the tracking the changes in the frequency of the incoming signal?

g) Do you observe any phase lag between the two signals? Comment on it.

h) Try to measure the frequency of the signals, as available on the screen, using measurement procedure you learned earlier. Is the frequency 10 KHz (same as you have set initially)? If not why? Comment on this observation.

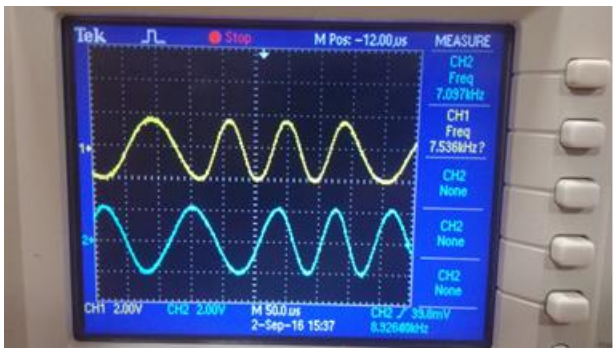


Figure 3 – PLL Tracking signal and VCO Generated signal (Old DSO Model No. TDS 2012C)

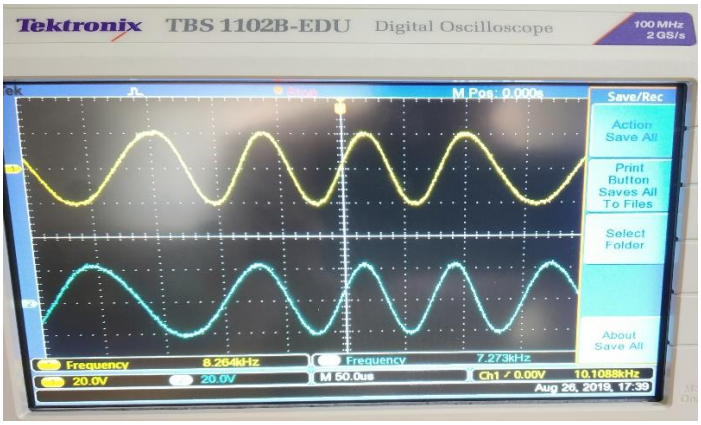


Figure 3 – PLL Tracking signal and VCO Generated signal (New DSO Model No. TBS 1102B-EDU)

i) Try to observe the signal at Point D. Should it have some relation to the square wave that is driving the VCO on the extension board?

C –Measurements on the Frequency Locking Range of PLL

From the experiment in Part B, you have observed that the PLL locks and the changes in the frequency of the incoming signal are tracked continuously. We now seek to obtain the locking ranges for the PLL over which it tracks the frequency of the signal at the input.

For proceeding meaningfully, first we need to characterize the VCO in the PLL loop, as it was done in Frequency Modulation Experiment. Use the connection diagram in Figure 4.

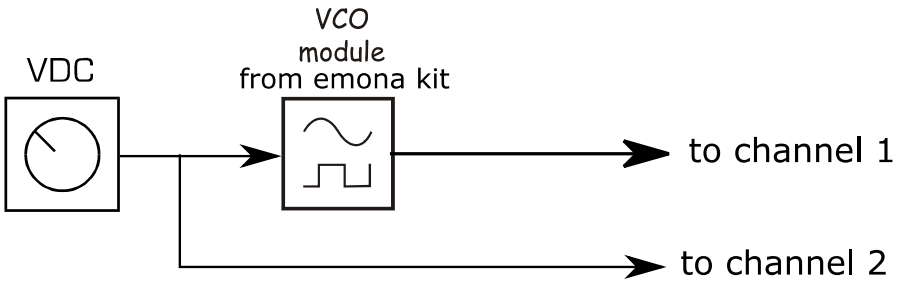


Figure 4- Connection Diagram for VCO Characterization

You may follow the steps given below:

a) Set the VCO (in the PLL) module's Range control to the **HI** position. Turn the VCO module's Frequency Adjust control so as to have a nominal frequency of 100 KHz. **Turn the VCO module's Gain Adjust control to Right position (→) position. *Do not disturb these settings.***

b) Turn the VDC control in one direction and tabulate the values of voltage and frequency. ***Make sure that Channel 2 is in DC Coupling mode***. Change the direction of rotation of the VDC controland tabulate the values of voltage and frequency.(You may take any 3 readings on either side). It is advised to use the voltage values between -3V to +3V.

c) Plot a graph between VCO's input Voltage and Frequency of the VCO output. You may use the graph sheet, provided to you, for plotting the graph. (Refer to Figure 7 for Sample plot). Calculate the slope of this plot as ***Slope1***. You will realize the need for this plot after going through few more steps.

d) Do not disturb the VCO gain and VCO frequency control settings.

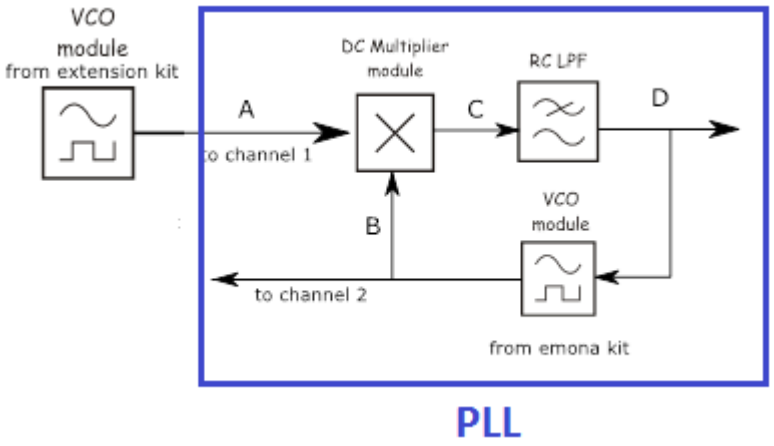


Figure 5- Connection Diagram for PLL locking Range Measurement

a) Next, for the VCO on the extension module set the VCO module's Range control to the **HI** position. Turn the VCO module's Frequency Adjust control so as to have a nominal frequency of 100 KHz. **Turn the VCO module's Gain Adjust control to middle position.*Do not disturb these settings.***

b) Next, rig up the PLL circuit and connect the output of the VCO of the extension module to the input multiplier of the PLL. See Figure 5.

c) Now, turn the frequency knob of the ***VCO in Extension kit*** slightly in the anti-clock wise direction, observe the signal obtained at point A connected to Channel 1 and measure its frequency.

d) How does the Signal at point B change? Does this signal have the same frequency as that of the signal at Point A? If it is same, does it mean that the PLL has tracked the change in the input signal frequency correctly? See Figure 6.

e) Keep turning, slowly, the frequency knob of the ***VCO of the extension board*** in the anti-clock wise direction and observe the tracking behavior of the PLL.

f) As you are turning anti-clock wise, after some position, you may observe that the frequency measurement at Point B is quite different from that of at Point A. ***It may also be observed that the signal at Point B has a frequency that is 100 KHz, as set initially.*** This implies that the PLL is no more locking to the incoming signal frequency. The lowest frequency at which the PLL perfectly locks is denoted by f_L. Tabulate this value in Table 1.

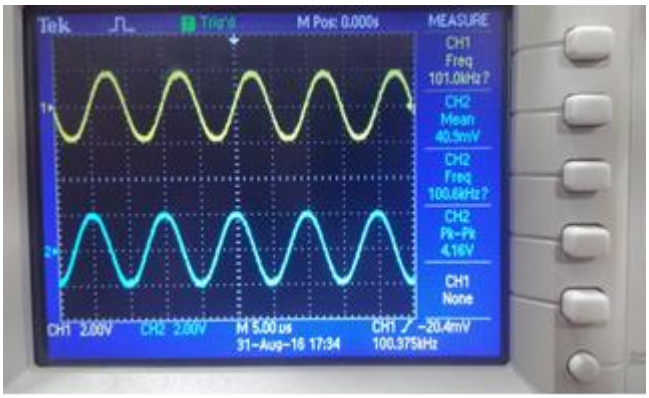


Figure 6- PLL Locked signal with respect to incoming signal

(Old DSO Model No. TDS 2012C)

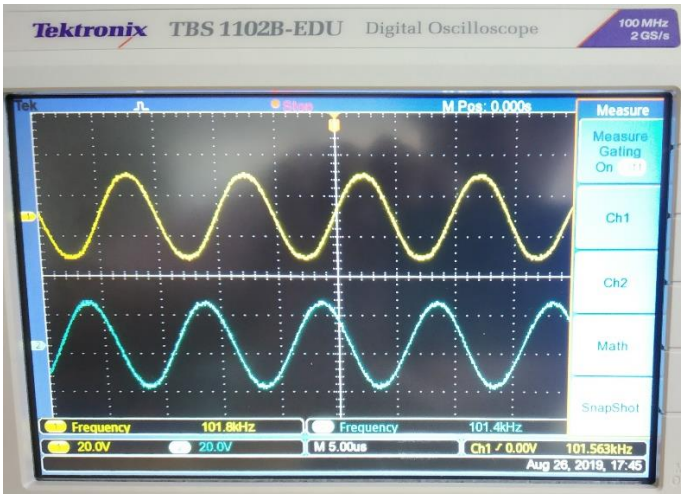


Figure 6- PLL Locked signal with respect to incoming signal

(New DSO Model No. TBS 1102B-EDU)

g) Now turn slowly, the frequency knob of the ***VCO of the extension board*** in the clock wise direction and observe the tracking behavior of the PLL. Keep turning the frequency knob and observe that the frequency measurement at Point B is quite different from that of at Point A. This implies that the PLL is no more locking to the incoming signal frequency. The highest frequency at which the PLL perfectly locks is denoted by f_H. Tabulate this value in Table 1.

h) The locking range, for the current settings of the ***VCO in PLL*** is given by ***(f_H–f_L).***

i) On the plot, as in Figure 7, draw lines parallel to the X-axis, corresponding to ***f_L*** and ***f_H*** and note the Voltage values corresponding to the points where the horizontal lines intersect the VCO characterization curve, and tabulate in Table 1.

S.No	Gain Knob position of the VCO in PLL block	Start Frequency ***f_L***	End Frequency ***f_H***	Locking Range (***f_H–f_L***)	***Voltage corresponding to f_L***	***Voltage corresponding to f_H***
1	Right position **(⟶)**					
2	Left position **(⟵)**					

Table 1

j) Now repeat the experiment with the ***gain knob of VCO in emona kit adjusted to left position (⟵).*** For this, first we need to characterize the VCO for this gain position, as was done for the gain position **(⟶)** and plot the graph between DC voltage and the VCO frequency. You will have to recalculate ***Slope 2*** value by plotting the graph.

k) For this new position of the VCO gain settings for the PLL, measure the ***f_L*** .and ***f_H*** and tabulate in Table 1.

l) Again, on the plot, as in Figure 7, draw lines parallel to the X-axis, corresponding to these new ***f_L*** and ***f_H*** corresponding to the new VCO gain position (⟵) and note the Voltage values corresponding to the points where the horizontal lines intersect the VCO characterization curve, and tabulate in Table 1.

m) Compare the range of voltage values obtained from Table 1 for different gain positions and comment on your observations.

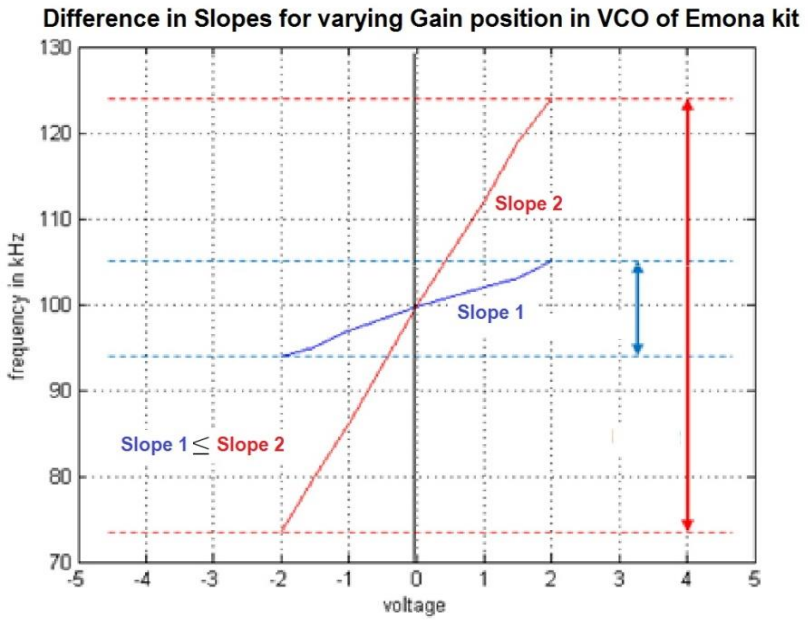


Figure 7- VCO Characterization for Different VCO gain positions

D – PLL Based Demodulation of Frequency Modulated Signal:

As you are aware, the PLL tracks the changes in the frequency of the incoming signal. In FM signal, the message signal modulates the frequency of a carrier. Thus, it is understandable that one can use PLL effectively to track the changes in the frequency of the FM signal and hence recover the message signal.

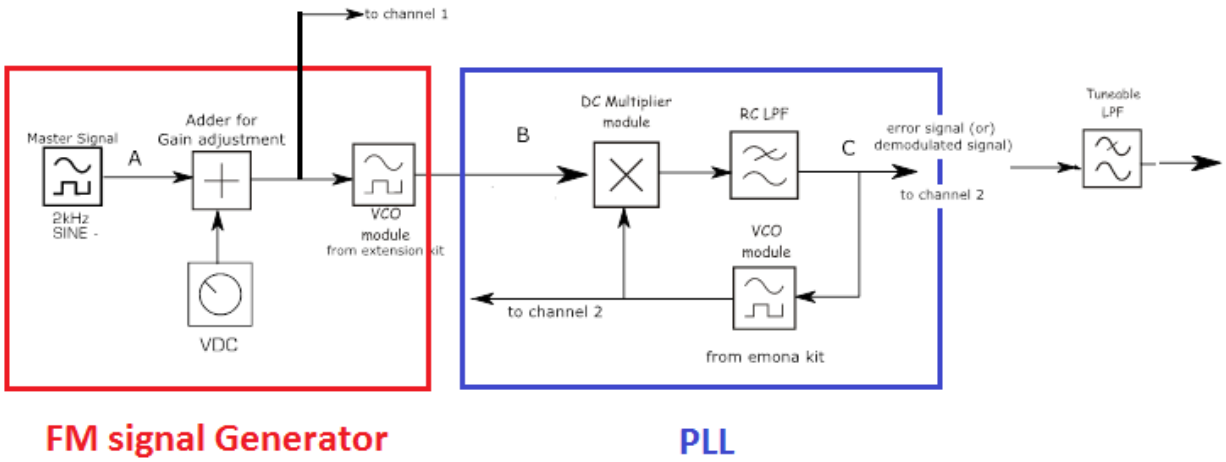


Figure 8- FM Demodulation Block Diagram

a) Generation of an FM signal:
    i. Set the Nominal frequency of the VCO on the extension board to 10 Khz. Let the amplitude of the VCO output signal is default value). Make sure that the VCO gain adjustment knob is in the middle.

    ii. Generate a message signal, with 2KHz sine and peak to peak voltage of 2V. The mean value is to be zero for this signal. You may use the adder module along with DC variable voltage signal to create a message signal with above parameters.

    iii. Generate an FM signal by connecting the message signal to the input of the VCO on the extension board.

b) Set the nominal frequency of the VCO of PLL to 10 KHz. Make sure that the VCO gain adjustment knob is in the middle.

c) Apply the modulated FM signal to the PLL at point B.

d) One may recall here that the error signal corresponding to the phase difference between the incoming signal and the VCO (in PLL) appears at Point C and is the one that is helping the PLL to track the incoming signal frequency. Since the message signal is the one that is creating variations in the frequency of the incoming signal, the error signal at Point C is precisely the demodulated message signal. Observe the demodulated message signal at C.

e) If you don't have a clear signal, you may connect the output of the RC LPF to a Tunable LPF to observe the demodulated signal. Adjust the cutoff frequency of Tunable LPF such that you get a clear waveform. You can use the Gain knob of the tunable LPF for amplitude adjustment.

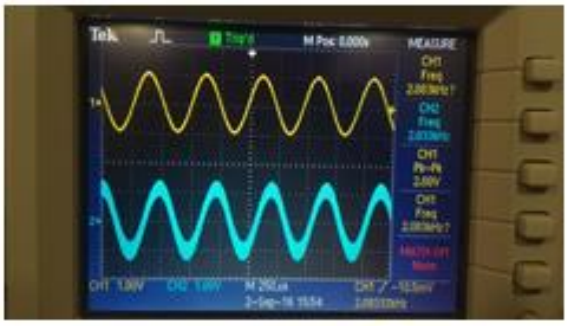


Figure 8- Demodulated signal after RC LPF

(Old DSO Model No. TDS 2012C)

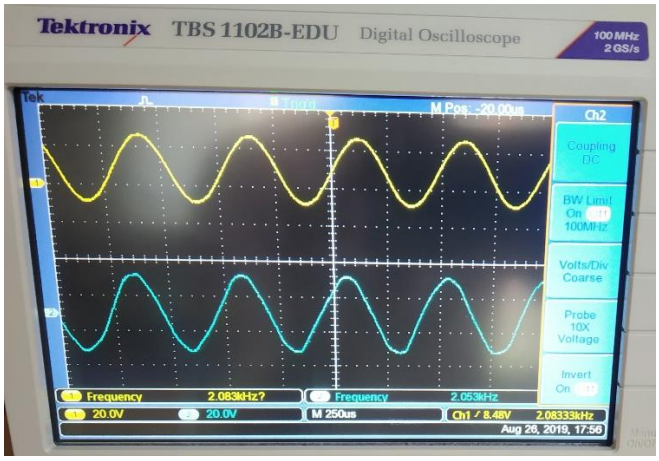


Figure 8- Demodulated signal after RC LPF
(New DSO Model No. TBS 1102B-EDU)

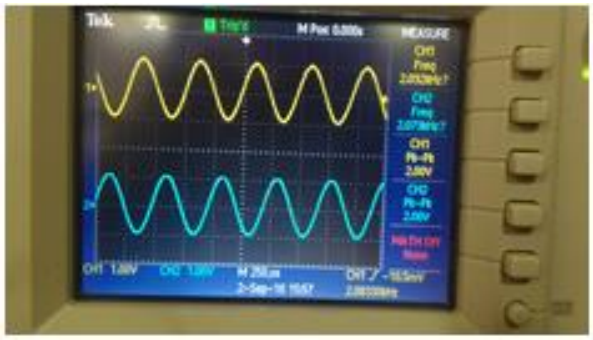


Figure 9- Demodulated signal after RC LPF and Tunable LPF

(Old DSO Model No. TDS 2012C)

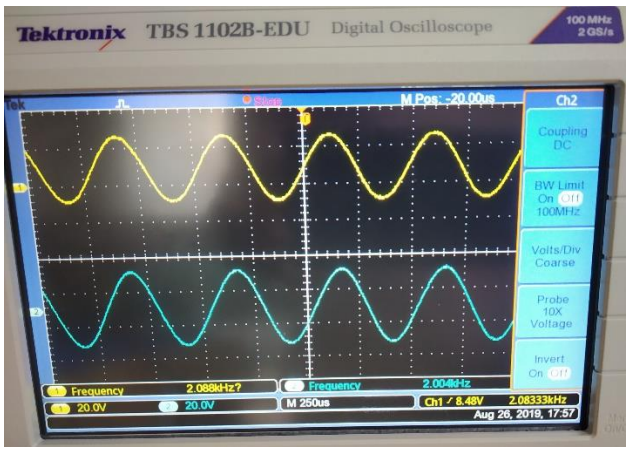


Figure 9- Demodulated signal after RC LPF and Tunable LPF
(New DSO Model No. TBS 1102B-EDU)

f) Since the PLL is expected to track the changes in the incoming signal frequency, it should be able to track if there is a difference between the nominal carrier frequency of the FM signal and locally generated carrier frequency (that is the frequency of the VCO in the PLL).

g) To check this, turn the Frequency adjustment knob of the VCO in the PLL and observe the Demodulated signal. For what values of the VCO frequencies, the demodulated signal correct? Comment on your observations.

E –Conclusions:

List out your learning's from the experiments.