1

$R_1 = 0XEF00DE12$

$R_2 = 0X456123F$

$R_5 = 4$

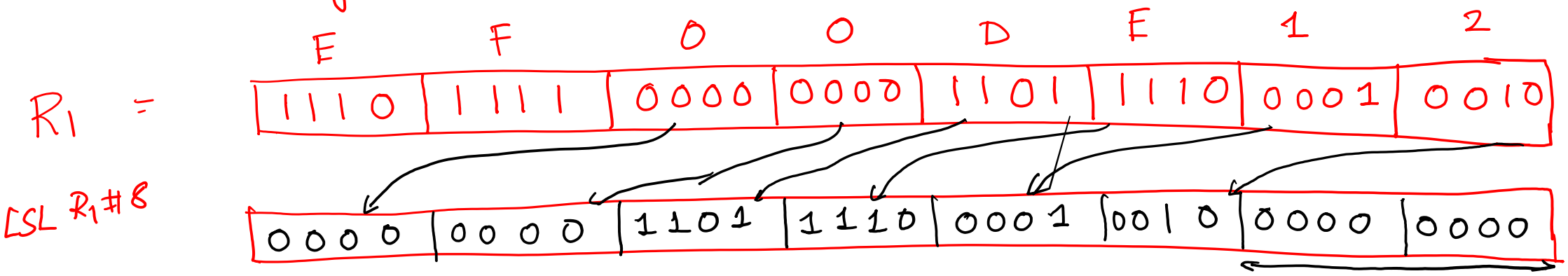
$R6 = 28$

① ROR R_2, R_6

② LSR R_2, #5 } #Class Work.

① LSL R_1, #8

Logical shift left by 8



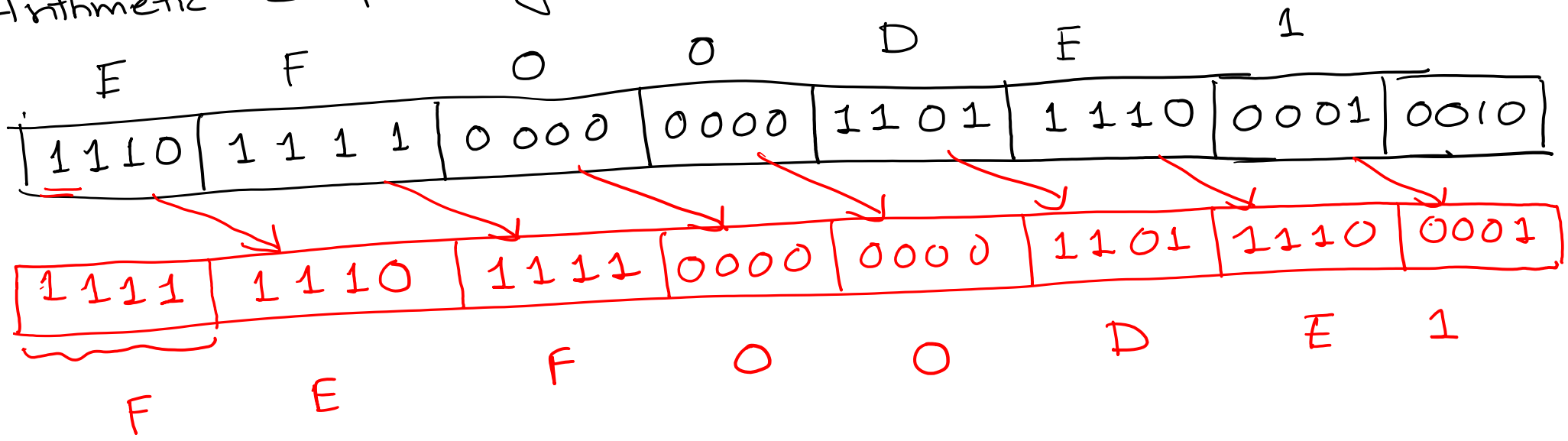
⇒ 0 0 DE1200

(2) ASR R1, R5

R1 = 0X EF 00 DE 12

R5 = 4 positive operand

ASR → Arithmetic Shift Right by 4 places



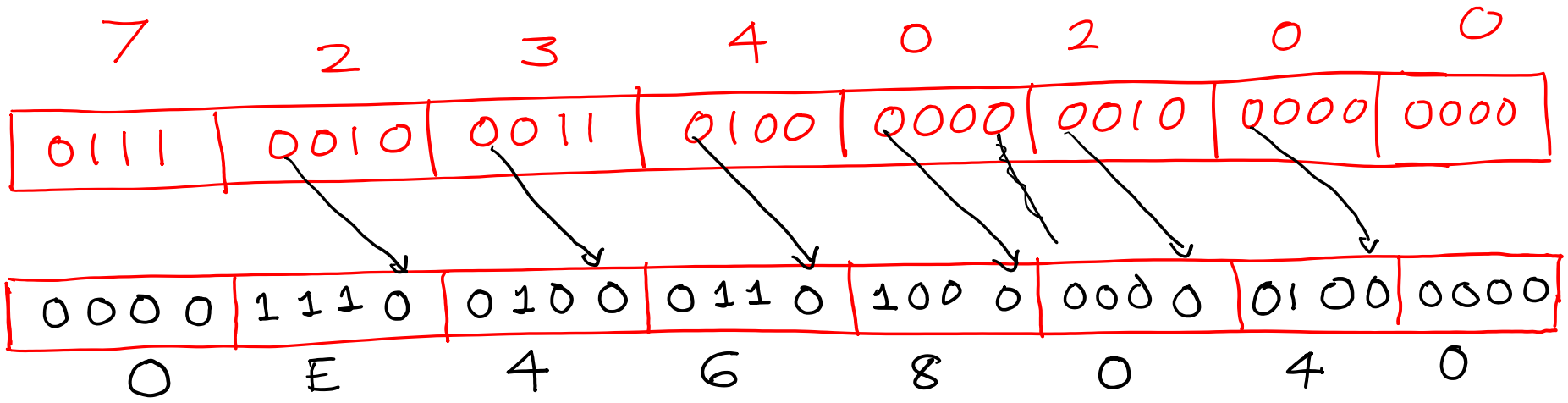
0X FEF00DE1

③ Find the content of the destination register

$R5 = 0X72340200$

$R2 = 4$

② MOV R3, R5, LSR #3
logical shift left by 3 places



$R3 = 0X0F468040$

Class Work: MOV R6, R5, ASR R2

④ WAP

R_1, R_2

if $R_1 < R_2 \longrightarrow R_{10} \leftarrow R_2$

$R_1 > R_2 \longrightarrow R_{10} \leftarrow R_1$

$R_1 = R_2 \longrightarrow R_{10} \leftarrow R_1 + R_2$

C-code

```
SUBS  R3, R1, R2
ADDEQ R10, R1, R2
MOVHI R10, R1
MOV   R10, R2
```

(5) Result ?

(a) ADD R1, R2, R2, LSL #4

$R_1 = R_2 + 2^4 \cdot R_2$

$= R_2 + 16R_2$

$R_1 = \underline{17R_2}$

(b) RSB R3, R3, R3, LSL #3

$R_3 = 2^3 R_3 - R_3$

$= 8R_3 - R_3$

$= \underline{7R_3}$

(c) SUB R0, R0, R0, LSL #2

$R_0 = R_0 - 2^2 \cdot R_0$

$= R_0 - 4R_0 = \underline{-3R_0}$

Logical Instructions

$R_3 \rightarrow$ 0x0FF00FF0

$R_4 \rightarrow$ 0x0FE0FAB8

$R_0 \rightarrow$ 0x0

① EORS R_1, R_3, R_4

② ANDS R_5, R_3, R_0

Which flags are getting affected

① XOR operation

$R_3 \rightarrow$ 0000 1111 1111 0000 0000 1111 1111 0000

$R_4 \rightarrow$ 0000 1111 1110 0000 1111 1010 1011 1000

0000 0000 0001 0000 1111 0101 0100 1000

EORS → 0 010F548

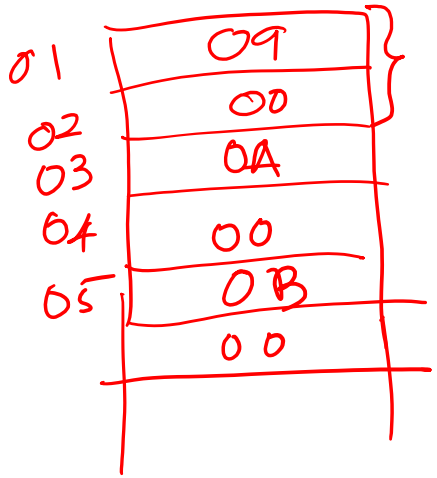
② $R_5 \rightarrow$ 0x0000 00 00

Zero flag = 1

LDR R_1, = const

LDR R_1, = 0X04

R_1 = 0X04



little Endian Rep

TABLE DCD 0X09, 0X0A : 0X0B

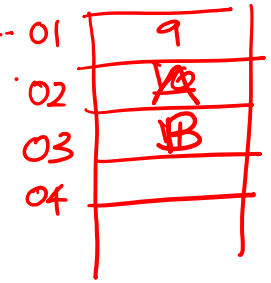
0X00 00 00 09

0X00 00 00 0A

byte

TABLE DCB 0X09, 0X0A, 0X0B

TABLE DCW 0X09 0X0A, 0X0B



0X 00 09 0X000A

TABLE DCB

DCW → HW

DCD → word