

ATLAS/CMS/LCD
RD53 collaboration:

**Pixel readout integrated
circuits for extreme rate
and radiation**

3rd LHCC status report

May 25 2016

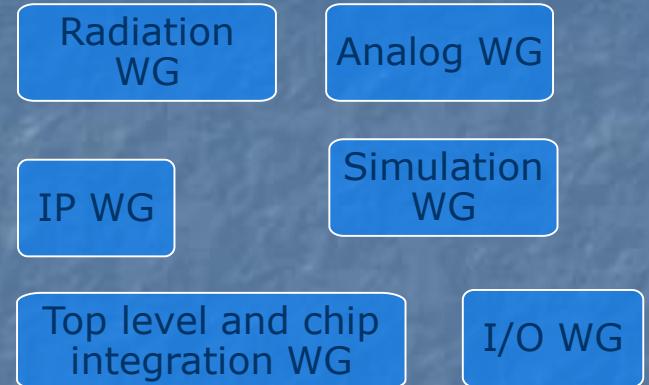
RD53 SPs: Jorgen Christiansen, CMS & Maurice Garcia-Sciveres, ATLAS
on behalf of RD53

Reminder RD53

- Focussed R&D program to develop pixel chips for ATLAS/CMS phase 2 upgrades and LCD vertex
- Extremely challenging requirements for HL-LHC:
 - Small pixels: $50 \times 50 \mu\text{m}^2$ ($25 \times 100 \mu\text{m}^2$) and larger pixels
 - Large chips: $\sim 2\text{cm} \times 2\text{cm}$ (~ 1 billion transistors)
 - Hit rates: 3 GHz/cm^2
 - Radiation: $1\text{Grad}, 2 \times 10^{16} \text{ neu/cm}^2$ over 10 years (unprecedented)
 - Trigger: $1\text{MHz}, 10\text{us}$ ($\sim 100x$ buffering and readout)
 - Low power - Low mass systems
- Baseline technology: 65nm CMOS
- Full scale demonstrator pixel chip in 2016.
- 19 collaborating institutes and many Guests
 - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, RAL, Seville, Torino, UC Santa Cruz. (PSI has withdrawn as very busy with phase 1 pixel upgrade)
 - 150 on collaboration Email list,
80 on RD53 NDA list (65nm TSMC technology access),
77 on RD53 guests list (ATLAS/CMS people involved in phase 2 pixel but not on chip design)
55 on serial power list (ATLAS/CMS people interested/working on serial powering)

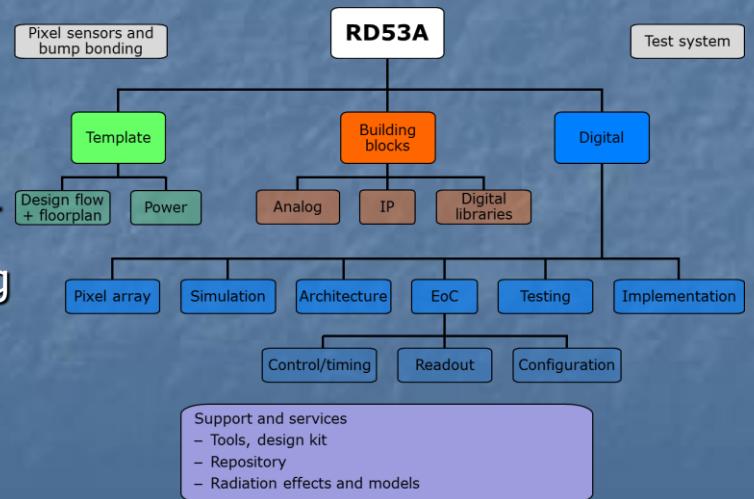
Internal organization

- Before: R&D in working groups:
 - Radiation effects and rad hard design
 - Analog: Low power/noise/area analog front-ends
 - IP blocks: ADC, DAC, PLL, Modified digital library, etc.
 - Simulation and architecture: Simulation, Optimization, Verification, ,
 - IO: IO interface



Collaboration meetings across WGs

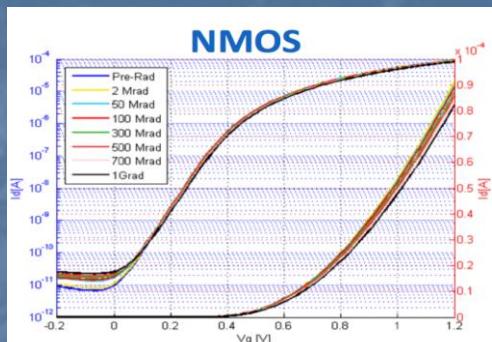
- Now (from 1/1 2016): Focussed on large scale demonstrator
 - Project structure for RD53A demonstrator
 - Bring everything together to make working large scale chip
 - Radiation WG (still a critical issue)



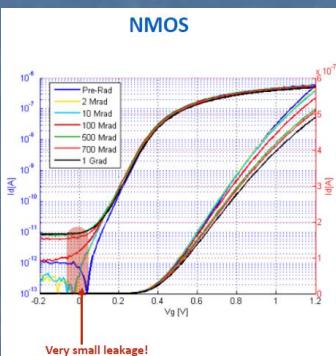
Radiation effects

- Radiation test and qualification of 65nm technology: 1Grad and $2 \cdot 10^{16}$ neu/cm²
 - Radiation tests with X-rays, Cobalt source and 3Mev protons
- Significant radiation damage above ~ 100 Mrad (only critical for pixels)
 - New radiation effects made it difficult to reach clear conclusions
- Two major “effects”
 - Radiation damage (transconductance) during radiation depends on: Device type, L, W, Bias, Temperature
 - Annealing effects depends on: Temperature, Time, Bias, Device type, L, W, Received dose
Partial recovery (transconductance) or getting worse (V_t shift)
 - (Low dose rate effect)
- Realistic to stand 500Mrad with conservative design approach
 - Cold detector: -20 - -10 °C, Not getting hotter than room temperature while powered
 - Analog: Appropriately designed (large transistors) will only have small radiation degradation
 - Confirmed with multiple RD53 prototypes
 - Digital: Suffers significant speed degradation as using small transistors
 - High density logic in pixel array will have significant (200-400%) speed degradation.
Only needs 40MHz operation frequency.
High density digital library for pixel array (small modifications of TSMC lib)
 - High speed circuits to be designed with large transistors (dedicated digital library)
 - Leakage is not a serious problem in 65nm.
 - Verification with dedicated digital radiation test chip (DRAD)
 - Inner barrel layer to be replaced after 5 years
- 200/500Mrad simulation models extensively used for circuit simulation and optimization
- Full scale pixel chip demonstrator will determine if 1Grad can be accomplished

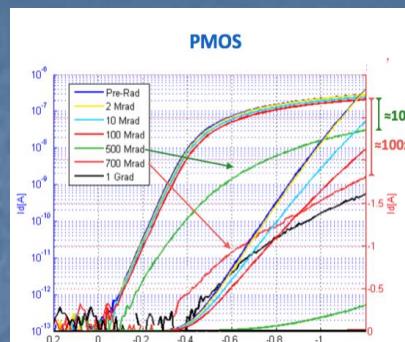
A few radiation effects plots



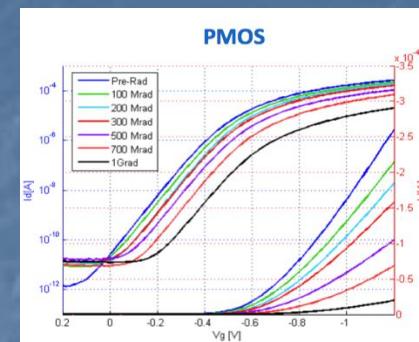
$L=1000$, $W=1000$



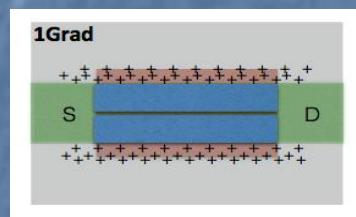
$L=1000n$, $W=120n$



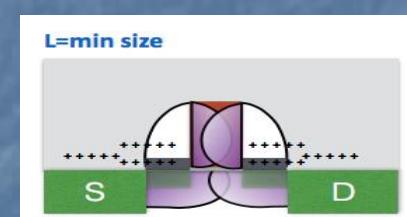
$L=1000n$, $W=120n$



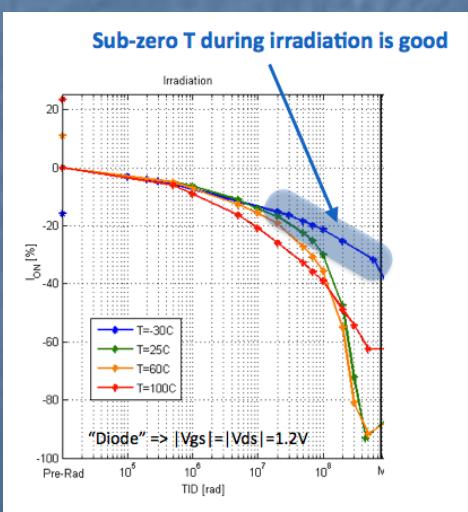
$L=60n$, $W=1000n$



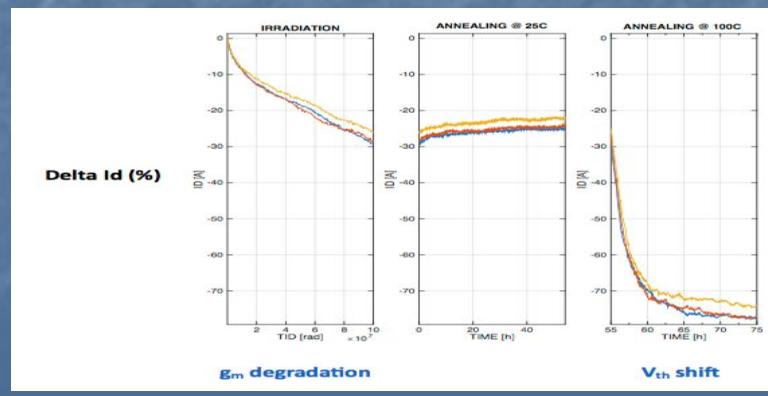
Radiation Induced Narrow Channel Effect: RINCE (known)



Radiation Induced Short Channel Effect: RISCE (new)



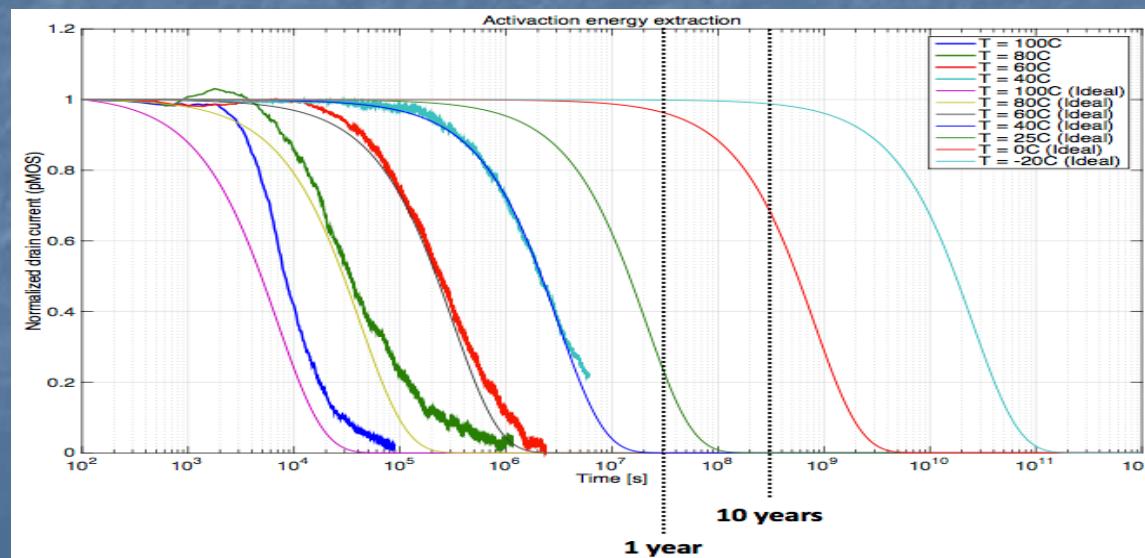
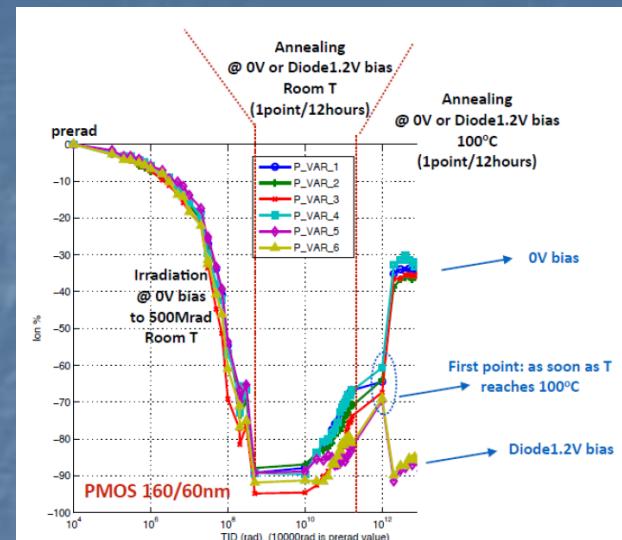
PMOS, $L=60n$, $W=600n$



Detrimental annealing effect (new)

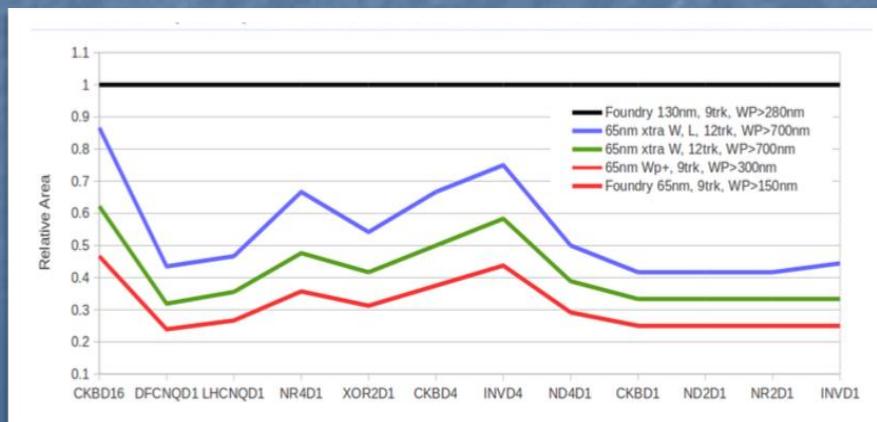
(bad) Annealing

- Significant V_t shift can develop with annealing depending on Temperature, Time, Bias, Device type, L, W, Received dose,
 - Foundry specific problem ?
- Latest's news: Indication that detrimental effect can be "avoided"/delayed by keeping cold
 - -20°C for 10years
 - Room temp for few months (if unbiased more ?)



Changing technology ?

- High density required in small pixels for hit storage during trigger latency
 - 130nm technology not sufficient density
- Other 65nm technologies will now be tested for radiation damage
 - One technology has been seen to have similar radiation damage, but most likely less detrimental annealing (but not any more available)
 - Others could be better or worse (unpredictable)
- Sub 65nm
 - Not yet radiation tested to these high levels
 - Significantly increased cost and complexity
- We would be “alone” as no other detectors needs to change technology
 - Technology access, design kit, support, radiation testing, IPs, shared runs, etc.
- RD53 stays with current 65nm technology for large scale demonstrator
 - Major design efforts invested in this
 - Appears viable for 500Mrad when taking appropriate precautions
 - If we are forced to change technology it will take ~1 year to remap design, IPs, FEs, libraries plus extensive radiation testing program will be needed.

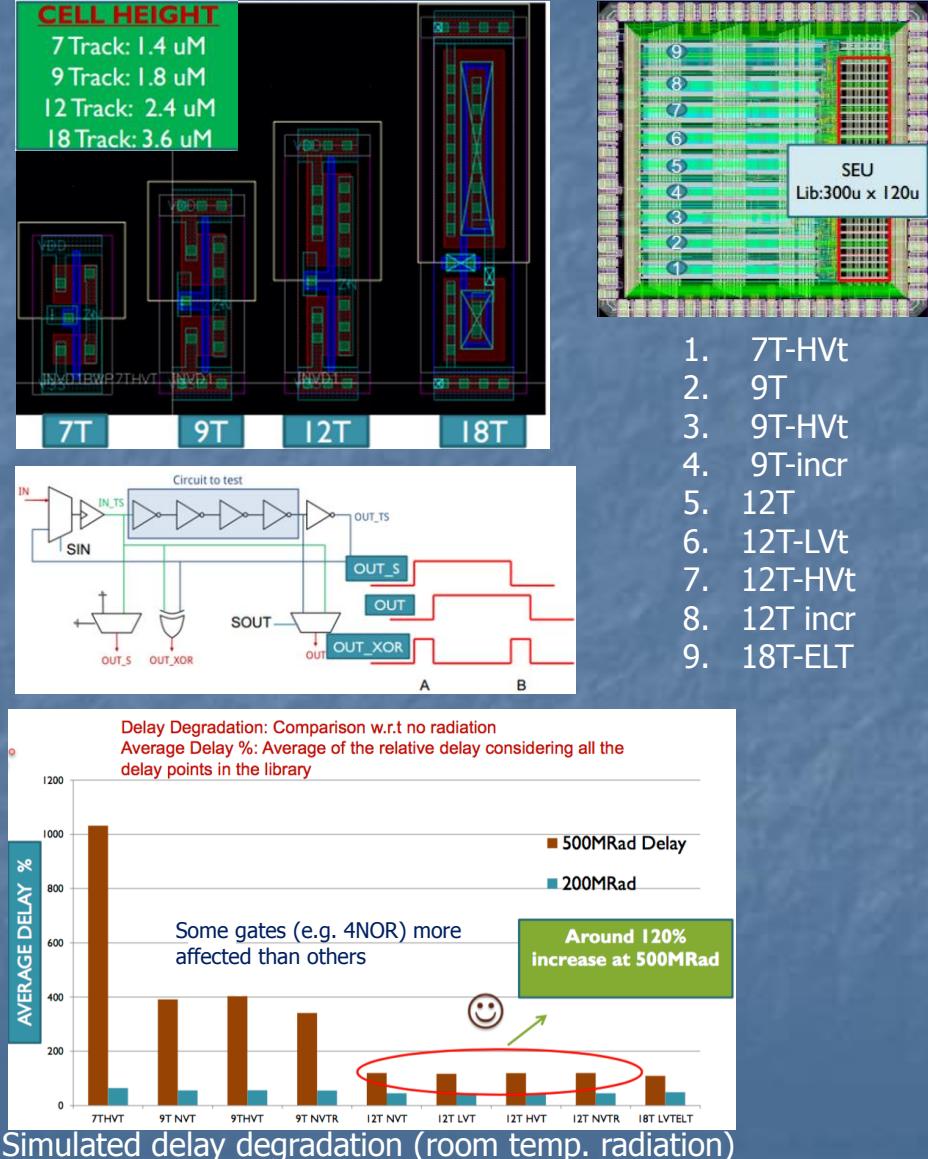


- Bad combination “avoidance”:
 - >200Mrad (inner layer),
 - Replace inner layer(s) after 5 years (5% surface)
 - Radiation at High/room temperature:
 - Pixel will run cold (-10 -20°C)
 - Small PMOS: High density digital
 - Only needs to run 40MHz
 - Analog and Fast Digital circuits:
 - Dedicated designs with large transistors
 - High/room temperature anneal
 - Pixel runs cold
 - No bias/power when not cooled

Needs to confirm that this “avoidance strategy” is sufficient and reliable

DRAD chip

- Dedicated test chip to measure delay degradation and power consumption of digital logic
 - RD53, MPA, LPGBT
- Test structures with different types of gates: NAND, NOR, buffers, flip-flop, latch
- SEU test structure
- 9 different libraries: 7-18 track
 - Small, Mid, Large transistors
 - Low V_t, normal V_t, High V_t
 - Linear, enclosed
- Submitted March. 2016
- Return: End May
- Radiation test campaign during summer

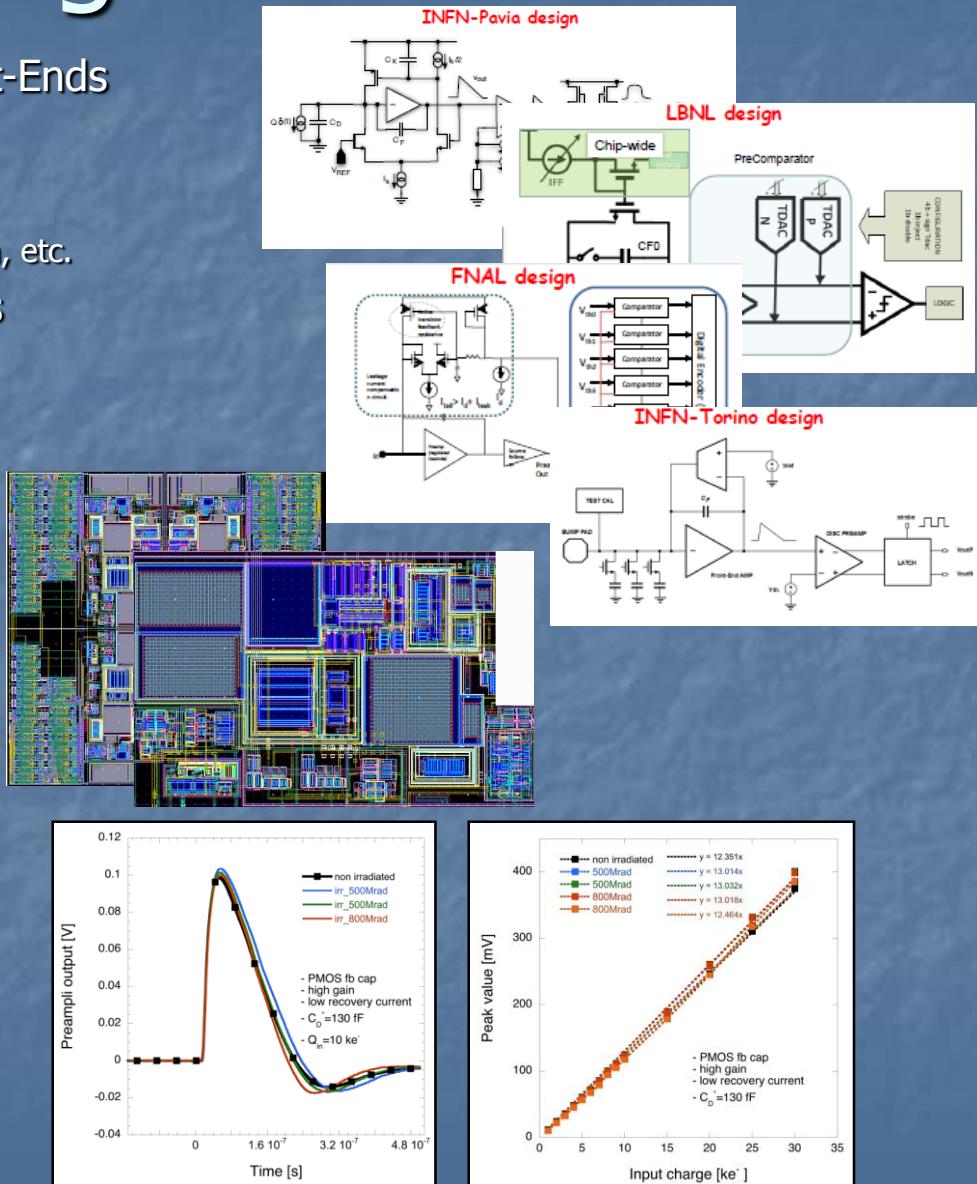


Analog FEs

- Low power/noise/area analog pixel Front-Ends
- ~50% pixel area for analog
- Analog front-end specifications defined
 - Capacitance, threshold, noise, power, dispersion, etc.
- Evaluation of alternative FE architectures
 - 3 implementations of TOT FEs
 - 2 slow (40MHz counting) TOT
 - 1 fast (200MHz counting) TOT
 - 1 Non linear fast digitizing FE
- 3 FEs prototyped and extensively tested
 - Limited radiation effects

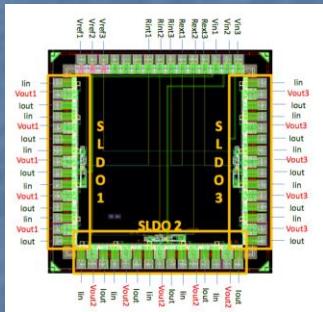
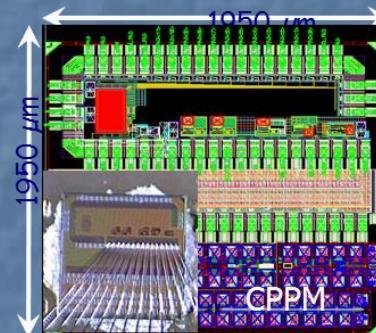
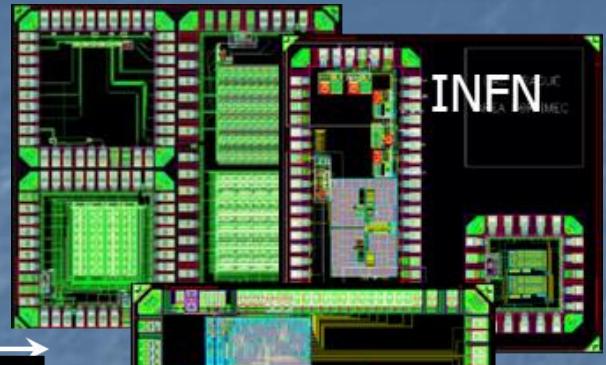
	Fresh AFE				500 Mrad corner				Ref
	TO	PV	LBL	FNL	TO	PV	LBL	FNL	
Charge sensitivity [mV/fC]	236	94	n.a.	120	n.a.	85		115	-
ENC [e rms]	60	84	50	85	80	79		92	<120
Threshold dispersion [e rms]	n.a.	35	50	35	n.a.	n.a.		n.a.	≤40
In-time overdrive ³ [e-]	150	300	500	0	150	1400		0	≤600
Current consumption [μ A/pixel]	4.4	4.0	4.0	5/8	4.4	3.4		n.a.	<5
Time-walk [ns] ⁴	9.3	13.5	20	9.1	8.5	24		9.9	<25
Time over threshold-ADC conversion time [ns] ⁵	292	360	n.a.	12.5	110 @ 10ke	371		12.5	<500
ADC resolution [bit]	5	5	n.a.	1/2					≥3
AFE area [μ m ²]	1225	1225	1190	620					≤1225

- Post layout simulations. "High gain" AFE configuration
- Detector capacitance CD=50 fF, T=27°C, TT corner
- Time walk → threshold=600 e-, Qin=1200 e-
- ToT → threshold=600 e-, Qin=30000 e-
- Preliminary results with the 500 Mrad corner for the LBL AFE show a remarkable increase in the noise



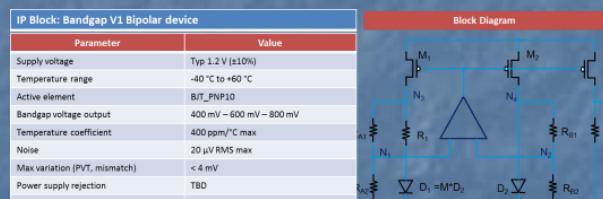
IPs

- Building blocks required to build full pixel chip
 - Large diversity of different IP blocks developed
 - ADCs, DACs, sensors (temp, current, radiation), Bandgap references, analog buffers, specialized storage cells, PLL, serializers, differential inputs/outputs, shunt-LDO, Power on reset, differential drivers/receivers, etc.
 - Specs and data sheets defined
 - IPs prototyped and tested.
- Large design effort



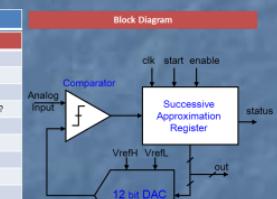
IP Block: Bandgap V1 Bipolar device

Parameter	Value
Supply voltage	Typ 1.2 V ($\pm 10\%$)
Temperature range	-40 °C to +60 °C
Active element	BJT_PNP10
Bandgap voltage output	400 mV - 600 mV - 800 mV
Temperature coefficient	400 ppm/°C max
Noise	20 μ V RMS max
Max variation (PVT, mismatch)	< 4 mV
Power supply rejection	TBD
Consumption	500 μ W (main stage)
Startup-circuit	Yes
Trimming	Yes
Max variation (1Grad, 10^{10} n/cm ²)	?
Status(end of June)	First prototype submitted
Designer (Email)	menouni@cpom.in2p3.fr; ewana@cpom.in2p3.fr;



12 bit Monitoring ADC

Parameter	Value
Supply voltage	1.2 V ($\pm 10\%$)
Temperature range	-40 °C to +60 °C
Architecture	SAR
Conversion clock Clk	312 kHz (40 MHz CLK/128) or lower ?
Resolution	12 bit
Input range	0 to 1 V (LSB = 244 μ V)
Integral Non Linearity (INL)	± 1 LSB
Differential Non Linearity (DNL)	± 0.5 LSB
Conversion time	14 clock cycle
Capacitor	MIMCAP
Power	< 1mW (depends on frequency)
Trimming	Yes
Status(end of June)	First prototype submitted
Designer (Email)	menouni@cpom.in2p3.fr; ewana@cpom.in2p3.fr;



Schedule	Status	Date
Prototype 0 submitted	Q2 2014	
Designer (Email)	Q3 2014	
First Tests and Irradiation	Q4 2014	
Re-design, Improvement	Q4 2014	
Prototype 1 submission	Q4 2014	
Prototype characterized	Q1 2015	
Prototype 2 submission	Q3 2015	
Prototype 2 characterized	Q3 2015	
Full IP available	Q4 2015	

I/O signals

Function
Input signals (Signal name)
Output signals (Signal name)
BGP
VDD
GND

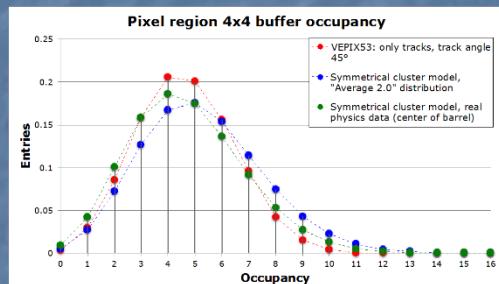
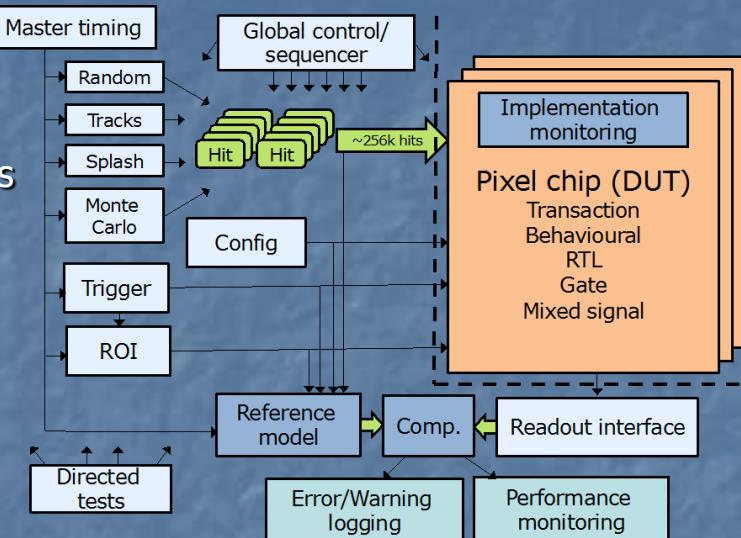
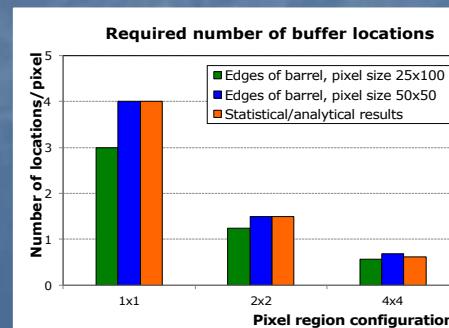
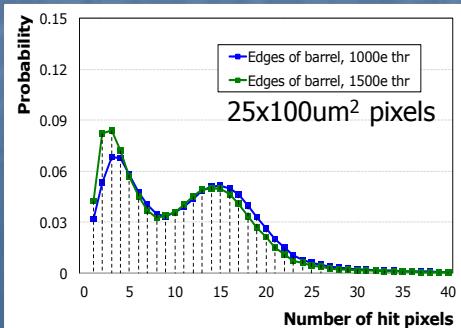
Function
Analog supply
Digital supply
Ground

Simulation/verification

- Simulation and verification framework for pixel chip
 - Based on system Verilog and UVM (industry standard for ASIC design and verification)
 - Available on repository and being used by several groups
 - Reference model
 - Basic/generic pixel chip
 - Detailed RTL/gate level implementations
 - Integration with ROOT to import hits from detector simulations and for monitoring and analysing results.
 - Simulation of alternative architectures with Monte Carlo data and/or internally generated hits
 - Performance characterization of different architectures
 - Verification of small scale prototypes
 - Power profiling under different conditions (hits, trigger)

Plans

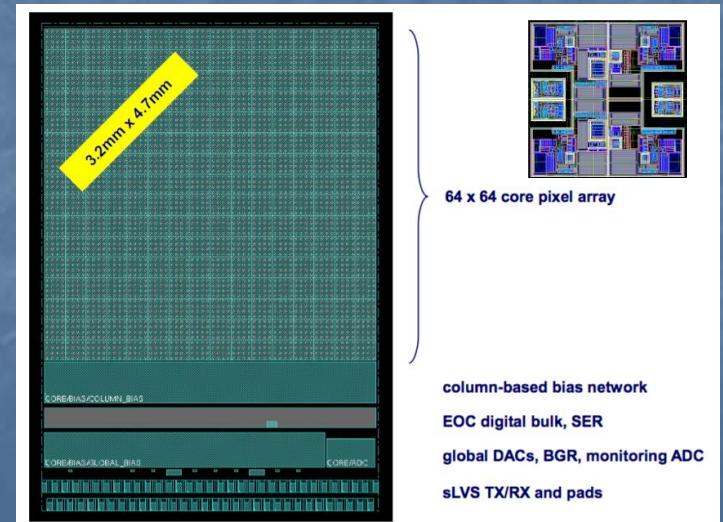
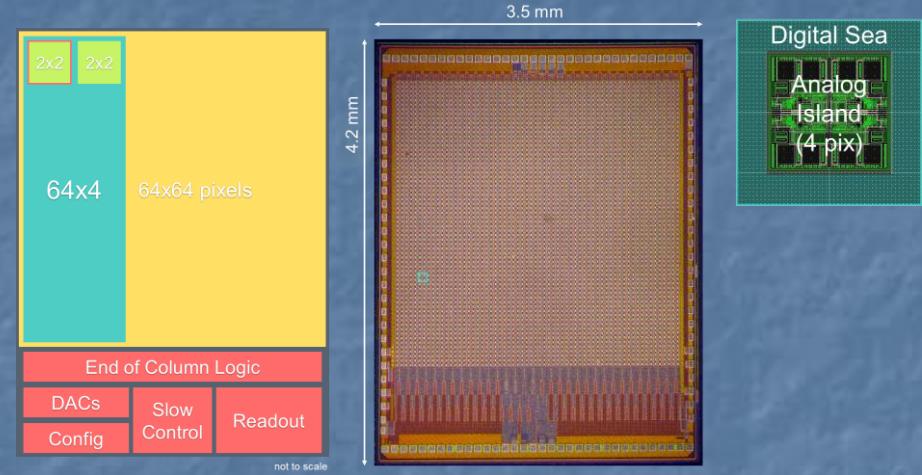
- Inclusion of SEU simulation/verification
- Detailed verification of demonstrator chip



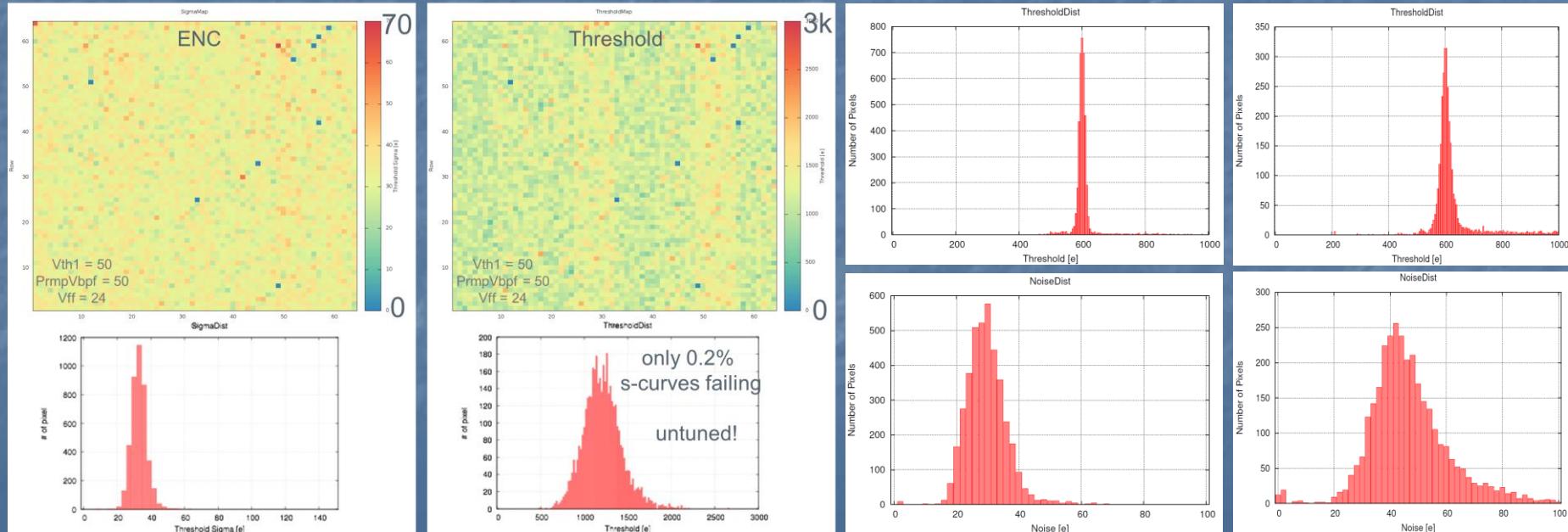
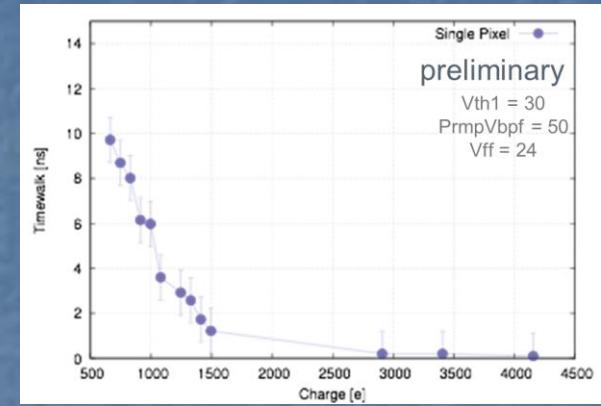
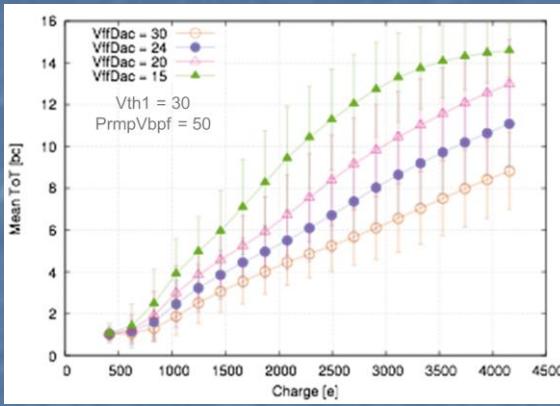
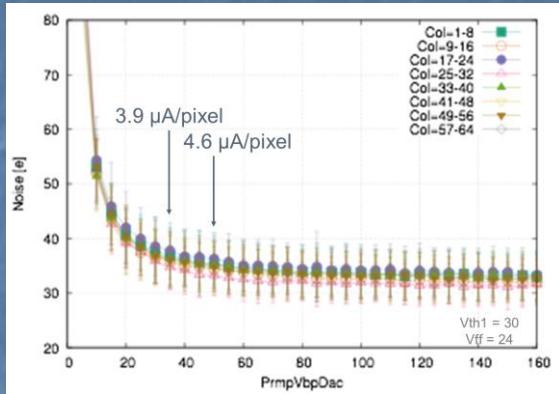
Buffer occupancy comparison between simulation and analytical statistical model

Pixel array prototypes

- FE65-P2: 64 x 64 pixels
 - 2 x 2 pixel region (evolution from FEI4)
 - Low rate readout
 - Double Analog / Digital isolation
 - 4b-ToT with slow (40MHz) FE
 - Status: Functional, Under test. Bump bonding to pixel sensor on-going.
- CHIPPIX65: 64 x 64 pixels
 - 4 x 4 Pixel Region
 - Single Analog / Digital isolation
 - 5b-ToT with slow and fast FEs
 - Includes multiple RD53 IP-blocks
 - Status: Submission June 2016
- RD53A: 400 x 400(200) pixels
 - Status: Under design



FE65-P2 test results

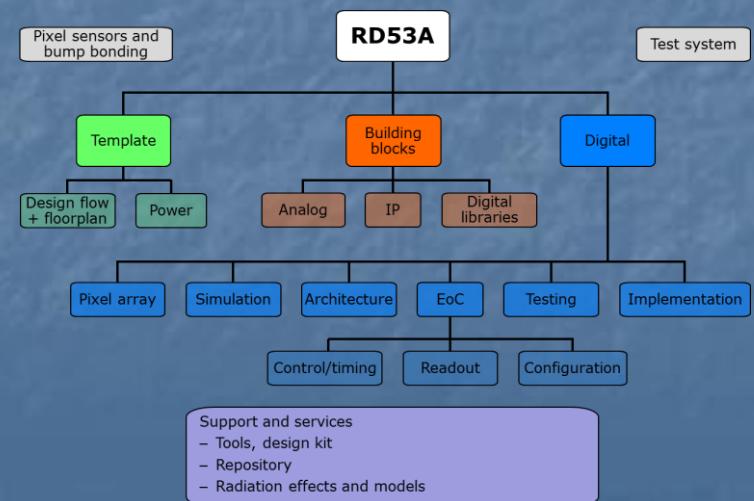
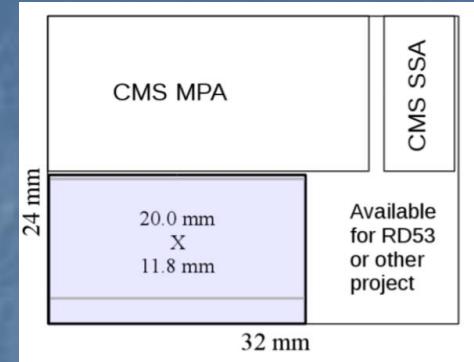


Before radiation

After 350Mrad

RD53A

- Demonstrator chip:
 - Full size chip: ~2cm x 1(2)cm), small pixels (50x50um²), Large pixels, Very high hit and trigger rates, Radiation and SEU tolerance, Effective in-time threshold: 1200e-, Low power, Serial powering, Functional in test beams, etc.
 - Specification document agreed with CMS and ATLAS phase 2 pixel communities.
 - Pixel sensors compatible with this chip being prepared in both ATLAS and CMS
 - Engineering run ~1M\$ (we better get this right !)
 - Shared run with other project(s) (CMS MPA)
 - Demonstrator will be ~1/2 size, but designed as being full size
 - Starting to collect required funds (500k\$)
- Converge all activities in RD53 and WGs on this vital goal/milestone
- Schedule:
 - Up-scaling small demonstrator: Now
 - First version of near final chip: Q3 2016
 - Final version: Q4 2016
 - (plus some months for extensive verifications)
- Core design team: ~10 and increasing
 - Weekly design meetings since the beginning of the year.
 - Regular 1-2 days getting together
 - Defined project structure and responsibilities
 - Groups: INFN, Bonn, LBNL, Marseilles, NIKHEF, CERN



RD53A project structure

Pixel sensor and bump-bonding

- Signal, charge, pixel size, etc.
- Bump pad layout
- -----

RD53A chip: Jorgen, Maurice

- Specifications
- Documentation
- General organization

Test system: TBD (Bonn, CERN, Pisa, ?)

- Requirements, specifications
- Hardware, Firmware, Software
- Chip test/characterization: wafer level, chip level, beam tests
- Radiation testing

RD53A chip integration/verification: Flavio, Deputy: Tomasz

Floorplan: Flavio, Dario

- Pixel array, Bump pad
- EOC
- Power distribution
- Bias distribution
- Analog/digital isolation
- Integration/verification

Analog FEs (3/4) with biasing: Luigi, Valerio, Ennio, Abder, IP designers

- Specification/performance
- Interface (common)
- Analog isolation
- Digital/timing model
- Abstract
- Verification of block: Function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Distribution of global analog signals
- Verification of integration

Monitoring: Francesco, Mohsine, IP designers

- Specification/performance
- Interface
- Analog isolation
- Digital/ timing model
- Abstract
- Verification of block: Function, radiation, matching, etc.
- Shared database
- Integration in design flow
- Verification of integration

Digital: Tomasz

- **Simulation Framework:** Elia, Sara, Rebecca
 - Framework
 - Hit generation/ import MC
 - Reference model / score board
 - Monitoring/verification tools
 - Generic behavioural pixel chip
 - SEU injection
- **Architecture:** Elia, Sara, Andrea, Luca,
 - Evaluation – choice: Performance, Power, Area, ,
 - Simulation/Optimization
 - Functional Verification
 - SEU immunity
- **Pixel array/pixel regions:** Sara, Andrea
 - Latency buffer
 - Core/column bus
- **Readout/control interface:** Roberto, Paris
 - Data format/protocol
 - Rate estimation / Compression
 - Implementation
- **Configuration:** Roberto, Luca, Mohsine
 - External/internal interface
 - Implementation
- **Implementation:** Dario, Luca, Andrea, Luigi, Francesco, Sara, , ,
 - Script based to “quickly” incorporate architecture/RTL changes
 - RTL - Synthesis
 - Functional verification
 - SEU verification
 - P&R
 - FE/IP Integration
 - Clock tree synthesis
 - Timing verification
 - Power verification
 - Physical verification
 - Final chip submission

Digital lib.: Dario, Sandeep, Mohsine

- Customized rad tol library
- Liberty files (function, timing, etc.) Characterized for radiation
- Custom cells (Memory, Latch, RICE)
- Integration with P&R
- Radiation tolerance
- Integration in design kit

Power: Michael, Sara, Flavio

- Shunt-LDO integration
- On-chip power distribution
- Optimization for serial powering
- System level power aspects
- Power Verification

IO PAD frame: Hans

- Wirebonding pads, ESD, SLVS, Serial readout, **Shunt-LDO**, analog test input/output

Testing/Yield optim.: Sandeep, Luca ?

- Testability
- Scan path
- BIST
- Redundancy
- Bump-bonding test/verification

Support and services:

- Tools, design kit: Wojciech, Sandeep
- Cliosoft repository: **Elia, Dario, Sandeep, Wojciech**
- Radiation effects and models: **Mohsine**

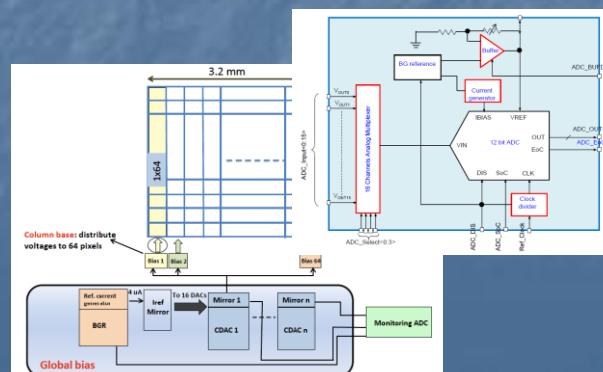
RD53A status

■ On-going:

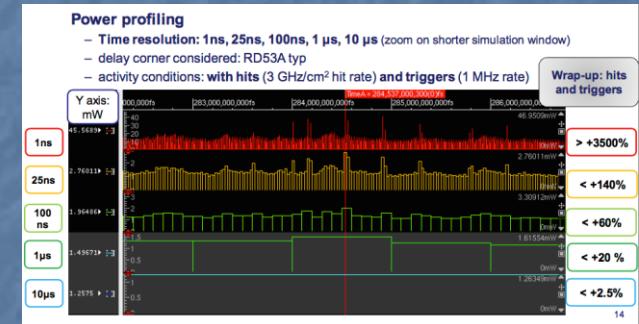
- Architecture simulations and optimization using Monte Carlo hit data from experiments.
- Global floor plan: Upscaled small demonstrator
- Shared repositories: IPs, FEs, RTL code, Simulation, full design
- Optimization of design flow & tools for very large complex design
- Integration of FEs (4) with biasing and required adaptions
- Integration of monitoring: ADC, Temp sensor, voltages, currents, etc.
- Integration of serial powering
 - Distributed power dissipation, power profiling, decoupling, system simulations
- Integration of IO pad frame
- Digital: RTL coding and technology mapping
 - Pixel array: Optimization (power, size, radiation tolerance)
 - EOC: Command decoder, chip configuration, readout data formatting, data compression
 - Synthesis and timing optimization/verification with radiation effects
 - Verification framework

■ To come:

- SEU optimisation and verification
- Final integration
- Extensive Analog and digital verification
- DRC verification
- Submission



Metrics	4x4 centralized buffer architecture*		2x2 distributed buffer architecture	
	Slow FE	Fast FE	Slow FE	Fast FE
Hit loss due to dead time (%)	2.44	0.69	0.58 – 2.67	0.33 – 0.71
Hit loss due to buffer overflow (%)	14 locations: 0.46 15 locations: 0.16 16 locations: 0.06		7 locations: 0.57 – 0.81 9 locations: 0.04 – 0.07	
Hit loss due to limited TotS (%)	0.29** (6 TotS max)			
Total loss (%)	3.19 (14 loc.) 2.89 (15 loc.) 2.79 (16 loc.)	1.44 (14 loc.) 1.14 (15 loc.) 1.04 (16 loc.)	1.38–3.24 (7 loc.) 0.65–2.71 (9 loc.)	1.15–1.43 (7 loc.) 0.40–0.77 (9 loc.)
Pixel region area*** (digital, post synthesis, pre-P&R) ($\mu\text{m}^2/\text{pixel}$)	664 (14 loc.) 728 (16 loc.)	761 (14 loc.) 786 (16 loc.)	1039 (7 loc.) (TBC) 1165 (9 loc.) (EST)	n.a.
Power consumption (average, post-P&R) ($\mu\text{W}/\text{pixel}$)			coming soon	4.832 (typical) 6.203 (worst)



400x400 pixels power	Typ	Worst
Analog array	0.96W	1.6W
Digital array	0.77W	0.99W
EOC	0.2W	0.3W
IO	0.2W	0.3W
Shunt-LDO	0.5W (25%)	1W (30%)
Total	~3W	~4W

Summary

- Many groups and people working on a focussed R&D effort to implement very high rate pixel chip for extreme radiation
- Large number of circuits, building blocks and small pixel arrays have been successfully prototyped and tested in 65nm technology.
- Improved understanding of the initially “mysterious” radiation effects seen at extreme radiation levels above 100Mrad
 - Many circuits and devices radiation tested
 - 500Mrad appears as realistic goal
 - Test of full pixel chip will determine if 1Grad is feasible when cold
- Focussed on submitting full scale demonstrator chip
 - Building blocks available and tested
 - Extensive experience gained with small pixel array prototypes
 - Defined design team with weekly meetings
 - Submission: ~End 2016

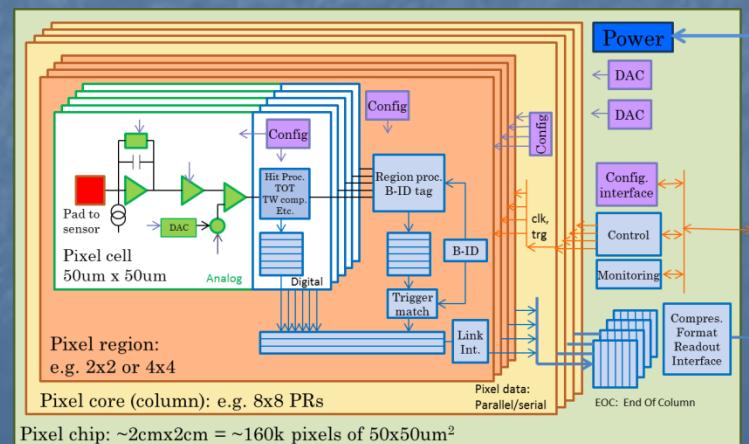
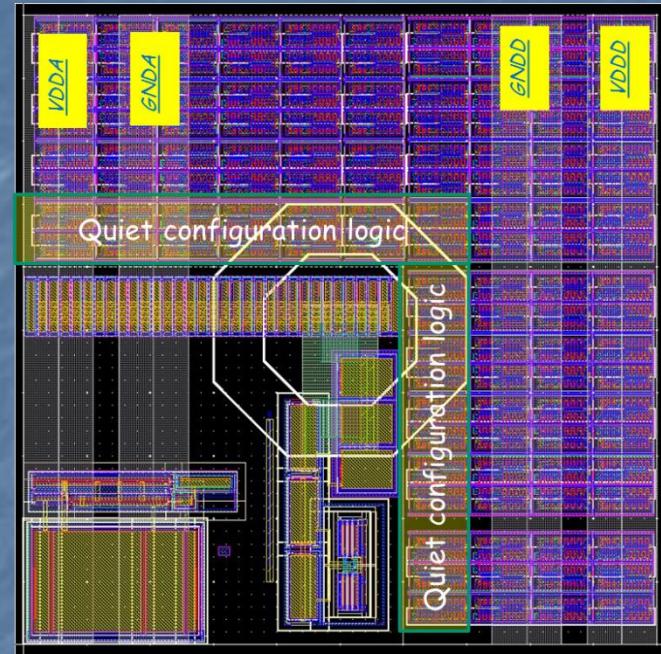
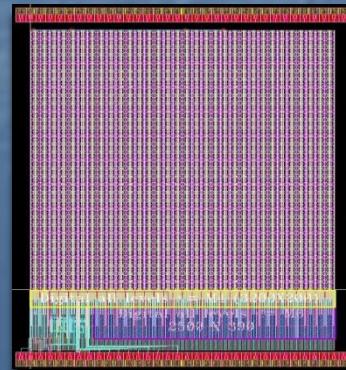
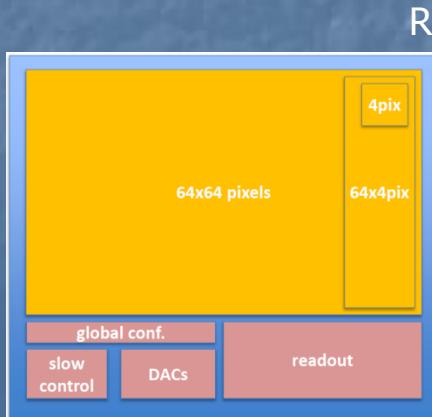
Backup slides

More information

- RD53 collaboration meetings:
<https://indico.cern.ch/category/5036/>
- ACES: <https://indico.cern.ch/event/468486>
 - RD53 + ATLAS and CMS phase 2 pixel upgrades
- Radiation seminar:
<https://indico.cern.ch/event/442426/>
- Conferences/workshops
- Coming conferences/workshops
 - Pixel, Vertex, TWEPP, IWORD, FE workshop

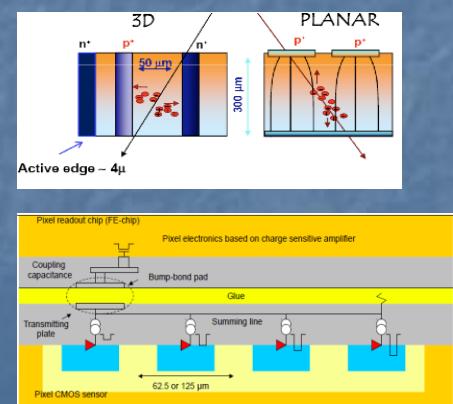
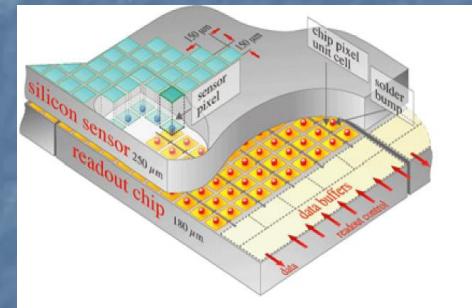
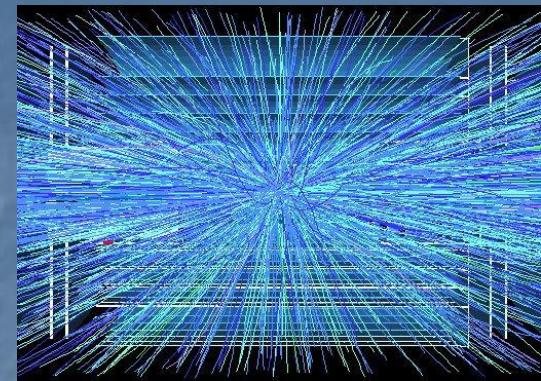
Top level WG

- Architecture and floor-plan for large pixel chip
 - Digital sea with analog islands floorplan
 - Distribution of power and global signals
 - Analog – Digital isolation
 - Digital “on-top” design flow
 - Pixels – Pixel regions – Pixel cores – End of column
 - Implementation of small 64x64 pixel demonstrator in 65nm (submission end of this month)
 - Re-optimized “FEI4” for small pixels, higher hit and trigger rates.
- Plans
 - Refinement of pixel chip (digital) architecture
 - Using simulation framework
 - Integration of full pixel chip demonstrator



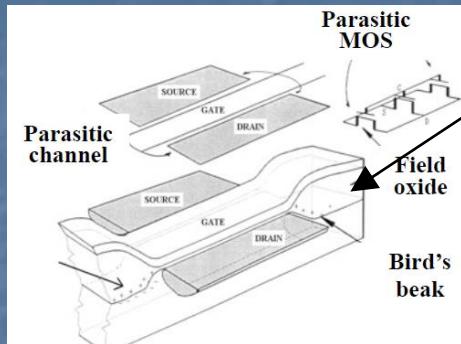
Phase 2 pixel challenges

- ATLAS and CMS phase 2 pixel upgrades very challenging
 - Very high particle rates: $500\text{MHz}/\text{cm}^2$
 - Hit rates: $2\text{-}3\text{ GHz}/\text{cm}^2$ (factor 16 higher than current pixel detectors)
 - Smaller pixels: $\frac{1}{4}$ - $\frac{1}{2}$ ($25\text{ - }50\text{ }\mu\text{m} \times 100\mu\text{m}$)
 - Increased resolution
 - Improved two track separation (jets)
 - Participation in first/second level trigger ?
 - A. 40MHz extracted clusters (outer layers) ?
 - B. Region of interest readout for second level trigger ?
 - Increased readout rates: $100\text{kHz} \rightarrow 1\text{MHz}$
 - Low mass \rightarrow Low power
- Very similar requirements (and uncertainties) for ATLAS & CMS
- Unprecedented hostile radiation: 1Grad , $2 \cdot 10^{16} \text{ Neu}/\text{cm}^2$
 - Hybrid pixel detector with separate readout chip and sensor.
 - Phase2 pixel will get in 1 year what we now get in 10 years
- Pixel sensor(s) not yet determined
 - Planar, 3D, Diamond, HV CMOS, , ,
 - Possibility of using different sensors in different layers
 - Final sensor decision may come relatively late.
- Very complex, high rate and radiation hard pixel readout chips required



ATLAS HVCmos program

Radiation effects

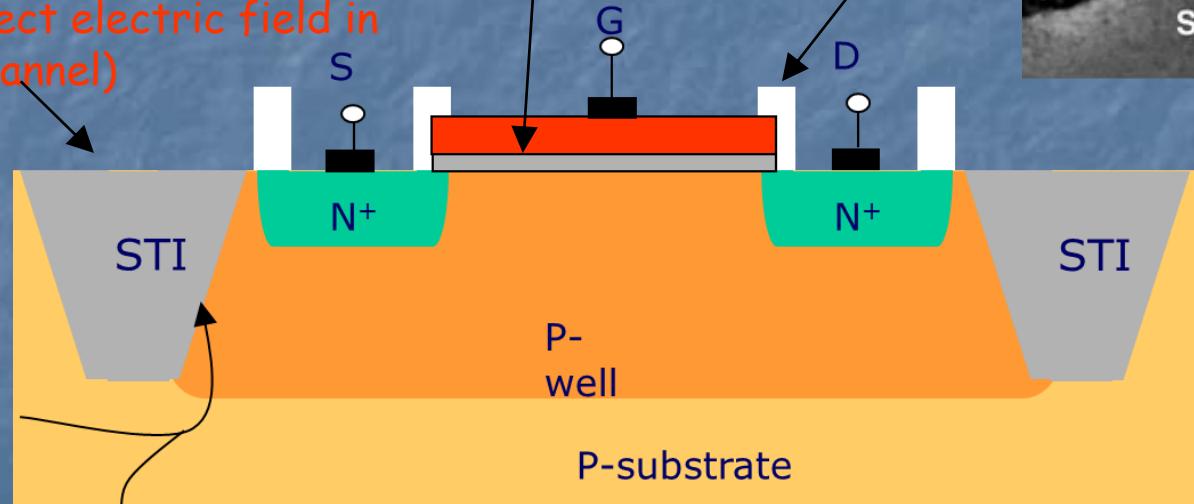


Birds beak parasitic device

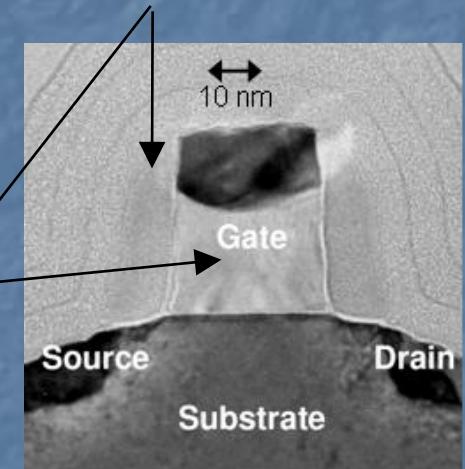
Spacer dielectrics may be radiation-sensitive

Thick Shallow Trench Isolation Oxide (~ 300 nm); radiation-induced charge-buildup may turn on lateral parasitic transistors and affect electric field in the channel)

Doping profile along STI sidewall is critical; doping increases with CMOS scaling, decreases in I/O devices



Charge buildup in gate oxide and interface states affects V_t



Increasing sidewall doping makes a device less sensitive to radiation (more difficult to form parasitic leakage paths)

Pixel chip generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2
Pixel size	100x150um ² (CMS) 50x400um ² (ATLAS)	100x150um ² (CMS) 50x250um ² (ATLAS)	25x100um ² ?
Sensor	2D, ~300um	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, MAPS ?
Chip size	7.5x10.5mm ² (ATLAS) 8x10mm ² (CMS)	20x20mm ² (ATLAS) 8x10mm ² (CMS)	> 20 x 20mm²
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	~1G
Hit rate	100MHz/cm²	400MHz/cm²	2(3) GHz/cm²
Hit memory per chip	0.1Mb	1Mb	~16Mb
Trigger rate	100kHz	100KHz	200kHz - 1MHz
Trigger latency	2.5us (ATLAS) 3.2us (CMS)	2.5us (ATLAS) 3.2us (CMS)	6 - 20us
Readout rate	40Mb/s	320Mb/s	1-4Gb/s
Radiation	100Mrad	200Mrad	1Grad
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	65nm
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	Digital
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	Pixel
Power	~1/4 W/cm ²	~1/4 W/cm ²	1/2 - 1 W/cm²

Working groups

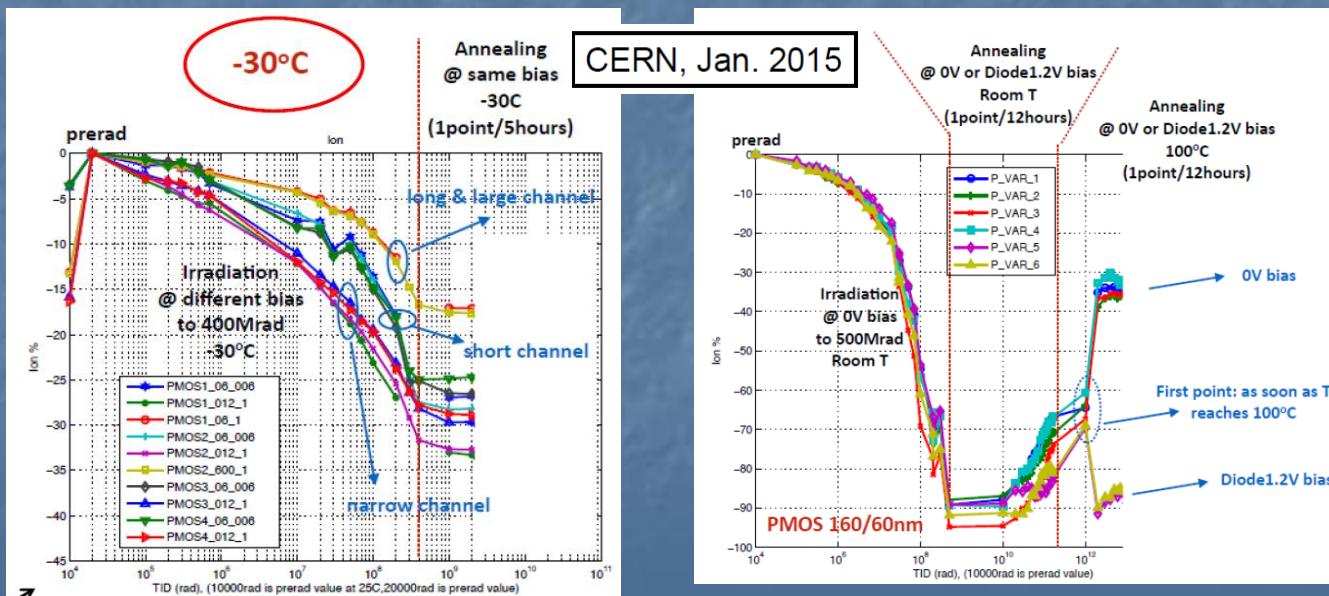
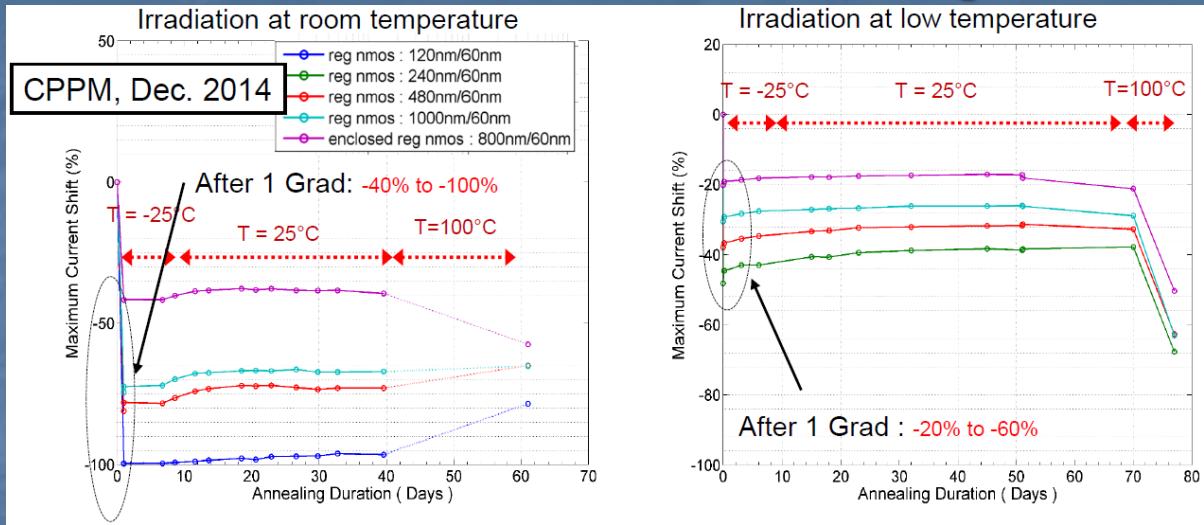
WG	Domain
WG1	Radiation test/qualification Coordinate test and qualification of 65nm for 1Grad TID and 10^{16} neu/cm ² Radiation tests and reports. Transistor simulation models after radiation degradation Expertise on radiation effects in 65nm
WG2	Top level Design Methodology/tools for large complex pixel chip Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization.
WG3	Simulation/verification framework System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells
WG4	I/O + (Standard cell) Development of rad hard IO cells (and standard cells if required) Standardized interfaces: Control, Readout, etc.
WG5	Analog design / analog front-end Define detailed requirements to analog front-end and digitization Evaluate different analog design approaches for very high radiation environment. Develop analog front-ends
WG6	IP blocks Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, , Distribute design work among institutes Implementation, test, verification, documentation

RD53 collaboration

- 20 Institutes (Seville has joined)
 - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, PSI, RAL, Seville, Torino, UC Santa Cruz.
 - 140 on collaboration Email list
 - ~70 actively contributing
 - 2015 FTE: ~23
 - 50 on RD53 guests email list
 - Spokes persons: Maurice Garcia-Sciveres, LBNL (ATLAS), Jorgen Christiansen, CERN (CMS)
 - IB chair: Lino Demaria, Torino
 - WG conveners: Marlon Barbero, Roberto Beccherle, Jorgen Christiansen, Maurice Garcia-Sciveres, Tomasz Hemperek, Valerio Re
 - 2 year terms coming up to renewal within 3 months
- MOU defined and signed (few exceptions)
- RD53 collaboration meetings: 2 times per year
- RD53 management meetings: Monthly
- WG meetings: Monthly – bi-monthly

Activity	FTE 2015
Radiation	4
Analog	3
IP	7
Simulation	3
Top	3
IO	1
Organization	2
Total	~23

Radiation effects (PMOS)



Requires an extended seminar to explain all this

power

400x400 pixels power	Typ	Worst
Analog array	0.96W	1.6W
Digital array	0.77W	0.99W
EOC	0.2W	0.3W
IO	0.2W	0.3W
Shunt-LDO	0.5W (25%)	1W (30%)
Total	~3W	~4W