Digital Logic Families

Digital Logic Families

- ICs are also classified based on their specific circuit technology, known as ***digital logic family***.
- Each family has its own basic electronic components (NAND, NOR, and NOT gates), used to build complex digital circuits.
- Various digital logic families have been introduced and used over the years.

Digital Logic Families (in chronological order)

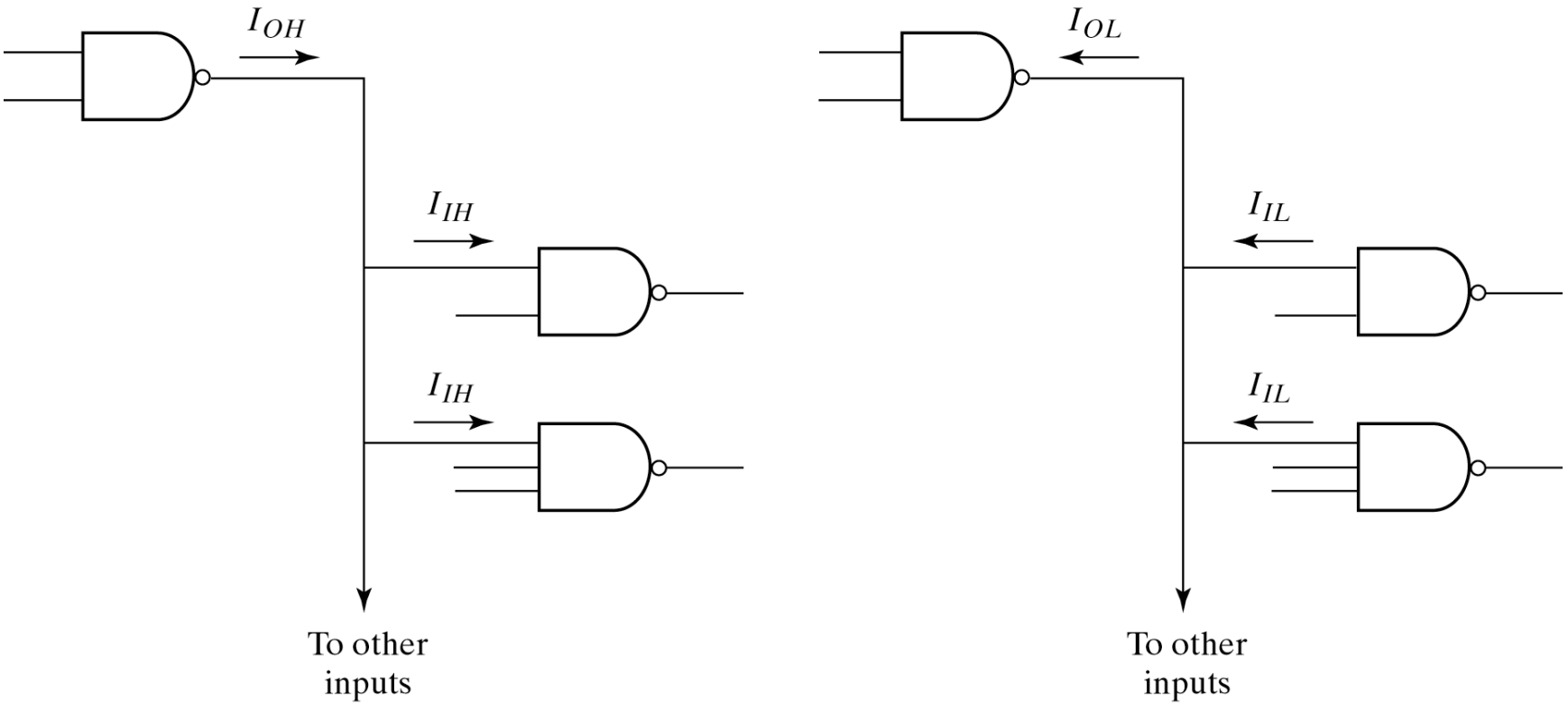
- RTL: Resistor-Transistor Logic
- DTL: Diode-Transistor Logic

earliest, now obsolete

- TTL: Transistor-Transistor Logic → widely used
- ECL: Emitter-coupled Logic → high-speed operation
- MOS: Metal-Oxide Semiconductor → compact
- CMOS: Complementary MOS
  - Low power dissipation, currently the MOST DOMINANT
- BiCMOS: Bipolar CMOS
  - CMOS and TTL for additional current/speed
- GaAs: Gallium-Arsenide → very high-speed operation

Defining Characteristics of Digital Logic Families

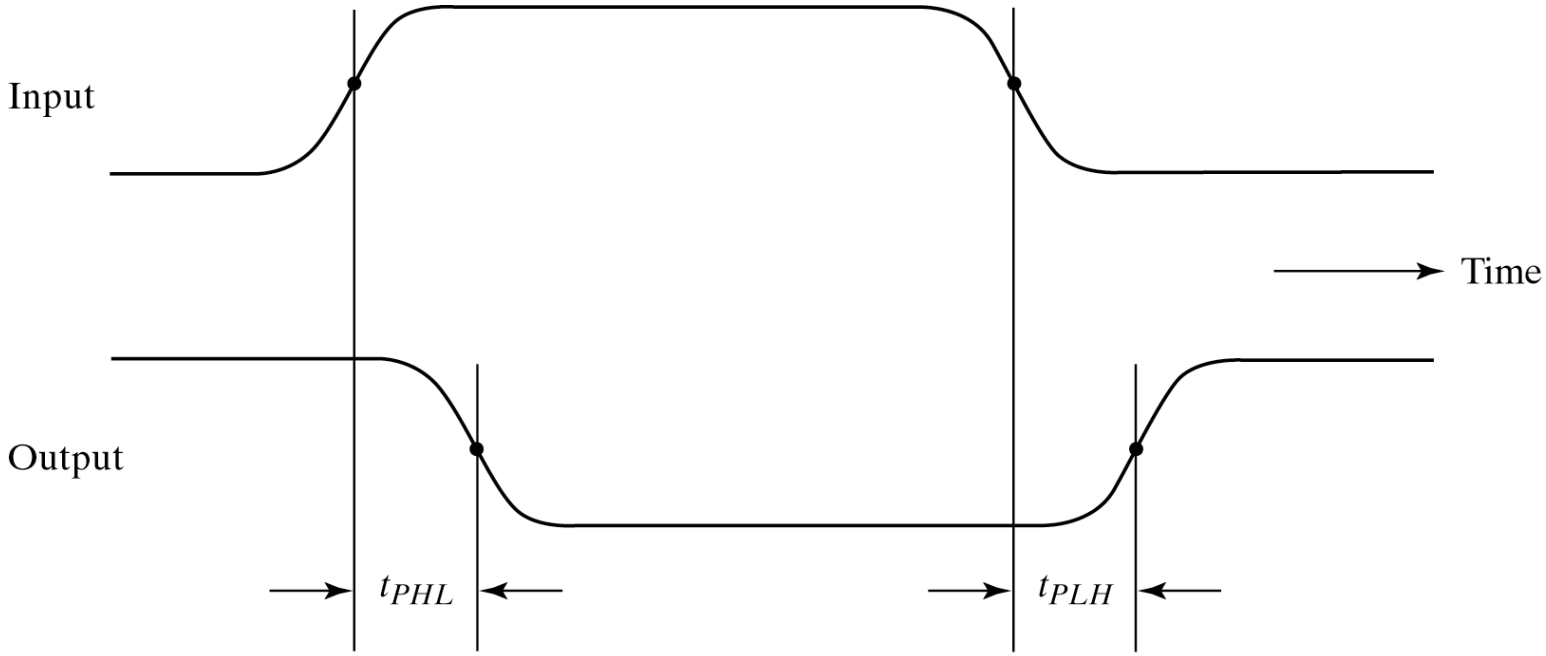
- ***Fan-in:*** # of gate inputs.
- ***Fan-out:*** # of standard loads a gate's output can drive.
- ***Noise margin:*** max external noise tolerated.
- ***Power dissipation:*** power consumed by the gate (dissipated as heat).
- ***Propagation delay:*** time required for an input signal change to be observed at an output line.



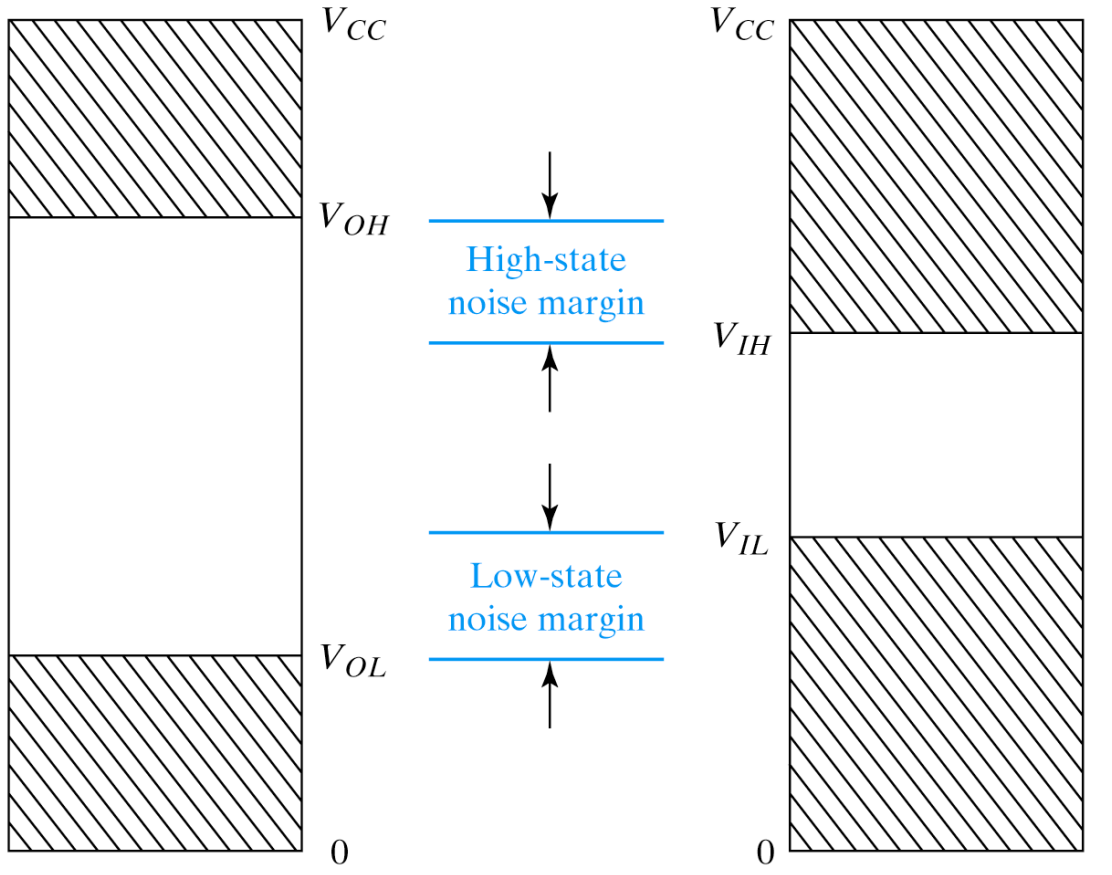
(a) High-level output

(b)Low-level output

Fan-Out Computation



Measurement of Propagation Delay



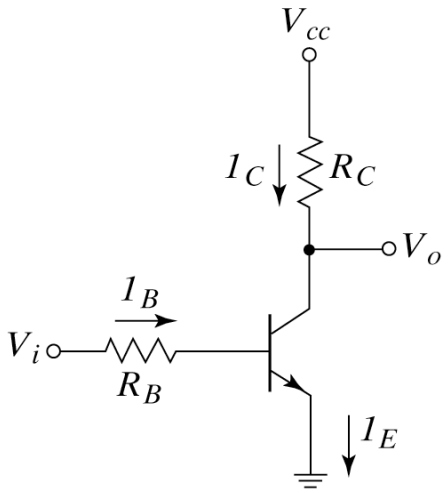
(a) Output voltage range (b) Input voltage range

Signals for Evaluating Noise Margin

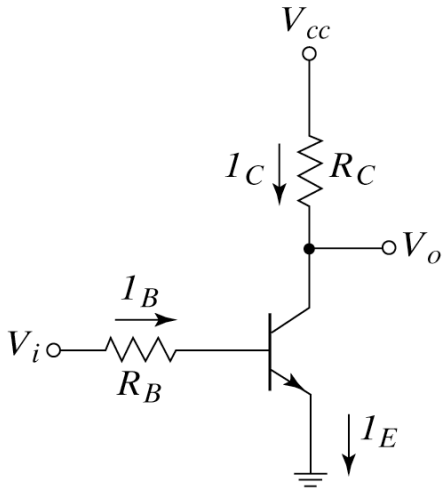
Power Dissipation (P_D)

- **Expressed in Milliwatts**
- **PD= V_{CC} * I_{CC}**
- **I_{CC}(avg)=(I_{CCH}+I_{CCL})/2**

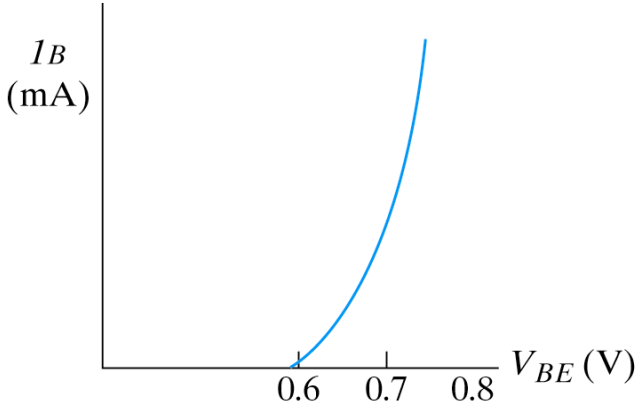
TTL LOGIC FAMILY



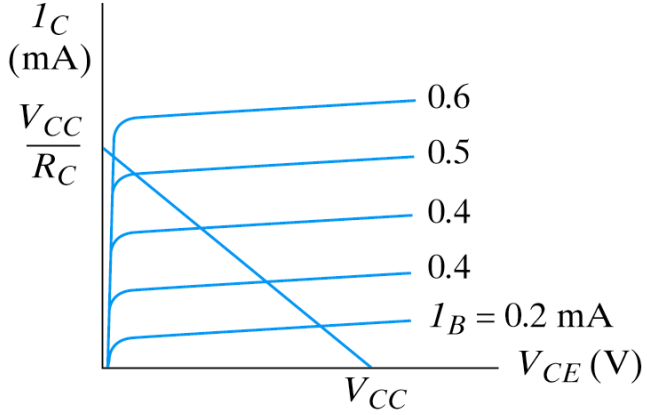
(a) Inverter circuit



(a) Inverter circuit

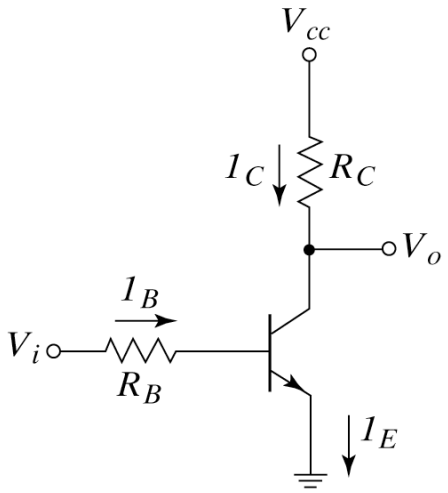


(b) Transistor-base characteristic



(c) Transistor-collector characteristic

Silicon *npn* Transistor Characteristics



(a) Inverter circuit

RC = 1kΩ, RB = 22kΩ, β= 50

VCC = 5V, find Vo for

Vi = 0.2V and Vi = 5V

BJT Characteristics

- **Base-Emitter voltage less than 0.6V ; $I_B = 0$: Cut-Off region**
- **Base-Emitter voltage more than 0.6V, transistor starts conducting - active region**
  $I_C = \beta I_B$
- **Maximum collector current $I_C = V_{CC}/R_C$**

- **In the cut-off region $V_{BE} < 0.6V$, V_{CE} – open circuit, I_C, I_B negligible**

- **In the active region V_{BE} about 0.7 V_{CE} wide range and $I_C = \beta I_B$**

- **In the saturation region V_{BE} hardly changes, $V_{CE} = 0.2V$**

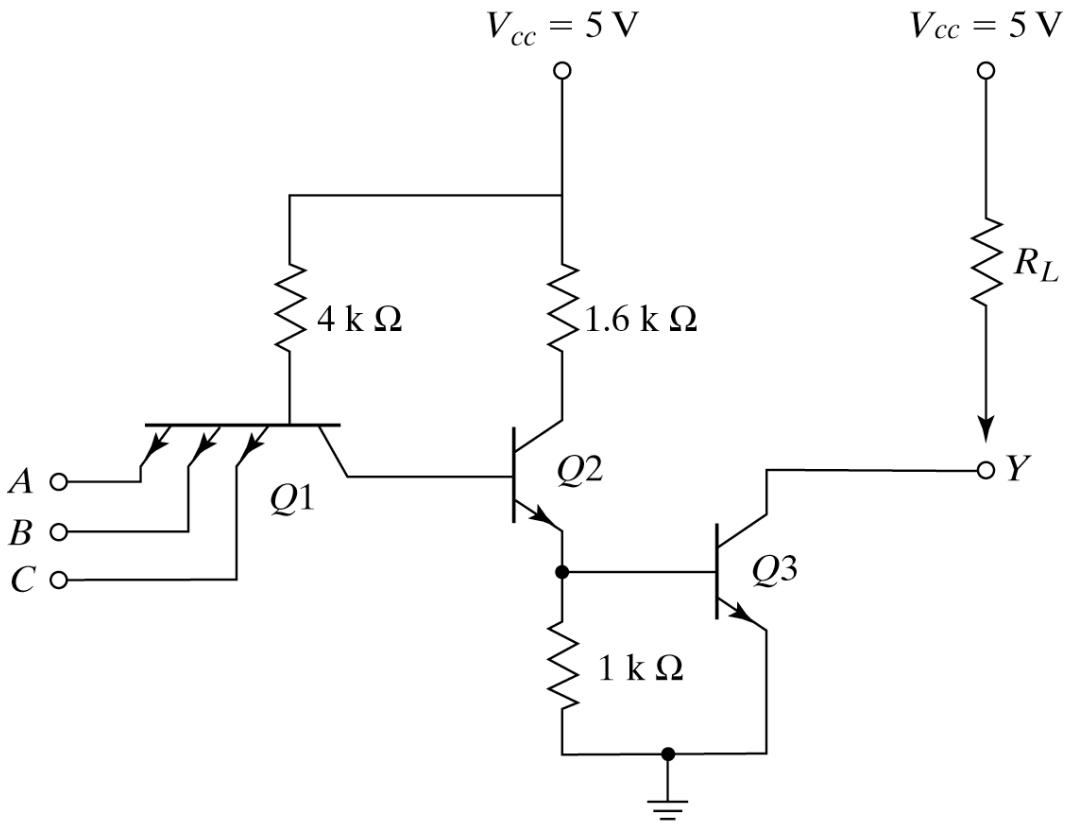
TTL Series name	Prefix
Standard	74
Low-power	74L
High-speed	74H
Schottky	74S
Low-power Schottky	74LS
Advanced Schottky	74AS
Advanced Low power- Schottky	74ALS
Fast	74F

Three Types of TTL gates

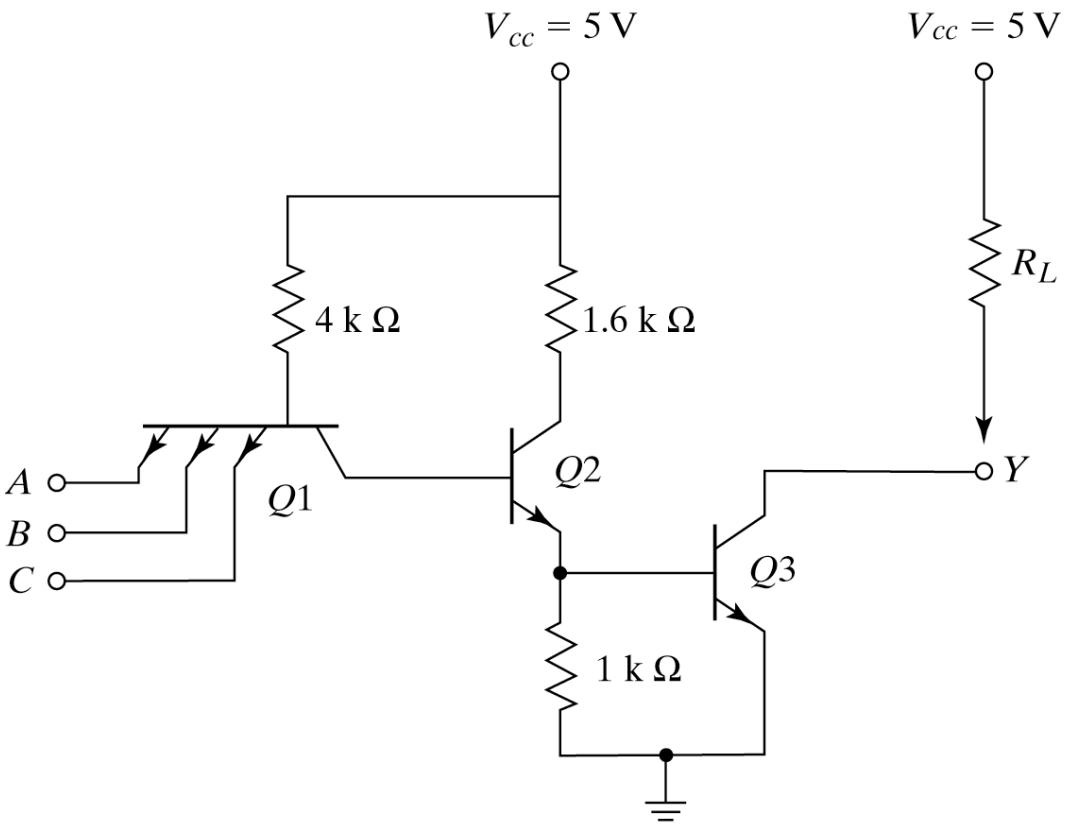
- Open - collector output

- Totem- pole output

- Three- state output

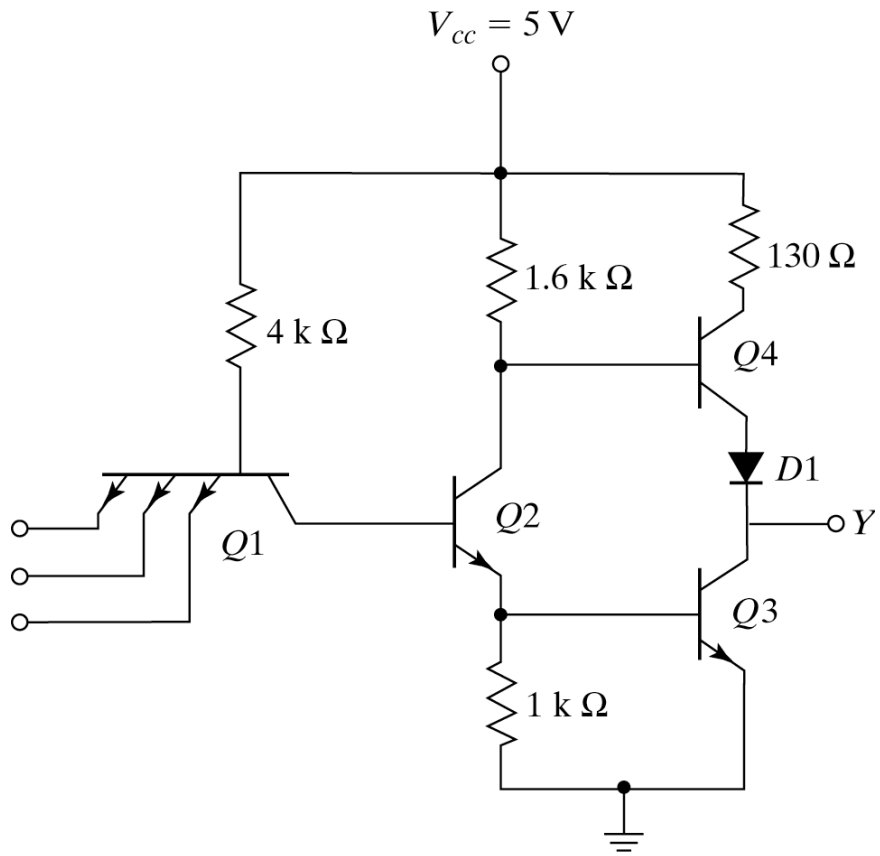


Open-Collector TTL Gate



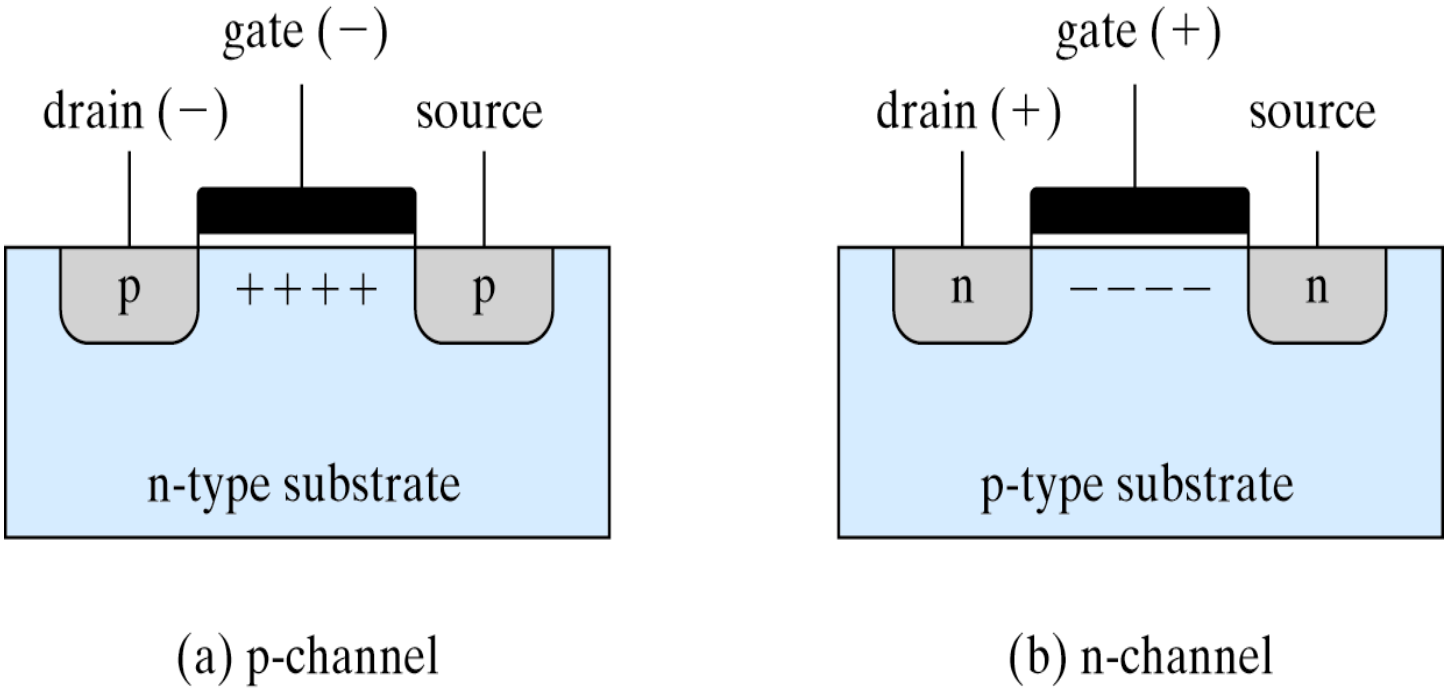
Open-Collector TTL Gate

- **Output impedance of a gate is resistive plus Capacitive load**
- **For output low to high transition C charges exponentially through RC**
- **R is R_L (external) in open collector**
- **With active pull-up delay can be reduced**



TTL Gate with Totem-Pole Output

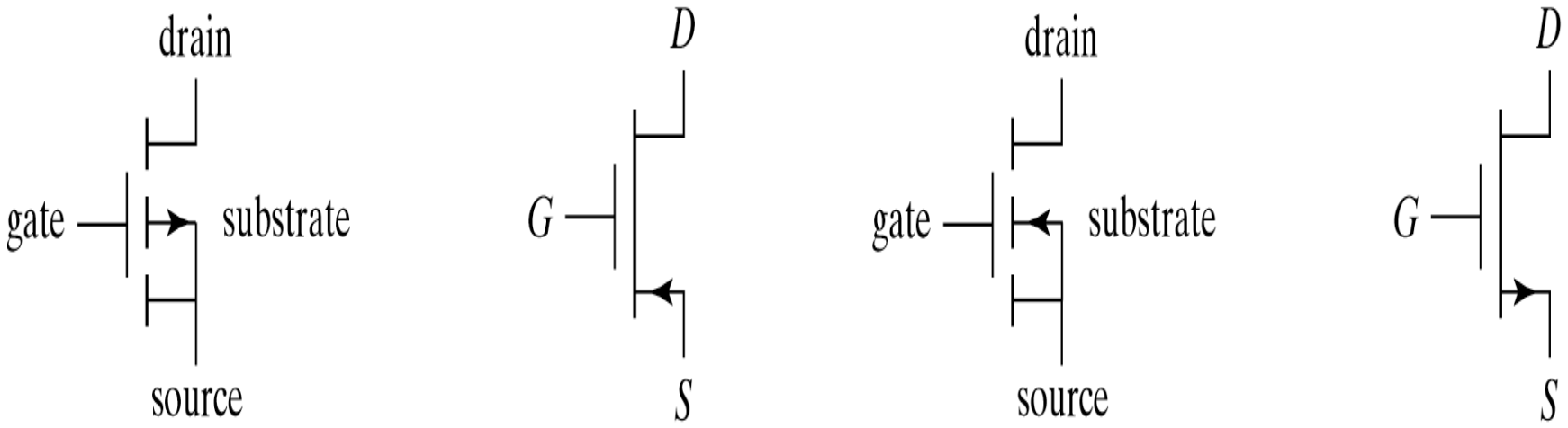
MOS Transistor



(a) p-channel

(b) n-channel

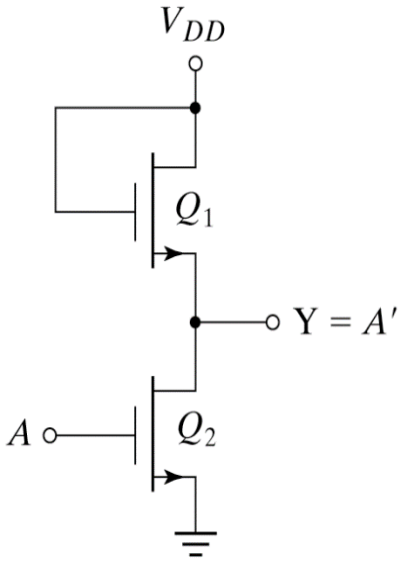
Basic Structure of MOS Transistor



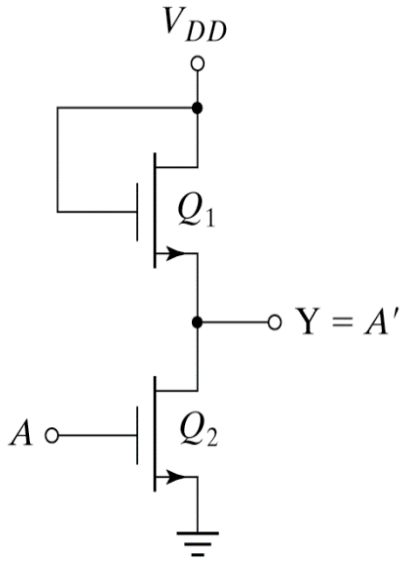
(a) p-channel

(b) n-channel

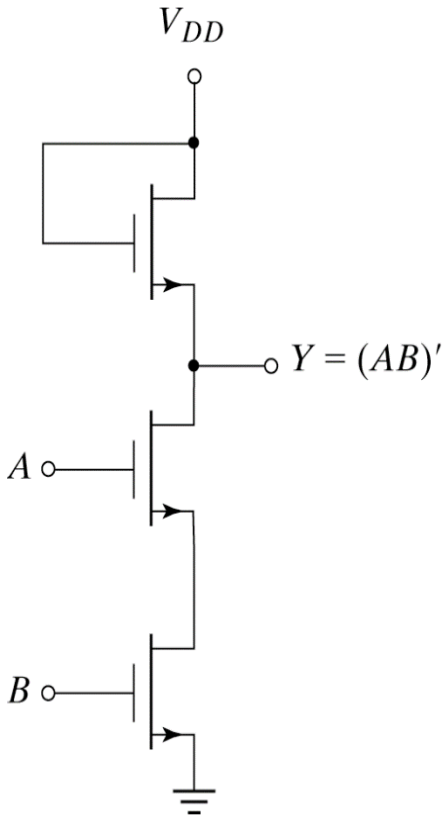
Symbols for MOS Transistors



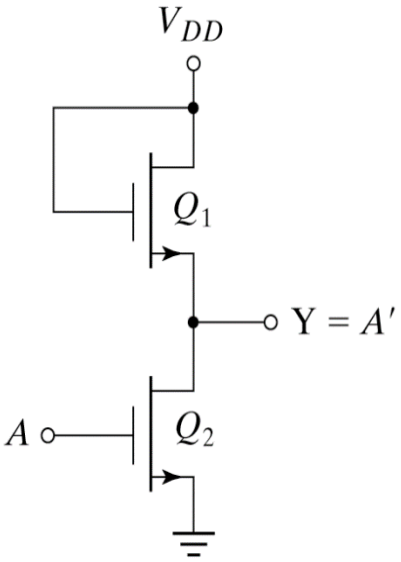
(a) Inverter



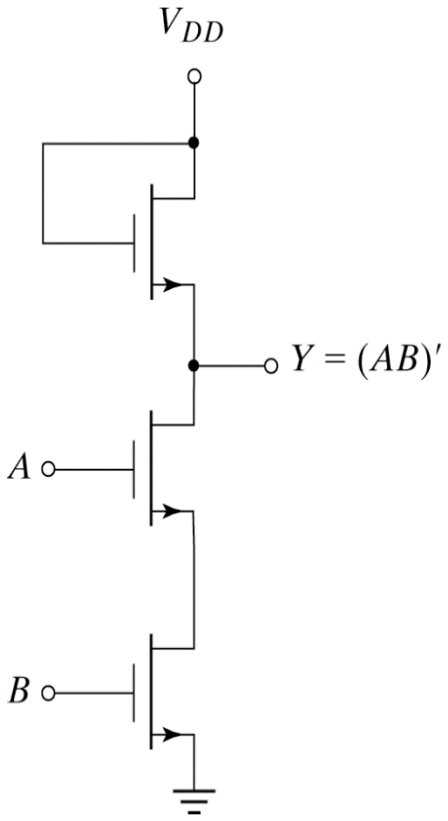
(a) Inverter



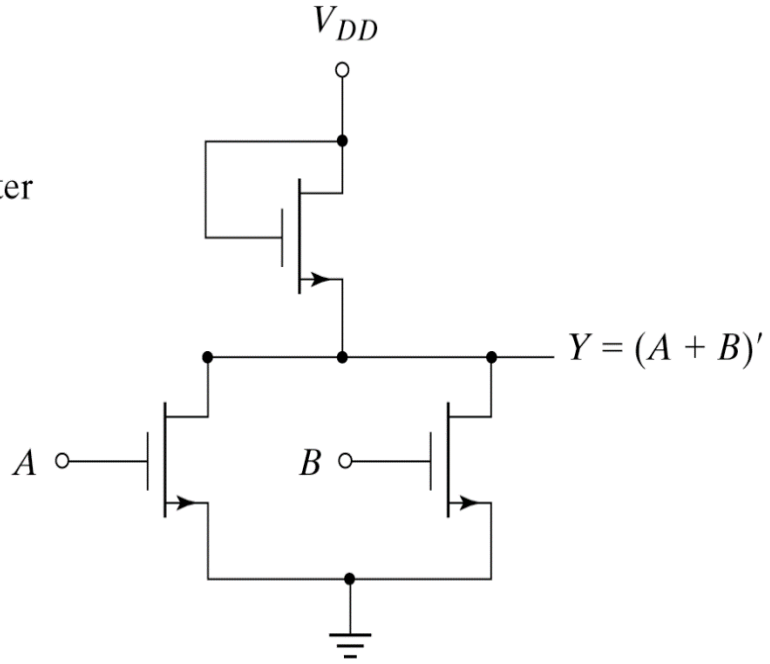
(b) NAND gate



(a) Inverter



(b) NAND gate

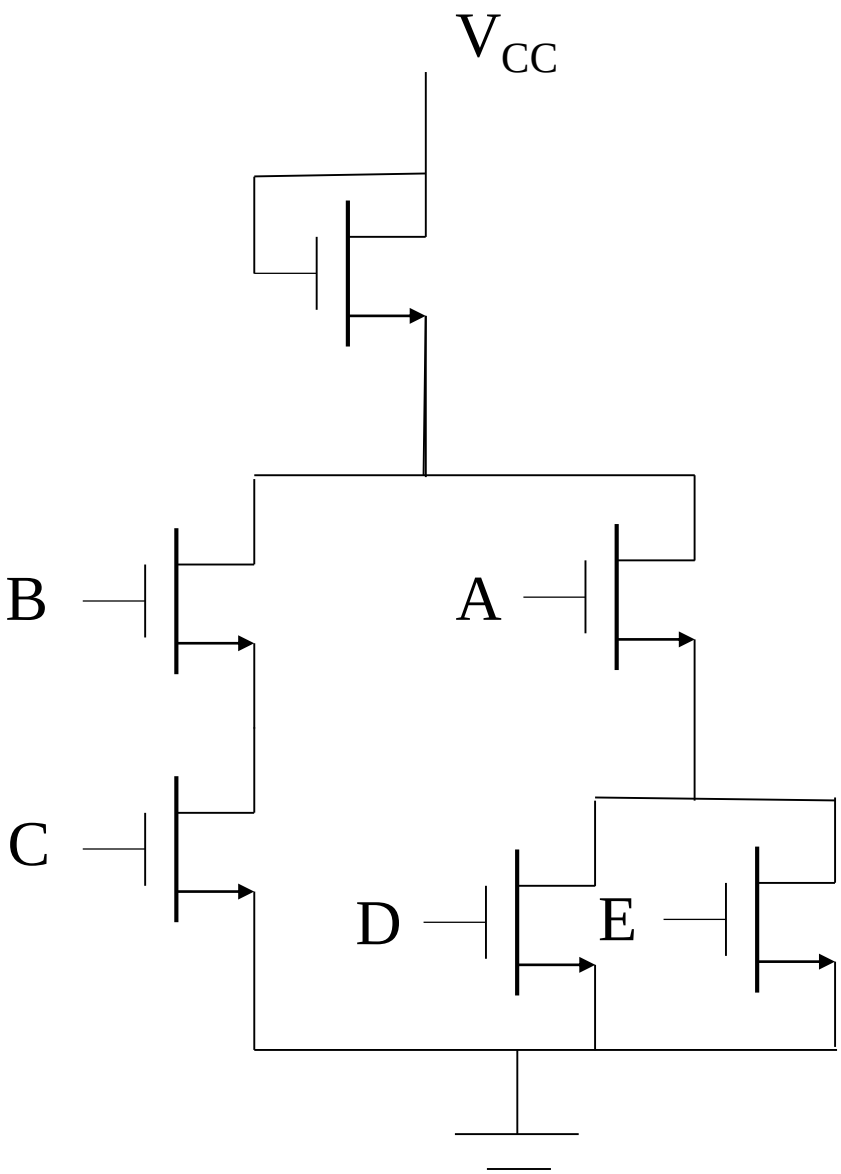


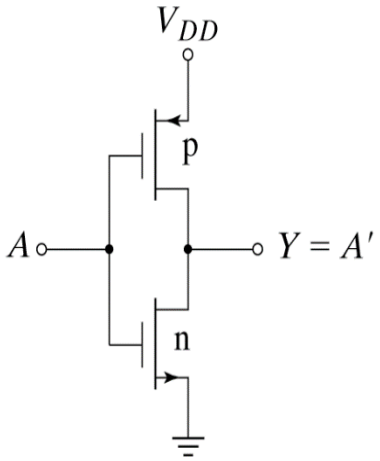
(c) NOR gate

n-channel MOS Logic Circuits

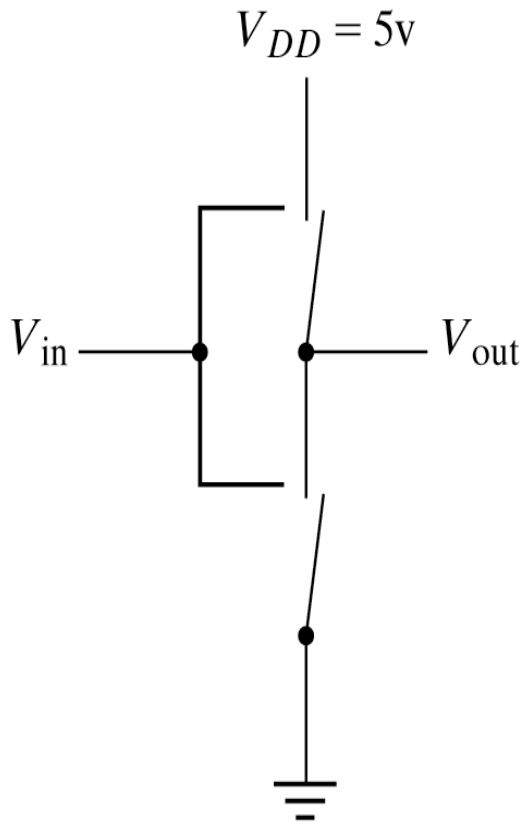
Design the logic Using NMOS

$$Z = (A(D+E) + BC)'$$

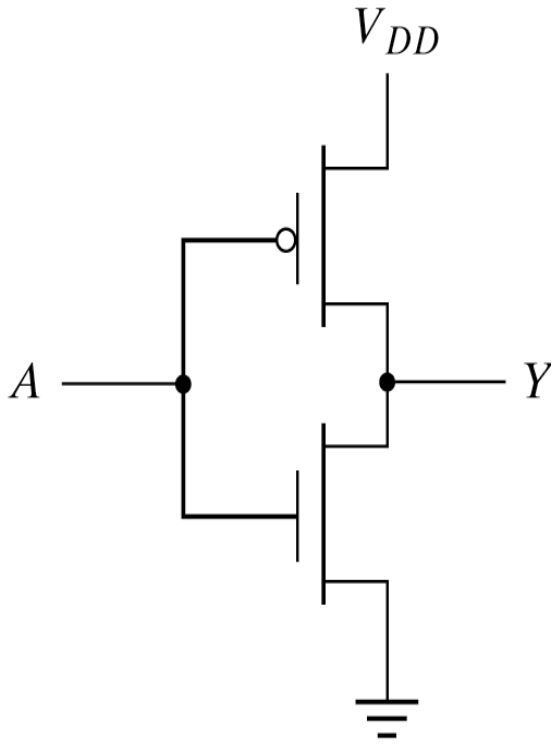

V_{CC}
B
A
C
D
E



(a) Inverter

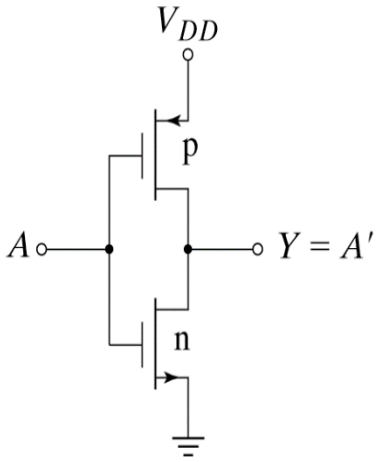


(a) Switch model

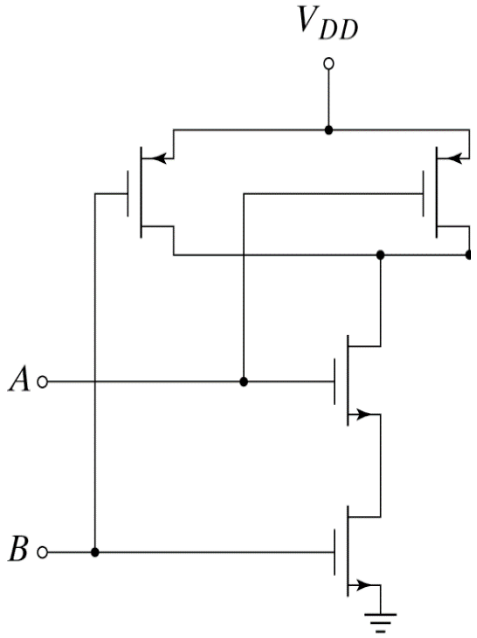


(b) Logical model

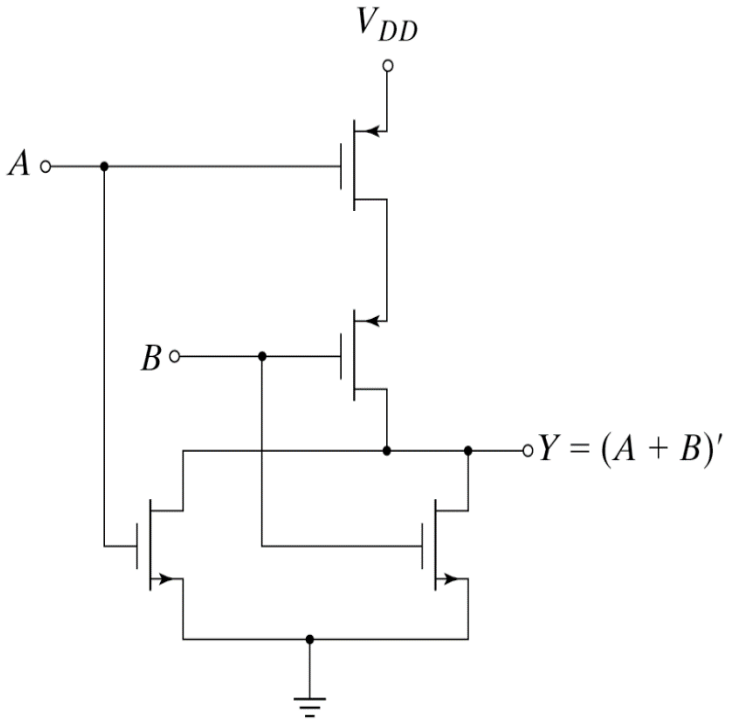
CMOS inverter



(a) Inverter



(b) NAND gate

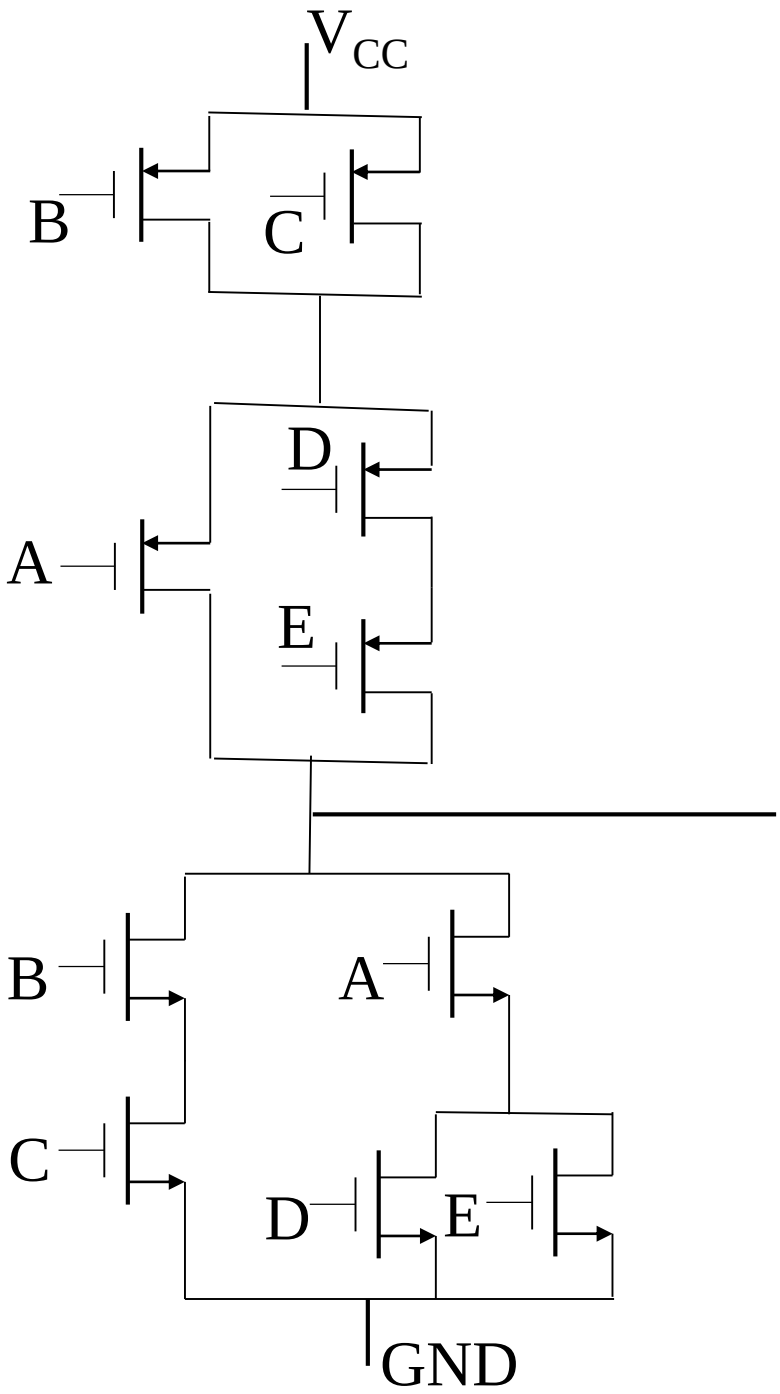


(c) NOR gate

CMOS Logic Circuits

Design the logic Using CMOS

$$Z = (A(D+E) + BC)'$$


V_{CC}
B
C
D
A
E
Z = (A(D+E) + BC)'
B
A
C
D
E
GND