CS/ECE/EEE/INSTR F215:Digital Design

Lecture 31: Shift register counters and Introduction to ASM

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BITS Pilani
Hyderabad Campus

Dr. R. N. Ponnalagu, EEE

Stop thinking of

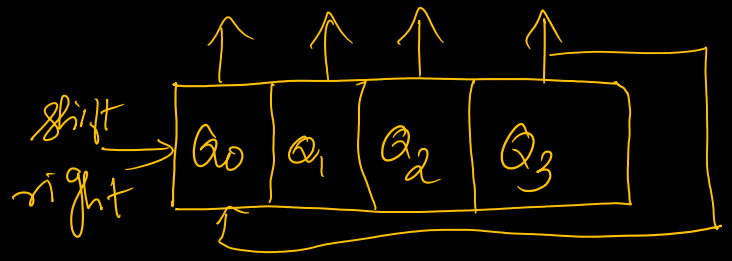
Limitations

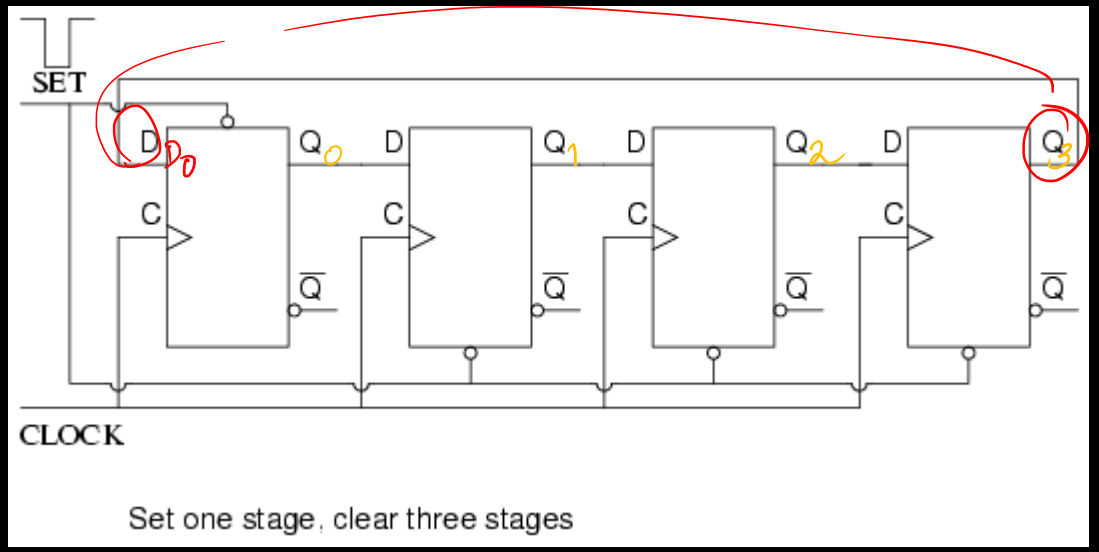
Start thinking of

POSSIBILITIES

Shift register counter : Two types : 1. Ring Counter
2. Johnson counter

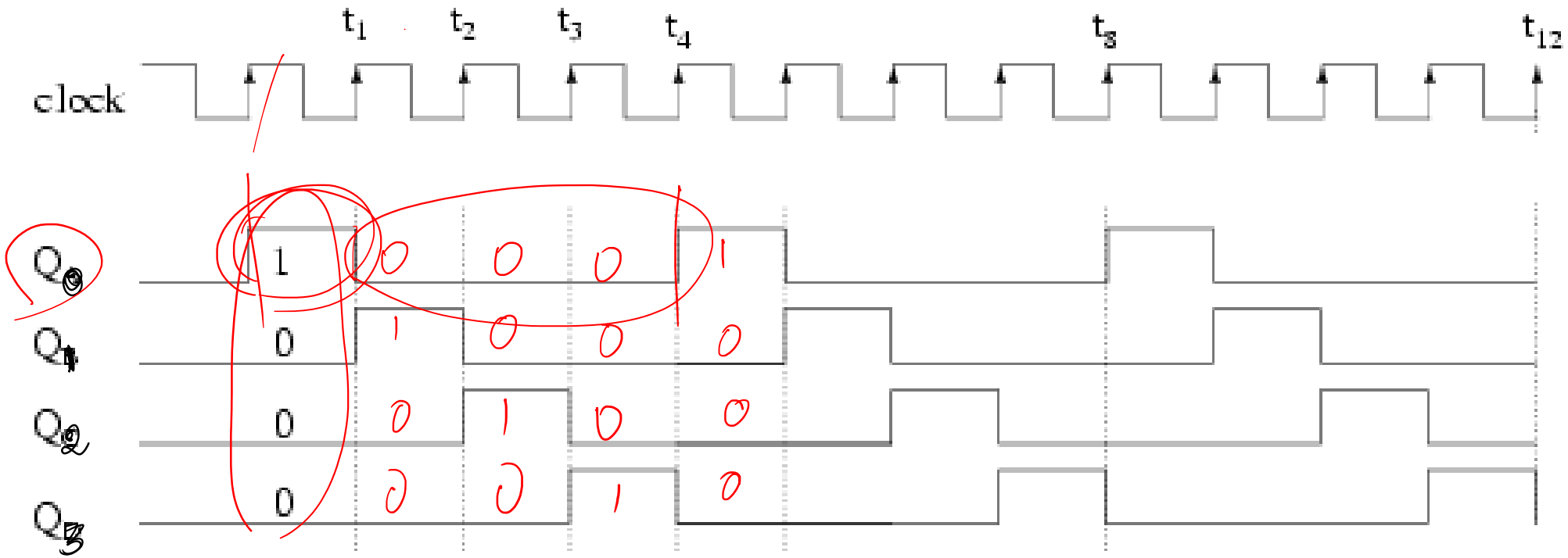
These two shift register circuits go through prescribed sequence of states hence they are called as counters





Set one stage, clear three stages

CLK	Q_0	Q_1	Q_2	Q_3
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0



Load 1000 into 4-stage ring counter and shift

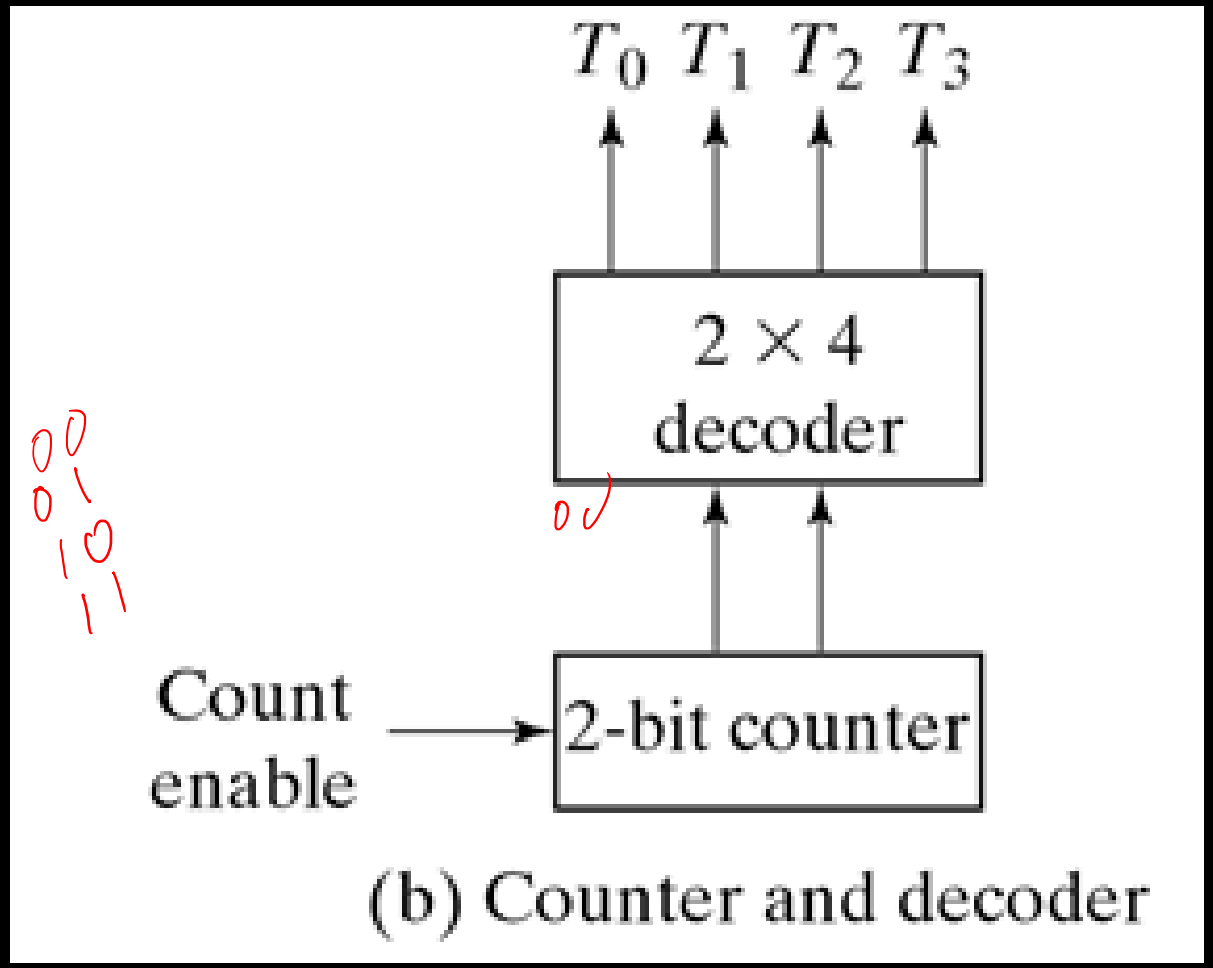
Application:
Used for generation of timing signals

The circuit above is a divide by **4** counter. Comparing the clock input to any one of the outputs, shows a frequency ratio of 4:1

4 different states ⇒ Mod-4 counter

4 flipflops are used → 16 states are possible out of which only 4 are utilized

Another method to generate 4 timing signal.



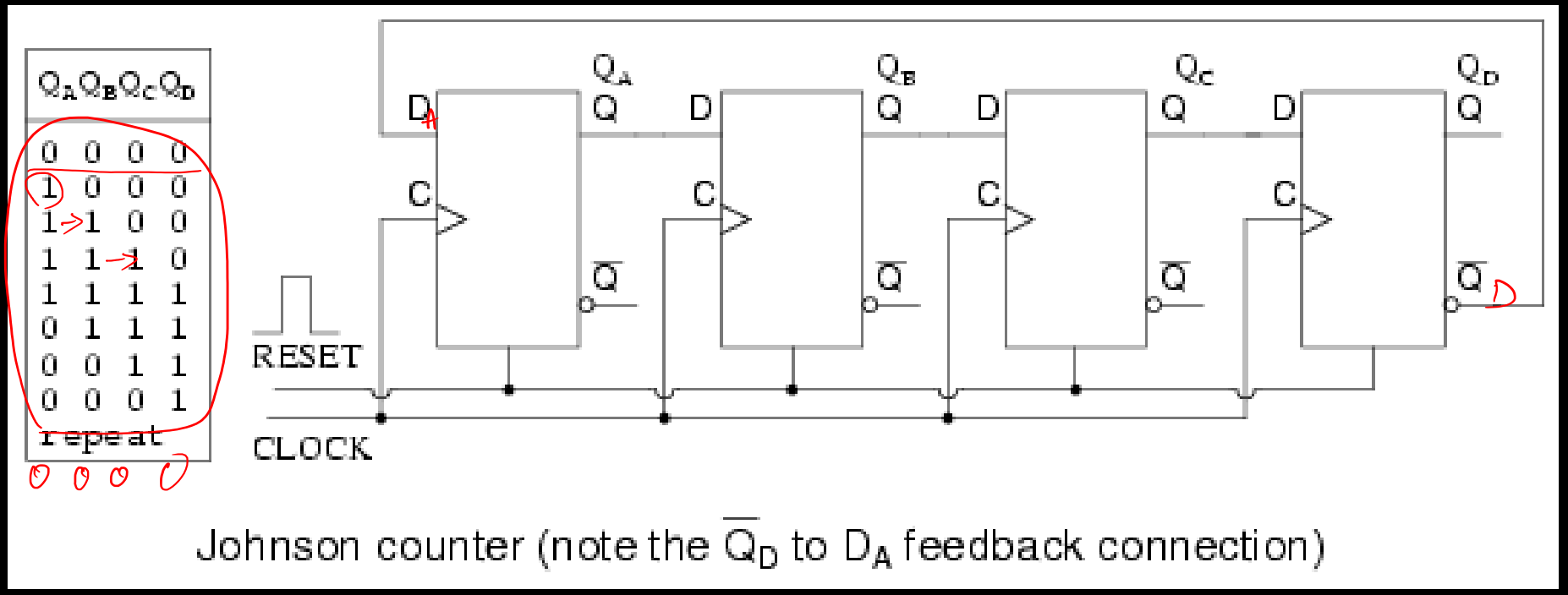
(b) Counter and decoder

To generate 2^n timing signals

1. Shift register with 2^n FFs
   or
2. n-bit binary counter with n to 2^n decoder can be used.

Johnson counter

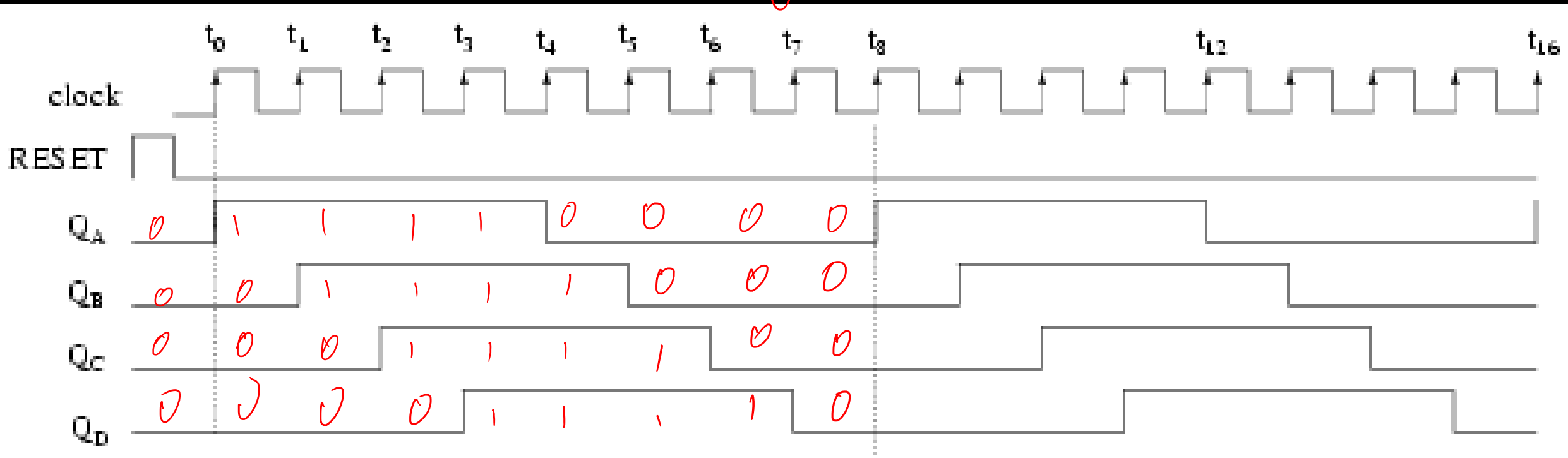
- A k-bit ring counter circulates a single bit and generates k- distinguishable states.
- No. of states can be doubled if shift register is connected as a switch tail ring counter.
- A switch tail ring counter is a circular shift register with the complemented output of the last FF connected to the input of the first FF.



Johnson counter (note the $\overline{Q}_D$ to D_A feedback connection)

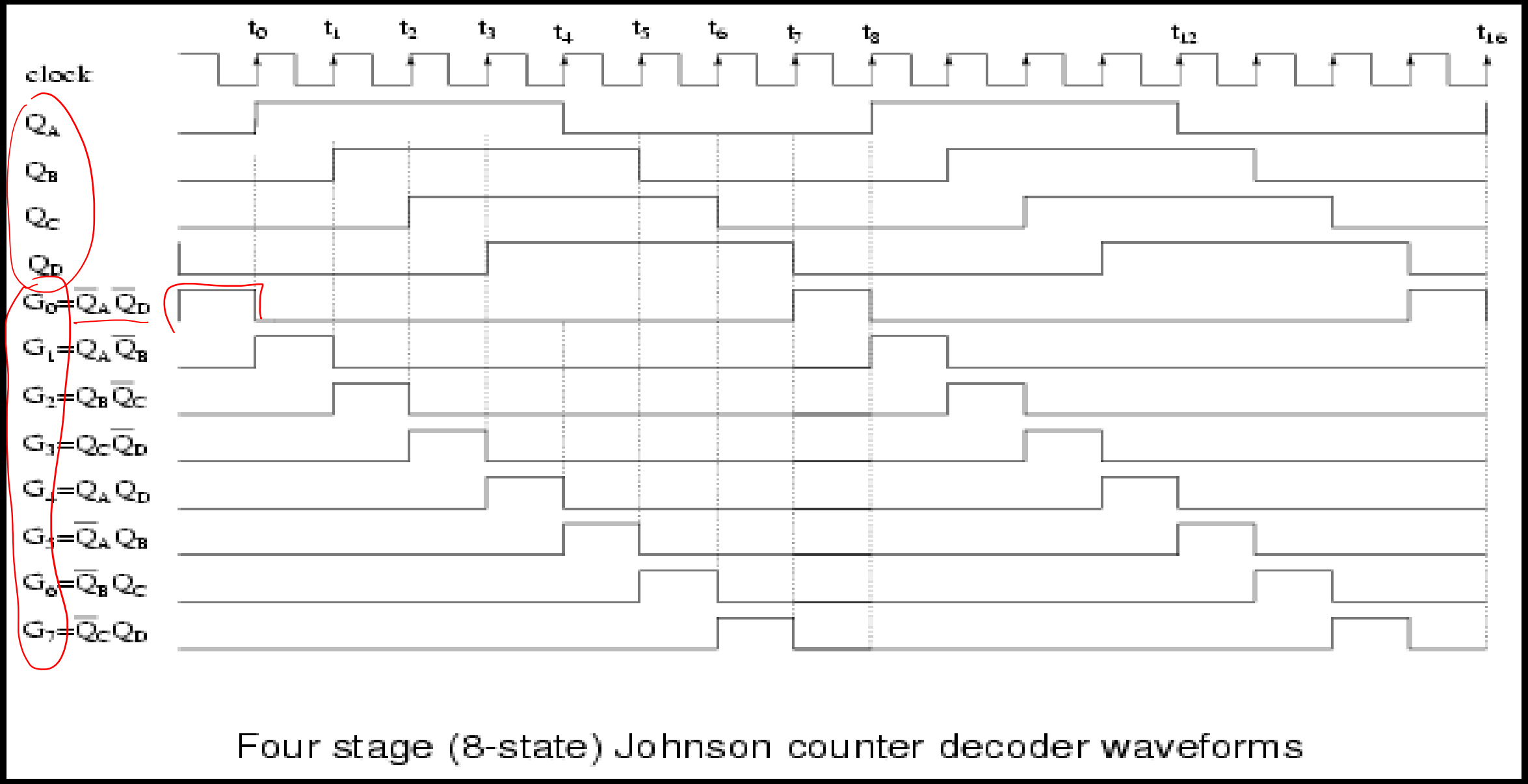
- Starting from cleared state 4 bit switch tail ring counter goes through 8 states

Timing diagram



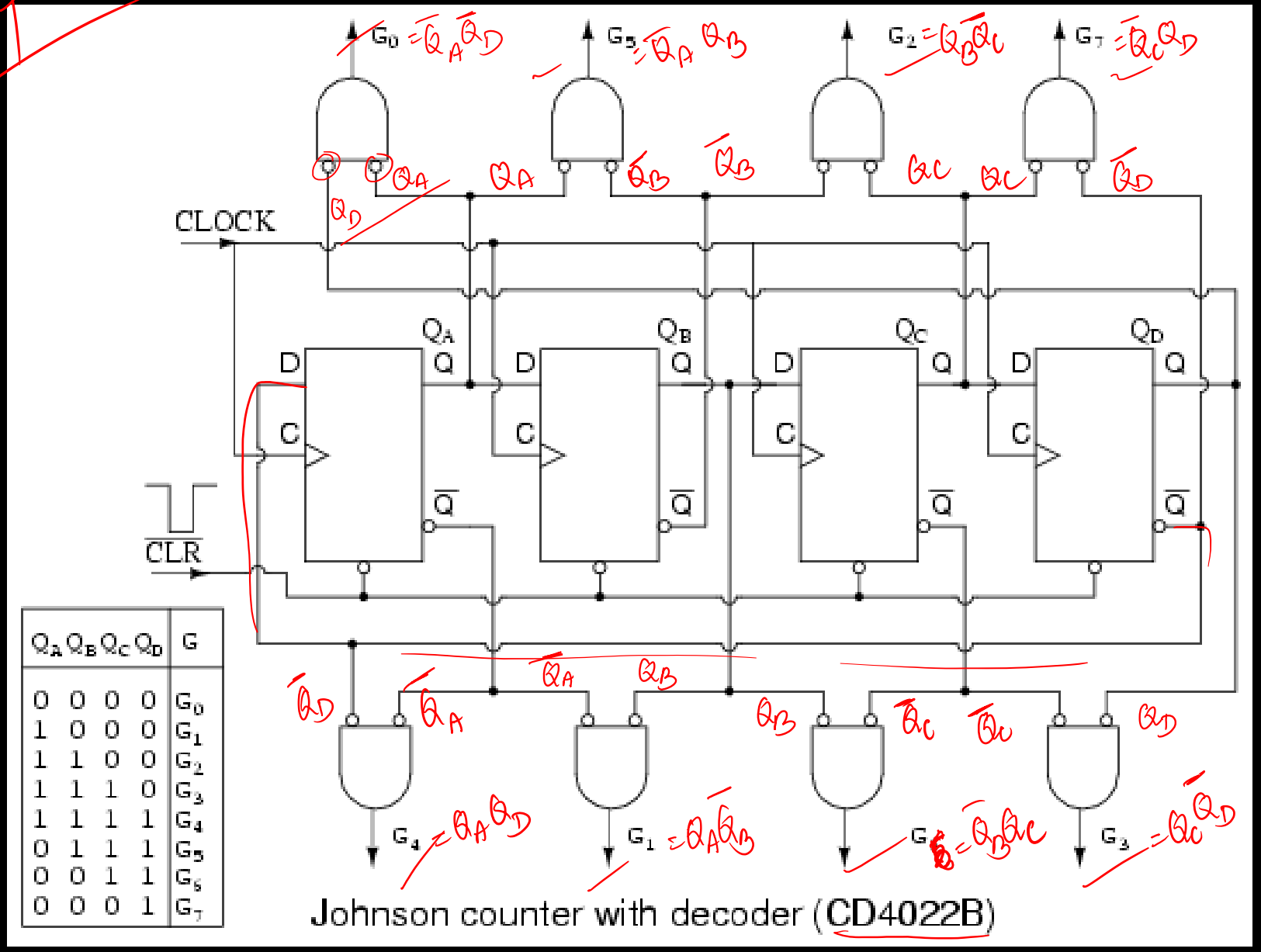
Four stage Johnson counter waveforms

four phased square waves Q_A to Q_D are decoded to eight signals (G_0 to G_7)



Four stage (8-state) Johnson counter decoder waveforms

IC 7474



Q_A	Q_B	Q_C	Q_D	G
0	0	0	0	G_0
1	0	0	0	G_1
1	1	0	0	G_2
1	1	1	0	G_3
1	1	1	1	G_4
0	1	1	1	G_5
0	0	1	1	G_6
0	0	0	1	G_7

Johnson counter with decoder (CD4022B)

A JOHNSON COUNTER is a k-bit switch tail ring counter with 2k decoding gates to provide outputs for 2k timing signals

2 i/p AND gates

Algorithmic State Machines (ASM)

Digital System Logic Design

- Design of digital circuits performing data processing operations

- Design of control circuits to manipulate data operations

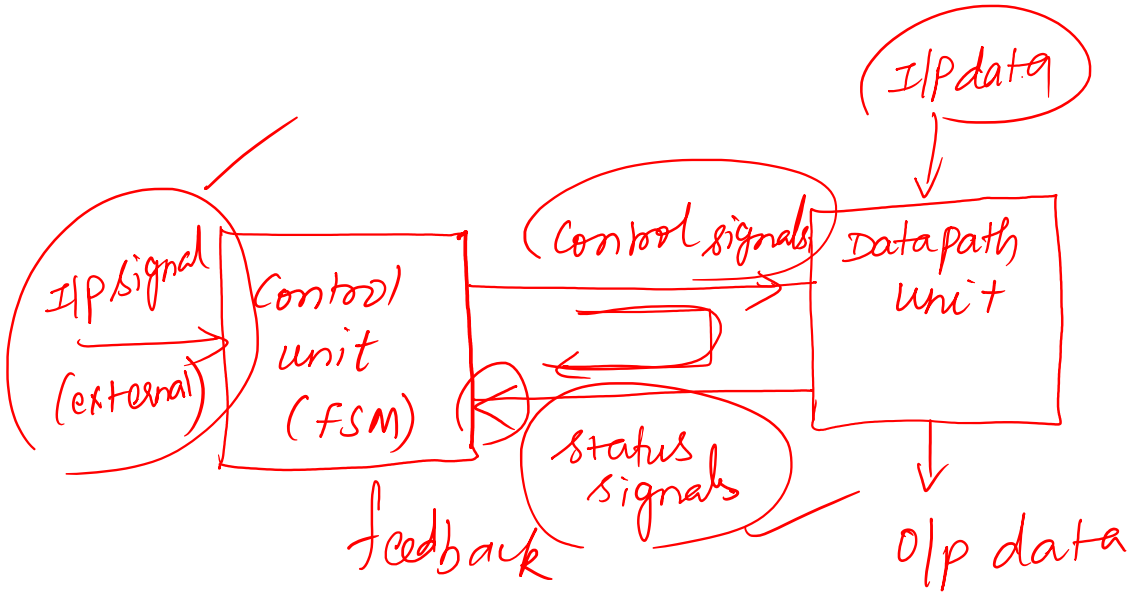
- **Binary information stored in Digital Systems can be classified as Data or Control**

- **Data are discrete elements of information (binary words) manipulated by performing arithmetic, logic, shift and other similar data processing operations. Implemented using digital H/W components such as adders, multiplexers, decoders, registers, counters etc.**

- **Control information provides command signals that coordinate and execute the various operations in the data section to execute desired data processing tasks**

- **Various modules are interconnected to form digital system**

Relationship between control logic and data processing operations



Control and data path interaction

- Data path unit manipulates data in the registers according to system requirements.
- Control unit issues sequence of commands to data path unit
- Feedback from data path unit to control unit provides status conditions
- Control unit uses the status conditions and external input to determine the sequence of control signals that direct the operation of data path unit.

FSM: Finite State Machine

- **FSM is a synchronous sequential circuit**
- **FSM produces the control commands for the system**
- **Control commands are functions of i) external inputs, ii) status signals and the iii) state of the machine**
- **Control commands are fed to data path unit**
- **Depending on present state, external inputs and status conditions of data path, FSM goes into its next state**

Algorithm

- The control sequence and data path tasks of a digital system are specified by means of a hardware algorithm
- An algorithm consists of a finite no. of procedural steps that specify how to obtain solution to a problem
- A hardware algorithm is a procedure for solving the problem with a given piece of equipment
- Challenge is the formulation of hardware algorithm for achieving required objectives

Algorithm

- A flow chart is the convenient way to specify the sequence of steps and decision paths for the algorithm

- Flowchart translates verbal instructions to an information diagram that depicts sequence of operations along with the conditions necessary for their execution.

- An algorithmic state machine (ASM) chart is a special purpose flowchart developed to define algorithms for execution on digital hardware

- Conventional flowchart describes procedural steps and decision paths of an algorithm in a sequential manner, without taking into consideration their time relationship

- ASM chart describes the sequence of events as well as the timing relationship between states of sequential controller and the events that occur while going from one state to next

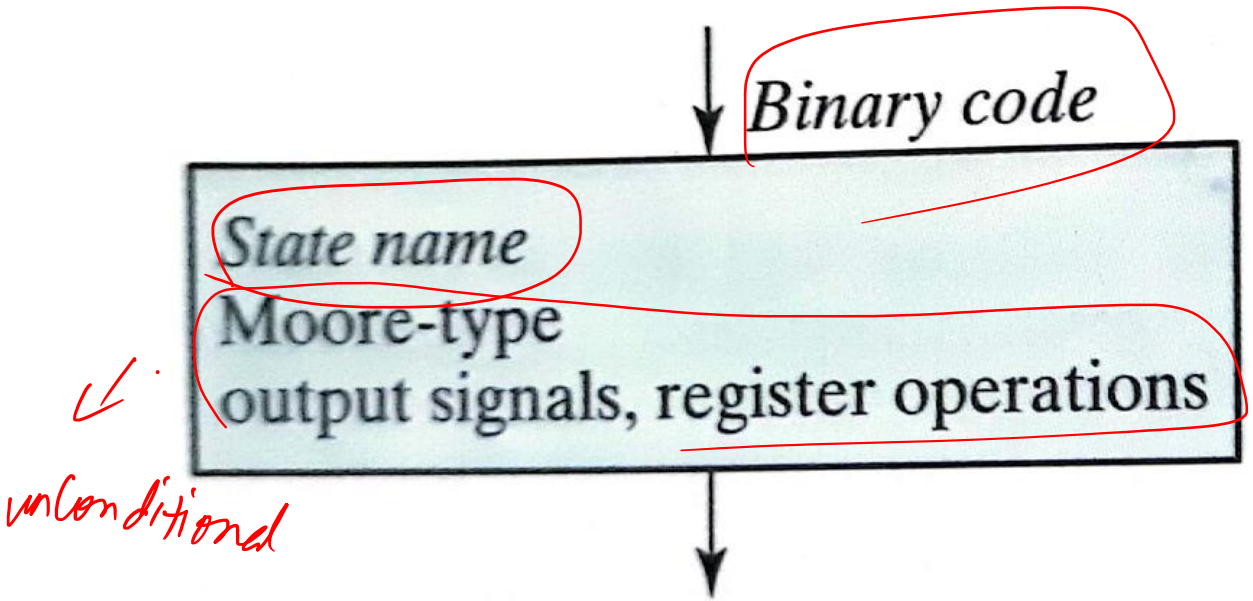
- **Flowchart developed to design Digital Hardware Algorithms is Algorithmic State Machines (ASM) chart**

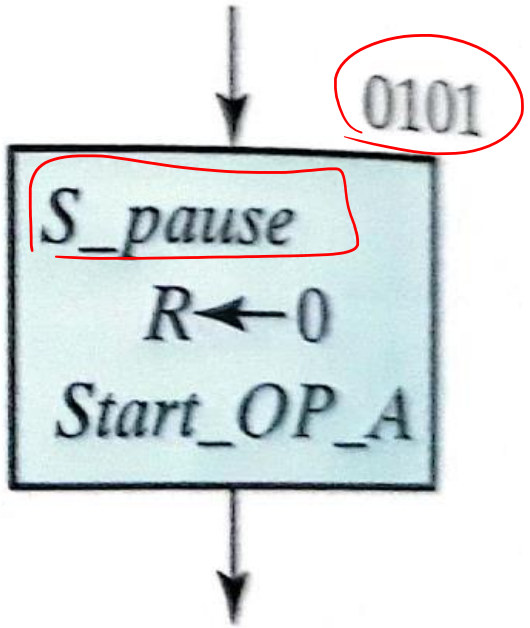
ASM CHART
composed of three basic elements

- The State box
- The decision box
- The conditional box

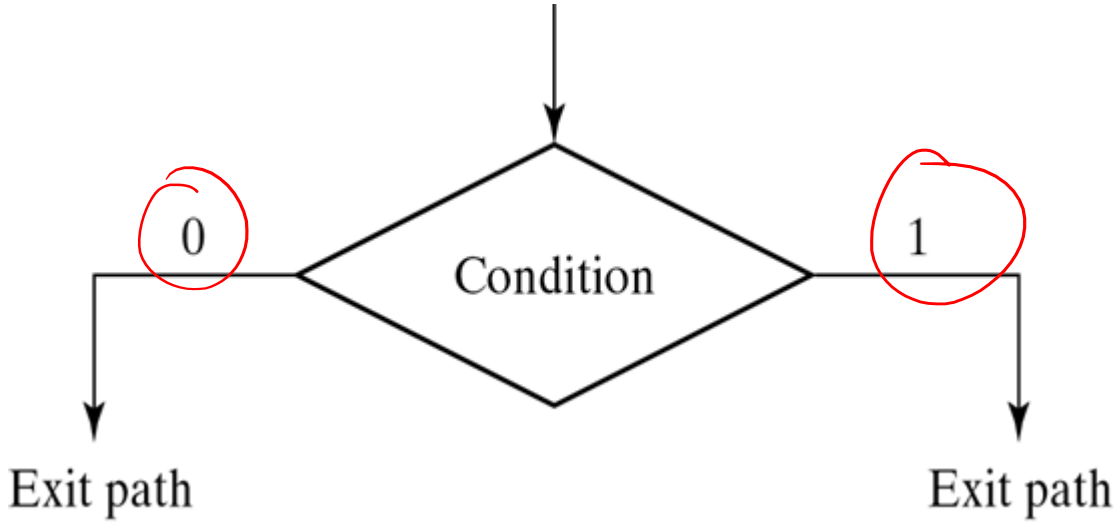
- **A state is indicated by the state box (Rectangle in shape) within which are written i) register operations that occur when state transitions to next state are written and/or ii) the names of the output signal that the control generates while being in the present state.**

- **State is given a symbolic name (Upper left corner of the box), binary code assigned to state (upper right)**



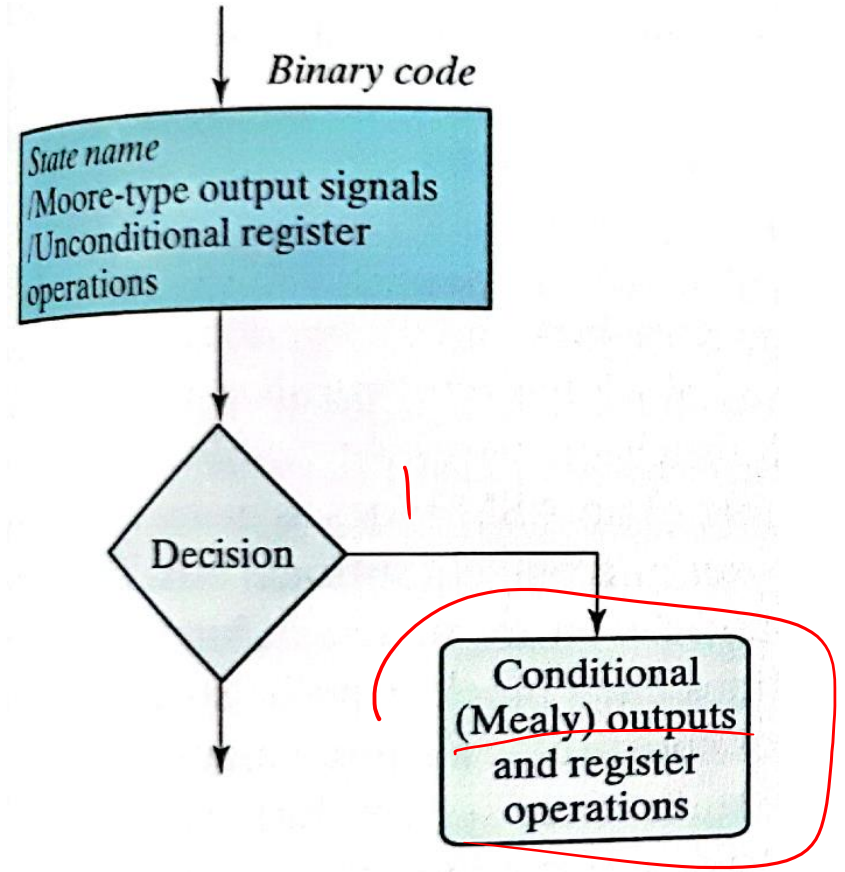


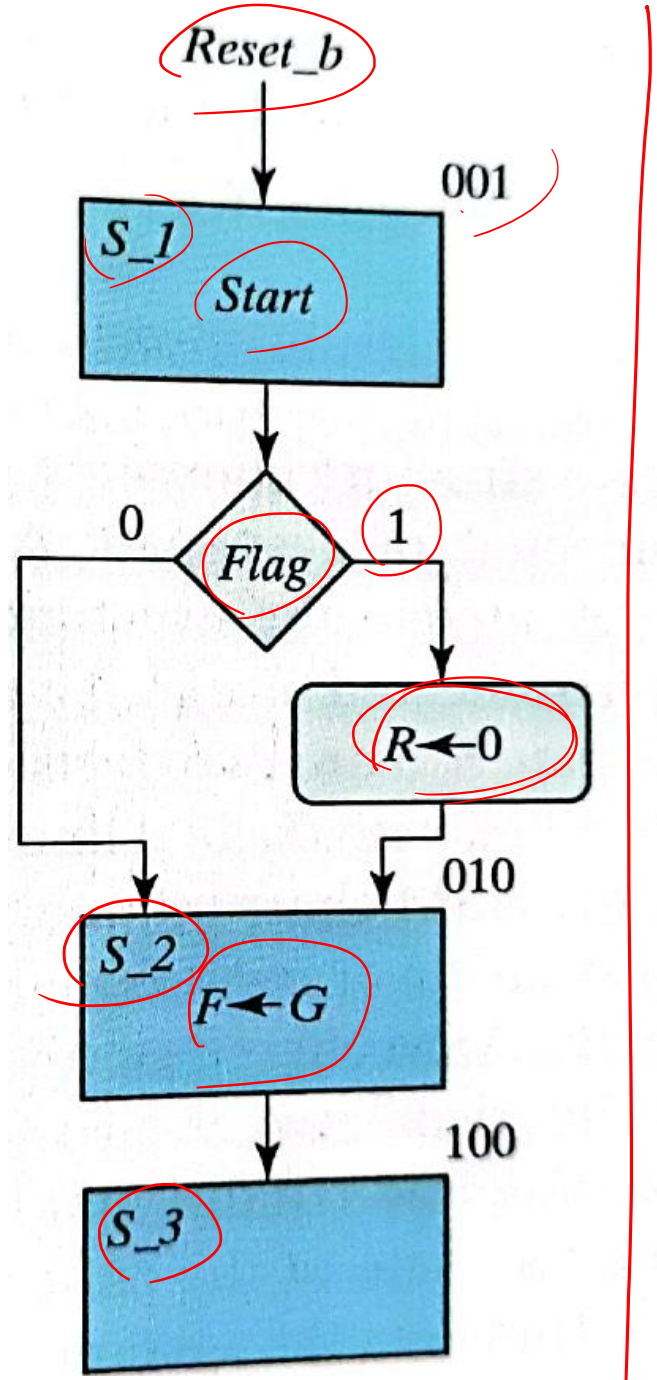
- **Decision box (diamond shaped) indicates the effect of an input on the control subsystem**
- **Condition to be tested is written inside the box**
- **One exit path is taken if the condition is true (label 1) and another if false (label 0)**

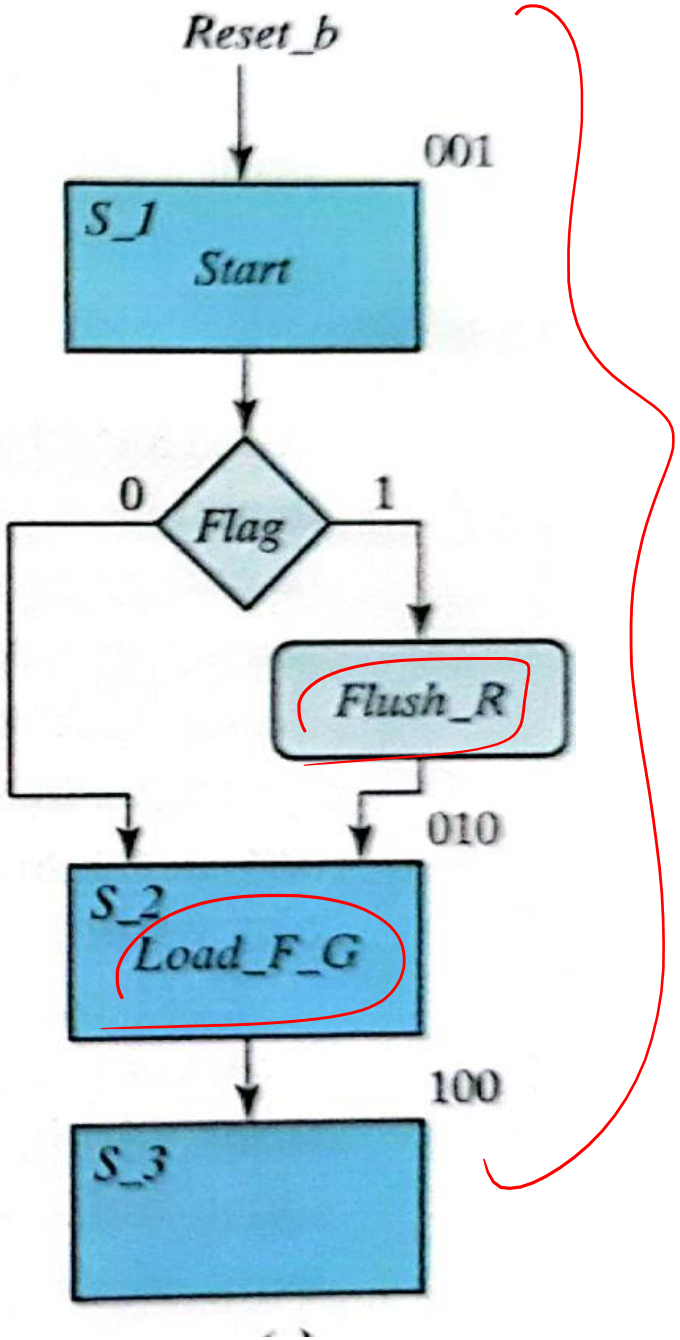


- **State box and decision box are similar to those used in conventional flowchart**

- **The conditional box (Shape: rounded corners) is unique to ASM chart**
- **Input path to conditional box comes from one of exit paths of a decision box**
- **The outputs listed inside a conditional box are generated during a given state and the register operations are associated with a transition from the state**




Reset_b
001
S_1
Start
0
Flag
1
R←0
010
S_2
F←G
100
S_3


Reset_b
001
S_1
Start
0
Flag
1
Flush_R
010
S_2
Load_F_G
100
S_3