BIRLA INSTITUTE OF SCIENCE AND TECHNOLOGY PILANI, HYDERABAD CAMPUS

DIGITAL DESIGN LABORATORY (Session 2021-22)

Workbook

Experiment -4

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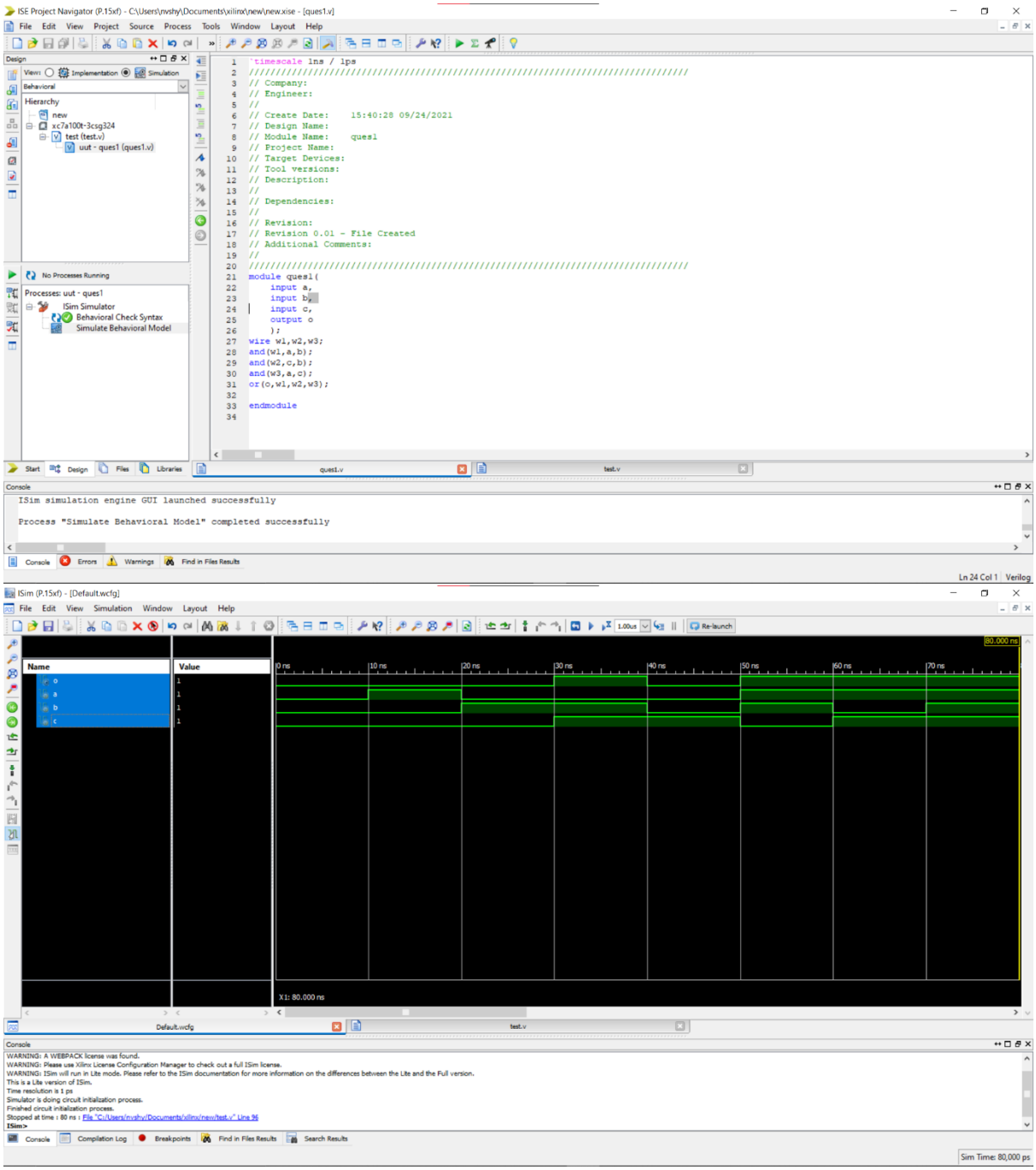
Title of Experiment: Experiment 4

Problem 1:

Implement the Majority circuit; F = AB + BC + AC using Xilinx ISE

(Provide proper snapshot and Show the graphical output)


ISE Project Navigator (P.15xf) - C:\Users\nvshy\Documents\xilinx\new\new.xise - [ques1.v]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
new
xc7a100t-3csg324
test (test.v)
uut - ques1 (ques1.v)
Processes: uut - ques1
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
1 `timescale 1ns / 1ps
2 //
3 // Company:
4 // Engineer:
5 //
6 // Create Date: 15:40:28 09/24/2021
7 // Design Name:
8 // Module Name: ques1
9 // Project Name:
10 // Target Devices:
11 // Tool versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module ques1(
22 input a,
23 input b,
24 input c,
25 output o
26);
27 wire w1,w2,w3;
28 and(w1,a,b);
29 and(w2,c,b);
30 and(w3,a,c);
31 or(o,w1,w2,w3);
32
33 endmodule
34
Console
ISim simulation engine GUI launched successfully
Process "Simulate Behavioral Model" completed successfully
Ln 24 Col 1 Verilog
ISim (P.15xf) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
o
a
b
c
1
1
1
1
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80.000 ns
X1: 80.000 ns
Console
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Stopped at time : 80 ns : File "C:/Users/nvshy/Documents/xilinx/new/test.v" Line 36
ISim>
Sim Time: 80,000 ps

Problem 2:

Implement Parity Generator (both even and odd) in Xilinx ISE

(Provide proper snapshot and show the graphical output)