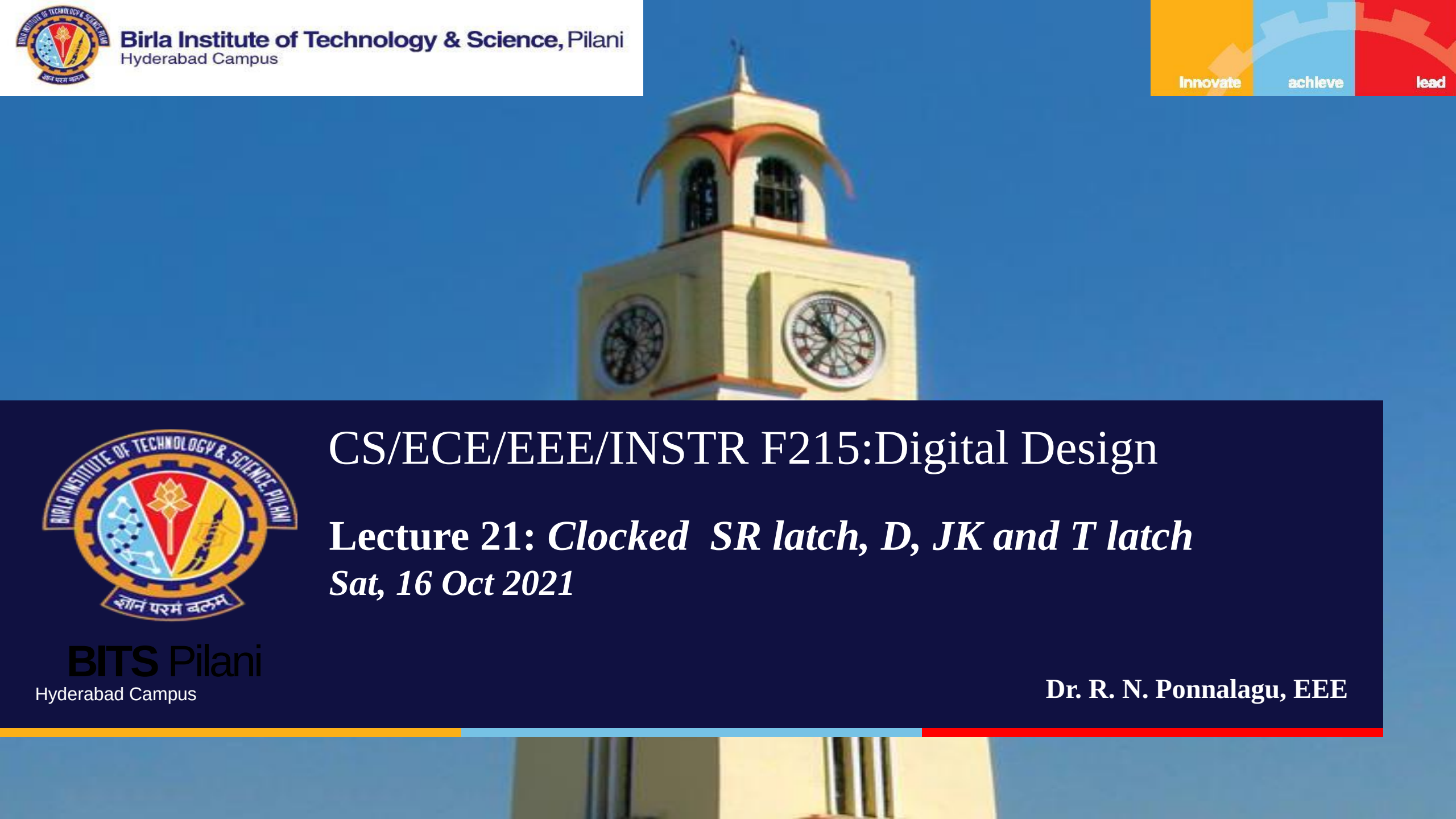

CS/ECE/EEE/INSTR F215:Digital Design

Lecture 21: *Clocked SR latch, D, JK and T latch*

Sat, 16 Oct 2021

BITS Pilani
Hyderabad Campus

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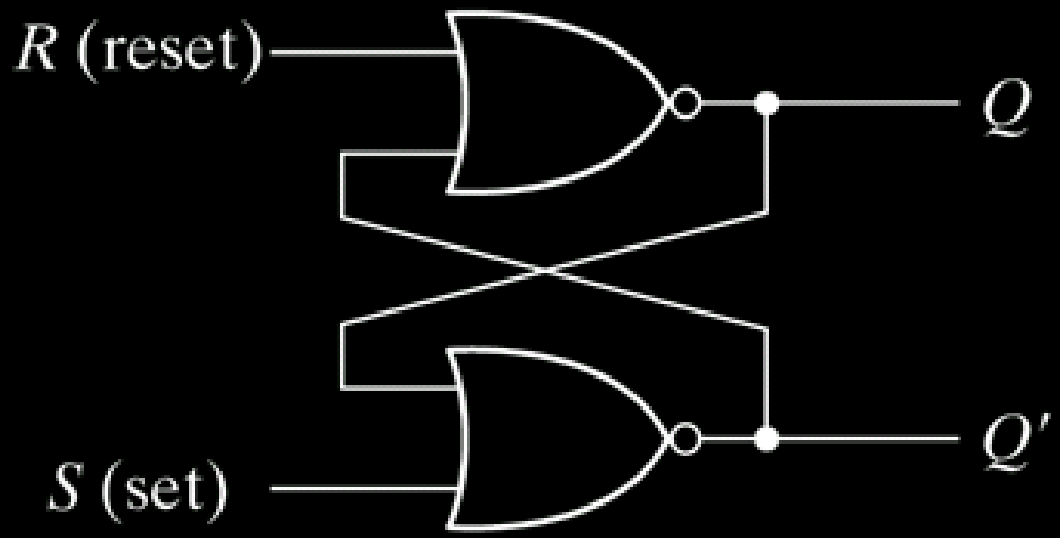
A seed grows with no sound,
but a tree falls with huge noise.
Destruction has noise,
but creation is quiet.
This is the power of silence.
"Grow silently"

NOR based RS latch



Charac. table

Ips		Present state	next state of the latch	
S	R	Q_t	Q_{t+1}	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	x	Indeterminate
1	1	1	x	

Characteristic equation $Q_{t+1} = S + \bar{R} Q_t$

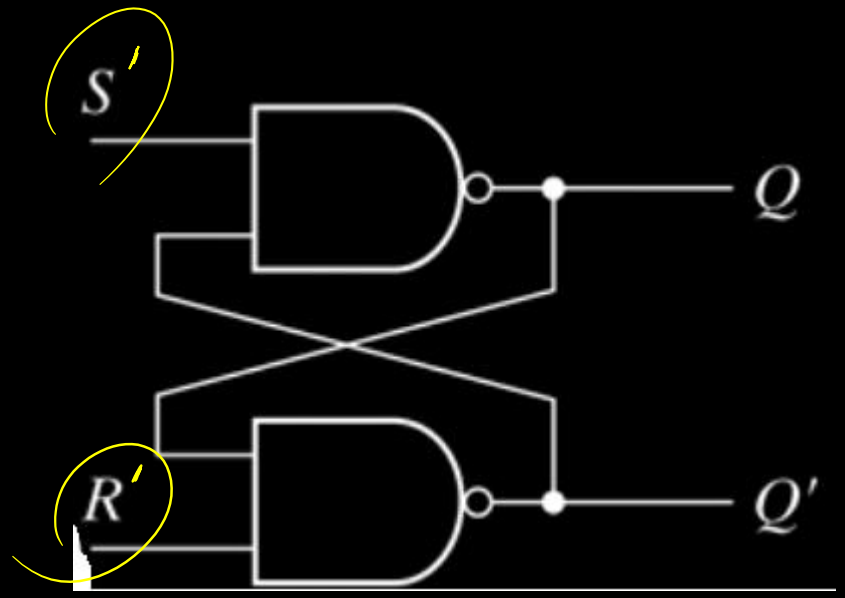
Provided $SR = 0$ - $\dot{x}$ -

undefined

NAND Based Latch

S'R' Latch

Complemented version of NOR based latch

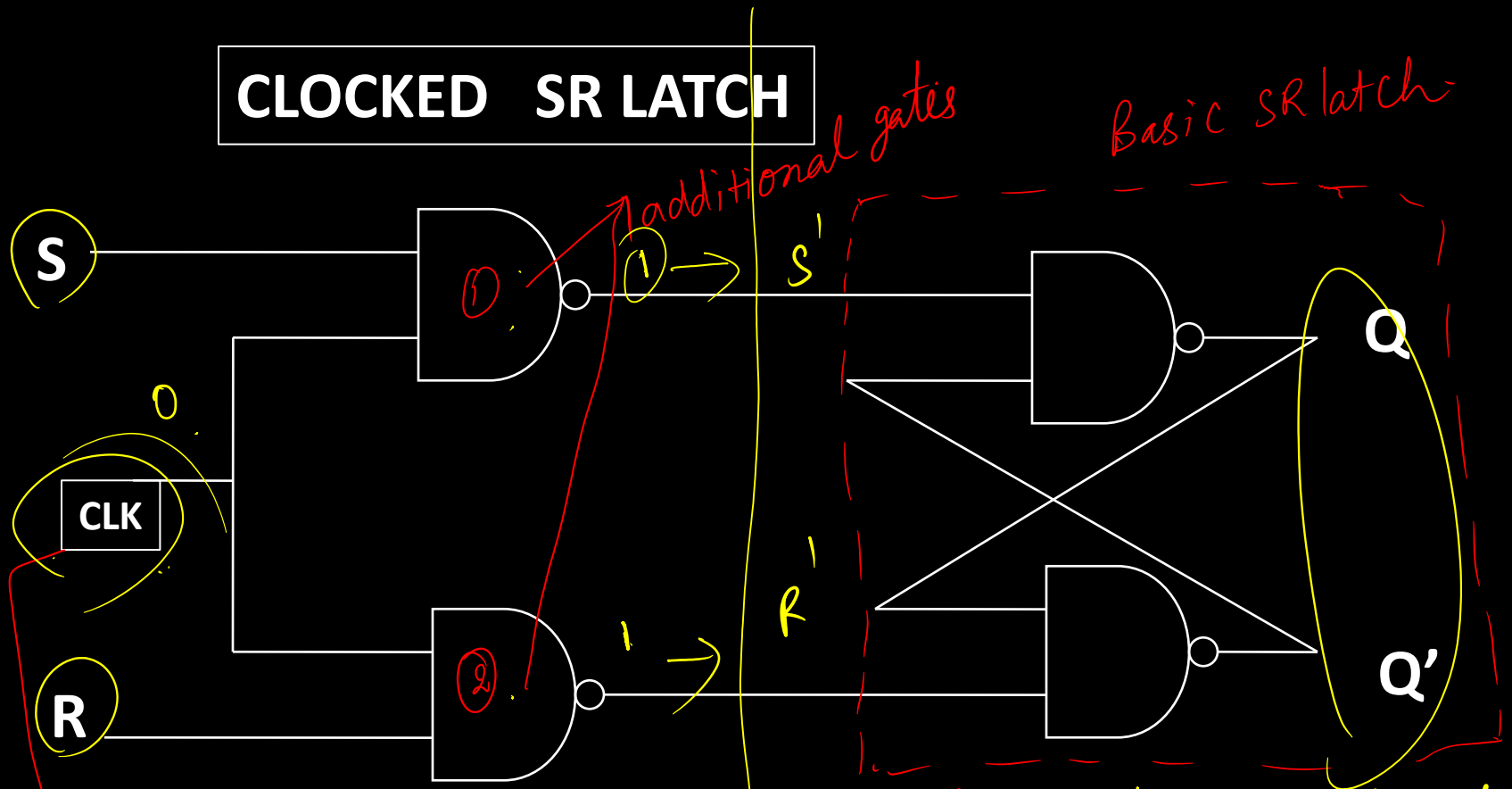


Two Cross-coupled NAND gates

S'	R'	Q	Q'	
0	0	Forbidden		Not recommended
0	1	1	0	Set
1	0	0	1	Reset
1	1	Q	Q'	No change

Quiescent state

CLOCKED SR LATCH



NAND gate

A	B	o/p
0	0	1
0	1	1
1	0	1
1	1	0

NO change in o/p

additional i/p signal ⇒ Control signal ⇒ determines when S & R i/ps can affect the circuit

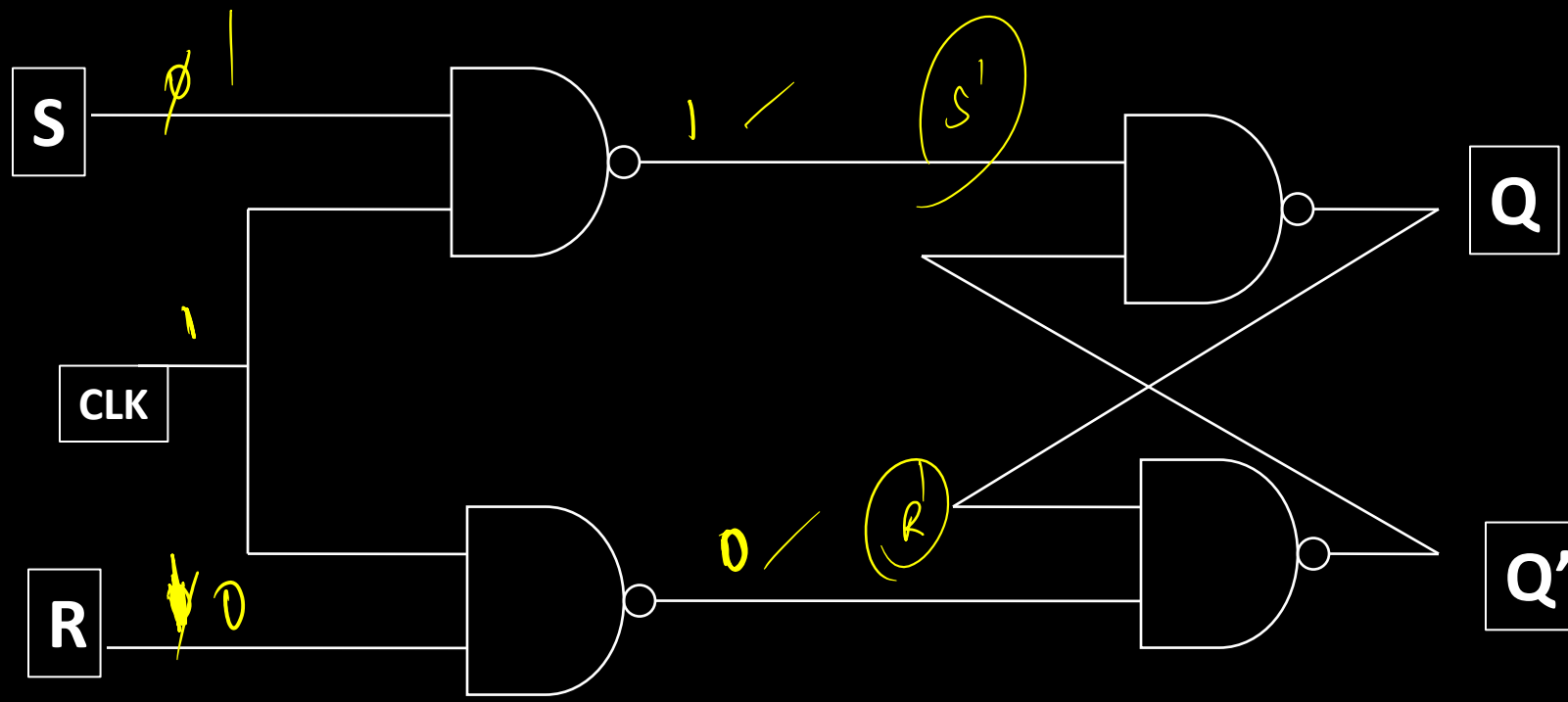
(or) Enable

Clock

Basic SR latch + 2 additional NAND gates

Clock => 0 gates ① & ② o/p is 1 ⇒ No change state for latch

CLOCKED SR LATCH



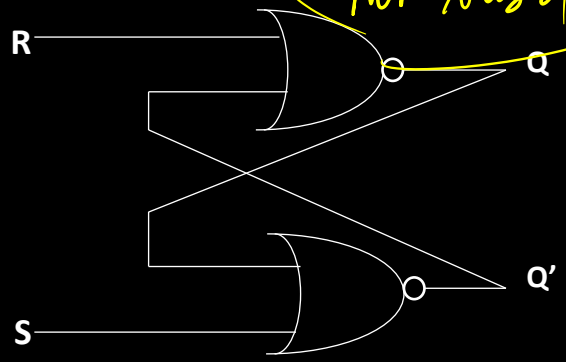
A Control (or) clock i/p is added to determine when S & R inputs should affect the circuit

CLK	S	R	Q
0	X	X	No change
1	0	0	No change
1	0	1	0 Reset state
1	1	0	1 set state
1	1	1	Not to apply / indeterminate

don't care

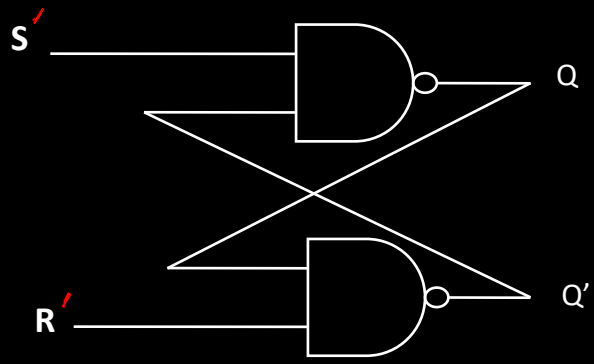
Not based RS Latch

NOR based



S	R	Q
0	0	no change
0	1	0
1	0	1
1	1	Not recommended

NAND based

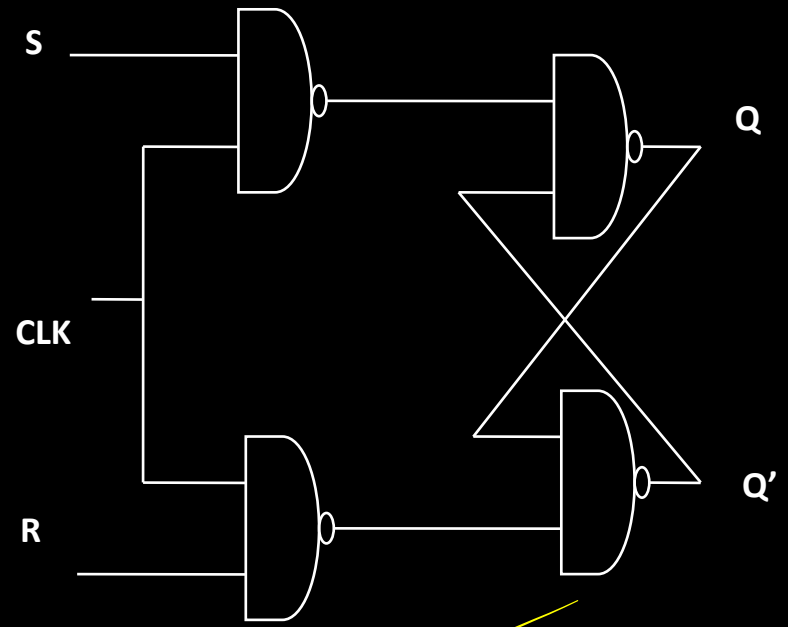


S'	R'	Q
0	1	1
1	0	0
1	1	No Change
0	0	Not recommended

both are same

Final

Clocked NAND based



CLK	S	R	Q
0	X	X	No change
1	0	0	No change
1	0	1	0
1	1	0	1
1	1	1	Not to apply.

When an SR NOR latch goes into an indeterminate state?

when both i/ps are '1'

When an SR NAND latch goes into an indeterminate state

when both i/ps are '0'

Problem in SR latch ?

Drawback (or) D-adv

Indeterminate state ⇒ both i/ps S & R should not be '1' at the same time.

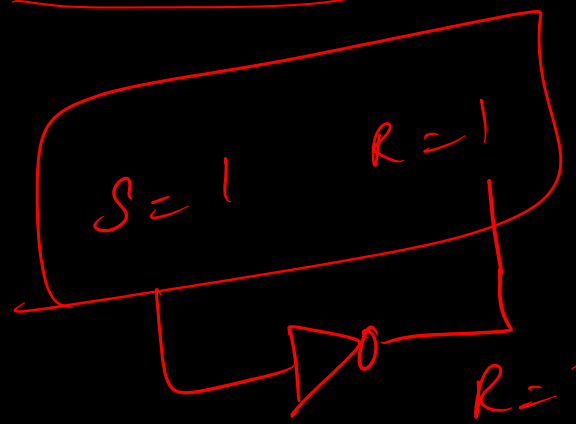
this makes it difficult to manage.

SR latch is important circuit as it is useful for other circuits constructed from it.

How to avoid this ?

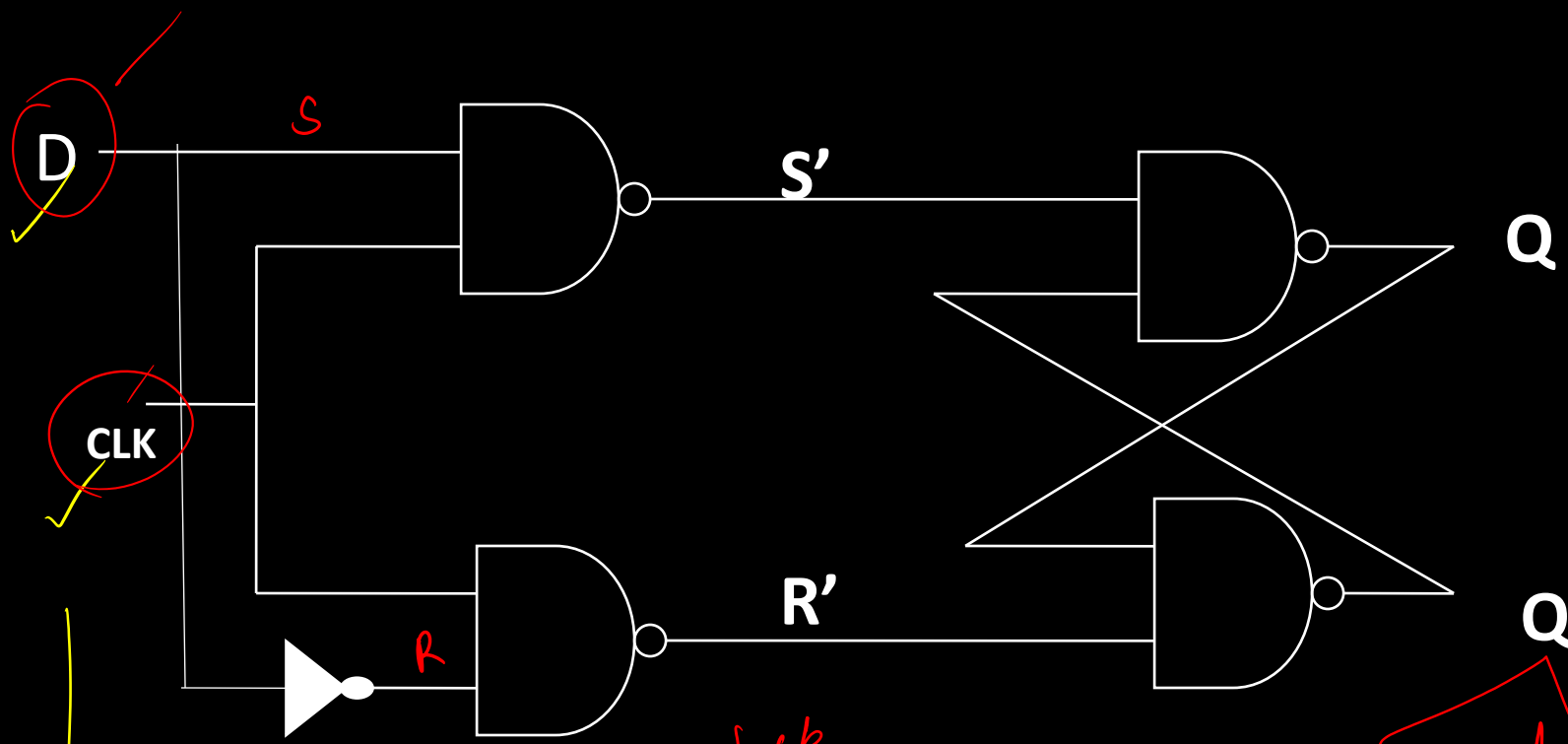
o/p keep or change

Solution ⇒ ?



⇒ should not happen

D latch



only two i/ps ⇒ D & clock

D ⇒ goes to S

$\bar{D}$ ⇒ goes to R

S=0, R=1 ✓ avoid

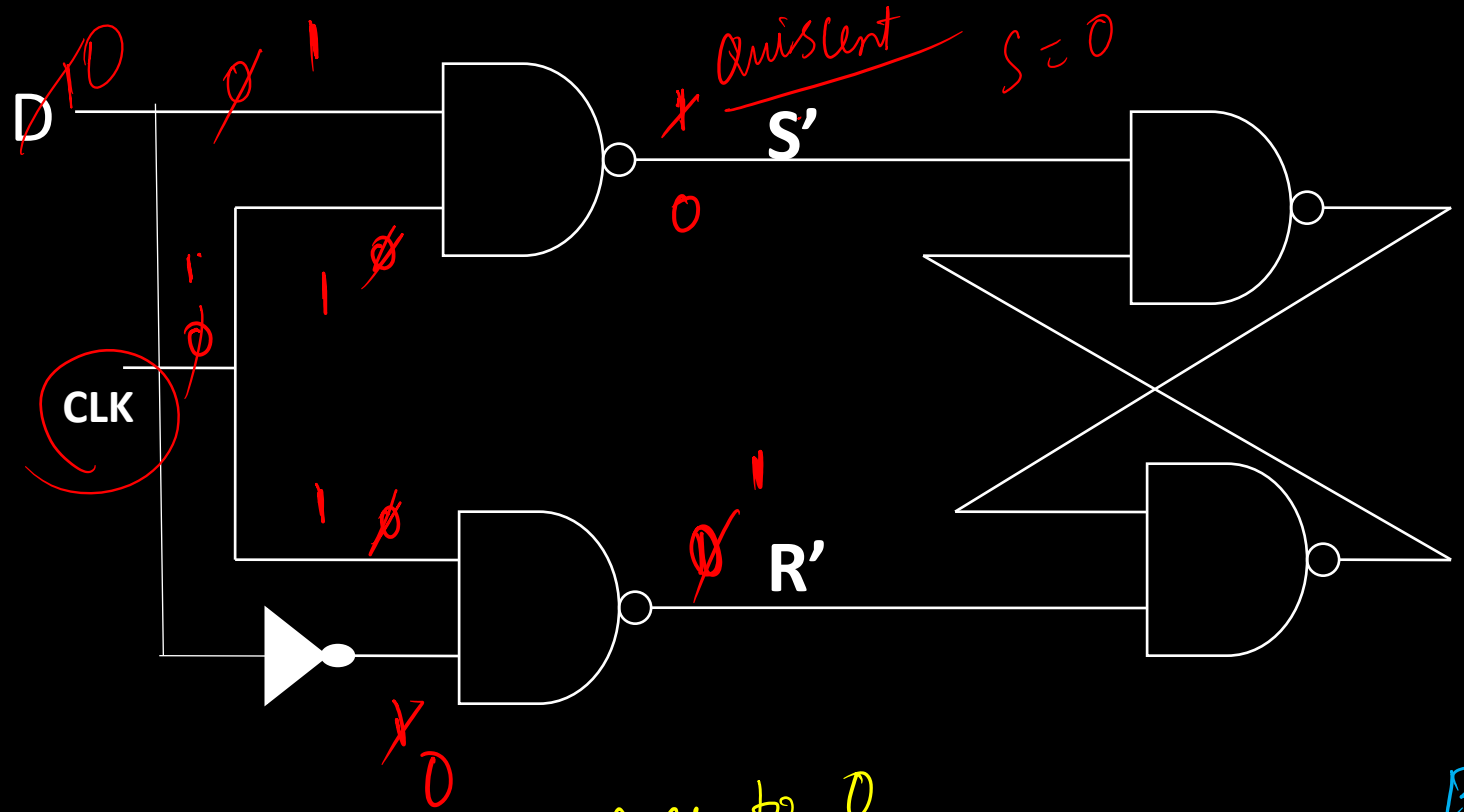
S=1, R=0 ✓ S & R ≠ '1'

(1 1)

One way to eliminate the undesirable condition in SR latch is to ensure that both S' & R' i/ps are never equal to '1' at the same time.

This can be obtained by connecting a NOT gate b/w them.

∨ Inverter b/w S & R i/ps



Clock	D	Q_{t+1} (Next state of Q)
0	X	No change
1	0	0 (reset state)
1	1	1 (set state)

if D = 0 Q goes to 0

if D = 1 Q goes to 1

D latch is transparent latch

Binary information present at the data i/p (D i/p) of D latch is transmitted to Q o/p of D latch when clock i/p is asserted.

o/p follows changes in i/p when clock is high.

Characteristic table

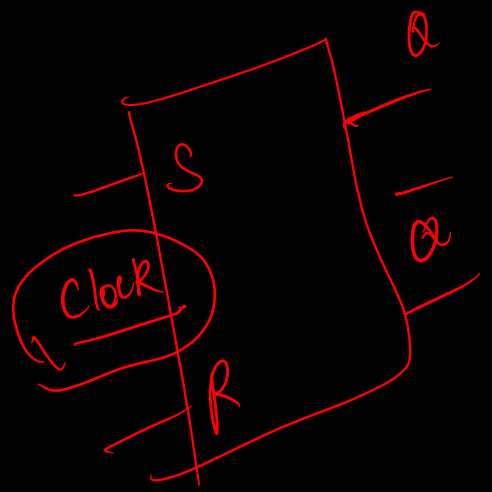
I/P	P.S	N.S	
D	Q_t	Q_{t+1}	
0	0	0	reset state
0	1	0	
1	0	1	set state
1	1	1	

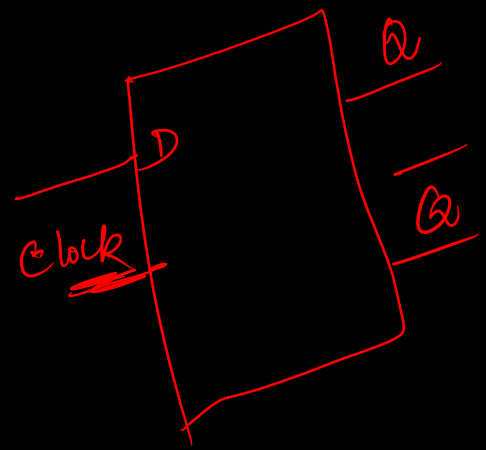
Characteristic equation

$Q_{t+1} = D$

D latch

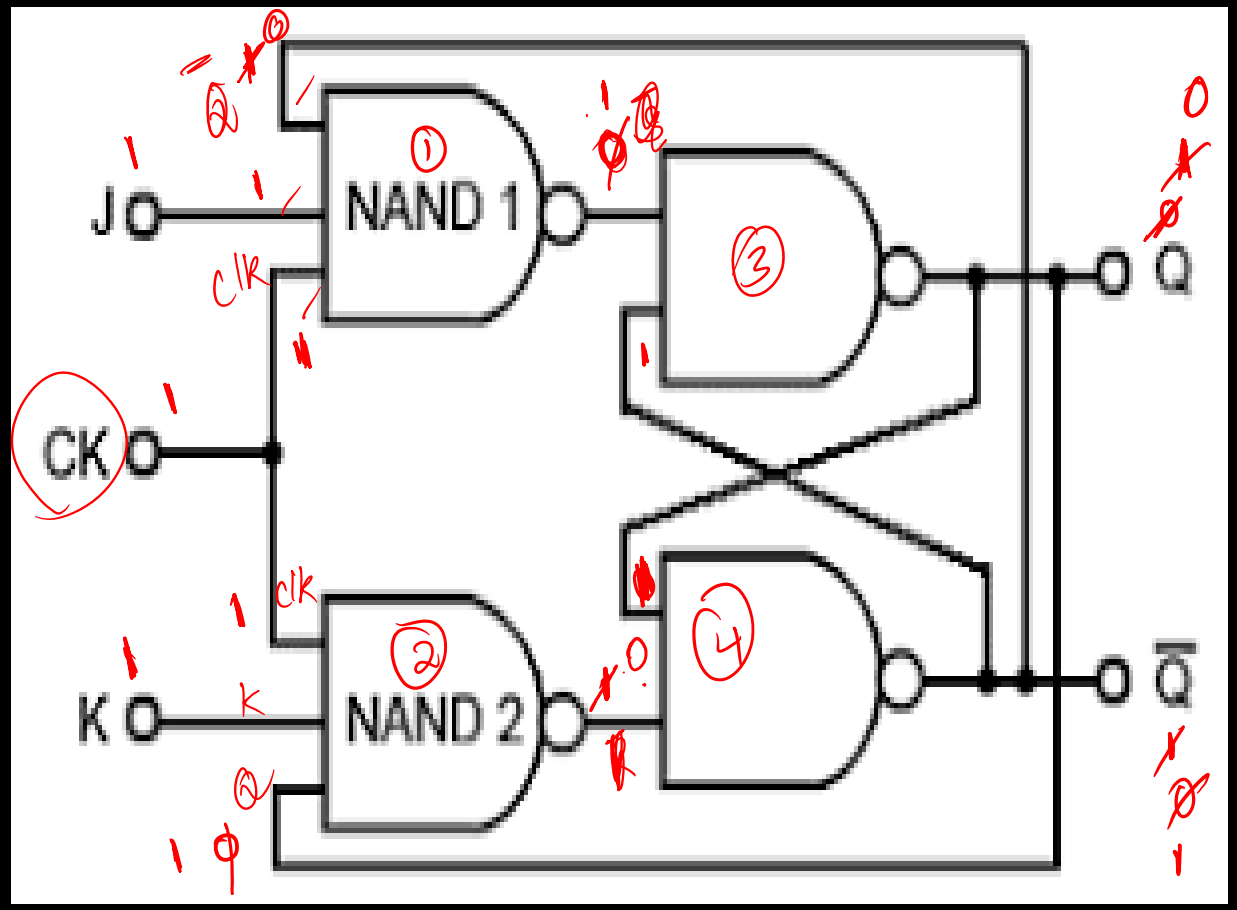
Next state = I/P





Race around condition

Jk Latch ⇒ SR latch is modified so that the indeterminate is determined



$J = S$ ⇒ Set i/p

$K = R$ ⇒ reset i/p

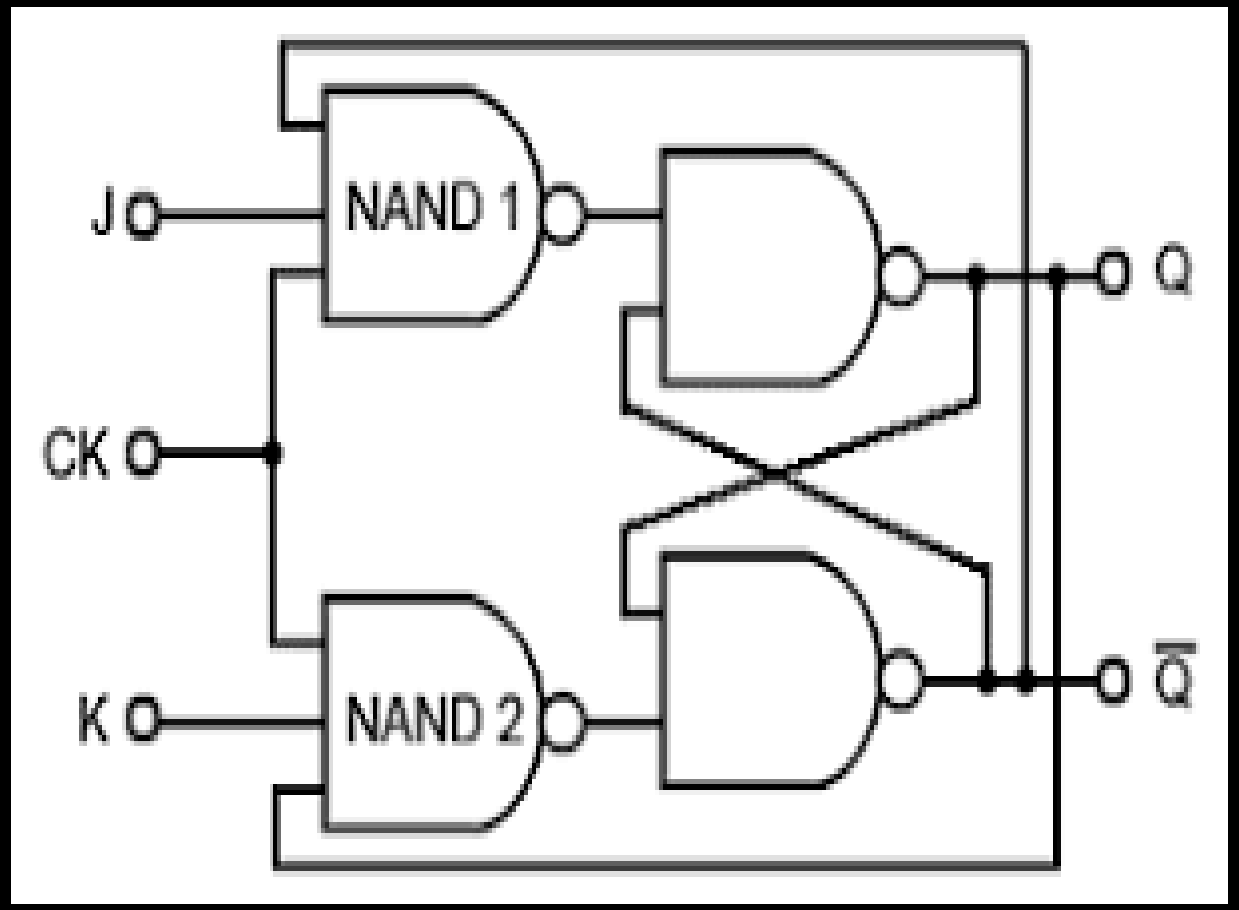
When both J & K are 1

Jk latch Switches to its Complement state that is

if $Q_t = 1$ $Q_{t+1} = 0$

$Q_t = 0$ $Q_{t+1} = 1$

Modified version of SR latch where the undefined state of both the i/ps being '1' is defined



Clock

J

K

Q

race around condition

Problem of latch

Clock

J

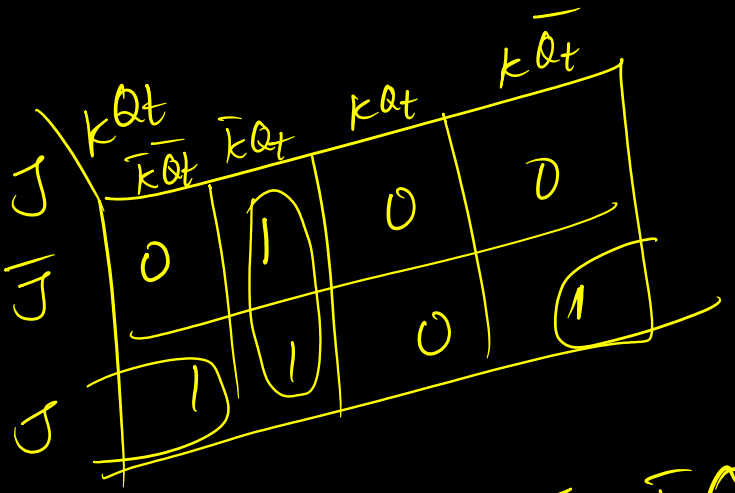
K

Q

toggling

complementing itself

Q_{t+1}



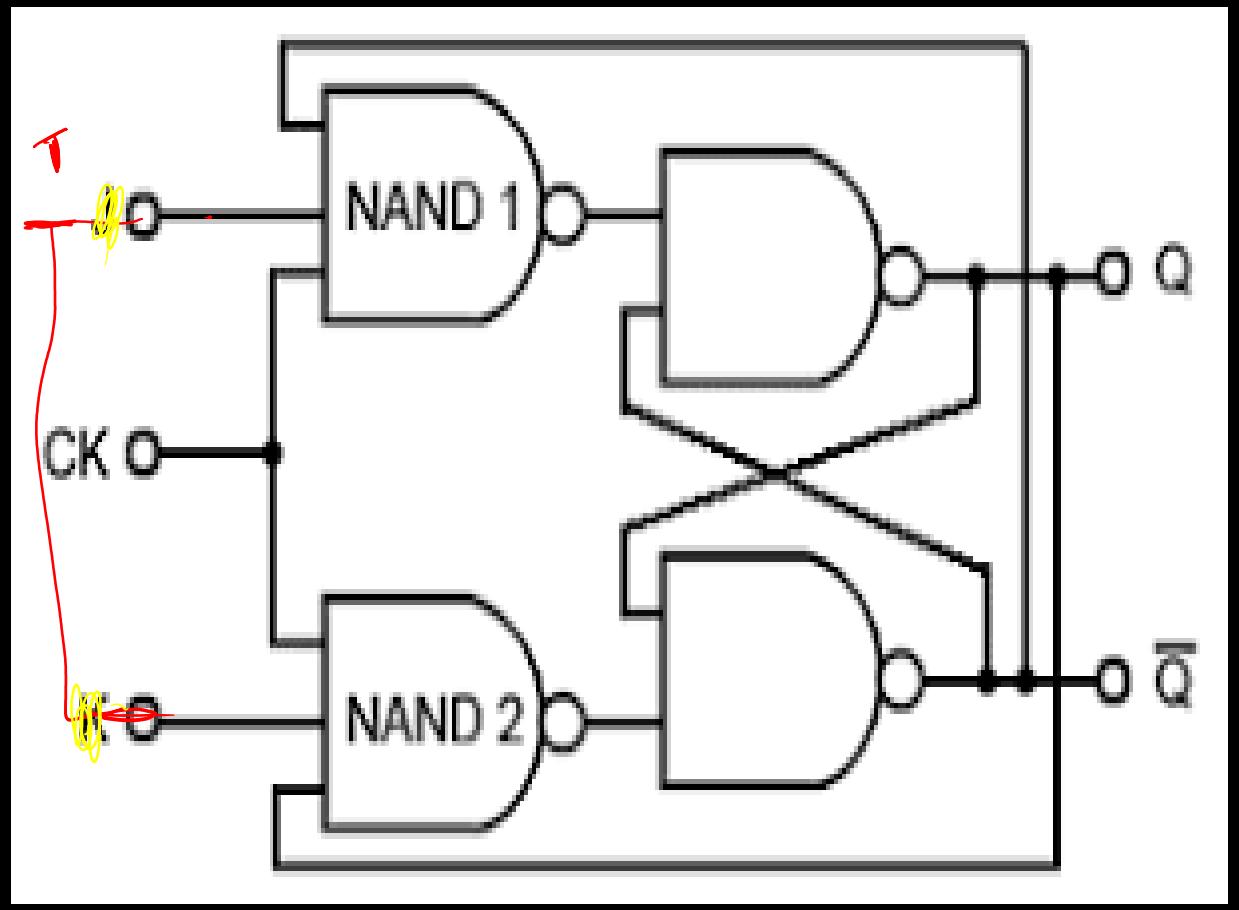
I/Ps		P.S	N.S	
J	K	Q_t	Q_{t+1}	
0	0	0	0	No change
0	0	1	1	
0	1	0	0	reset state
0	1	1	0	
1	0	0	1	set state
1	0	1	1	
1	1	0	1	Toggle
1	1	1	0	

J	K	Q_{t+1}
0	0	Q_t → No change
0	1	0 reset
1	0	1 set
1	1	Toggle

$Q_{t+1} = J\bar{Q}_t + \bar{K}Q_t$

Characteristic equation of JK latch

T latch



Both i/ps J & K are tied together & a single i/p T is obtained

$T \Rightarrow J = K$

$J=0\ K=0$

$J=1\ K=1$

Char. table

T	Q_t	Q_{t+1}	
0	0	0	No change
0	1	1	
1	0	1	Toggle
1	1	0	

T	Q_{t+1}	
0	Q_t	No change
1	$\bar{Q}_t$	Toggle

Char. eqn

$Q_{t+1} = \bar{T}Q_t + T\bar{Q}_t$