CS/ECE/EEE/INSTR F215:Digital Design

Lecture 22: *Flipflops*

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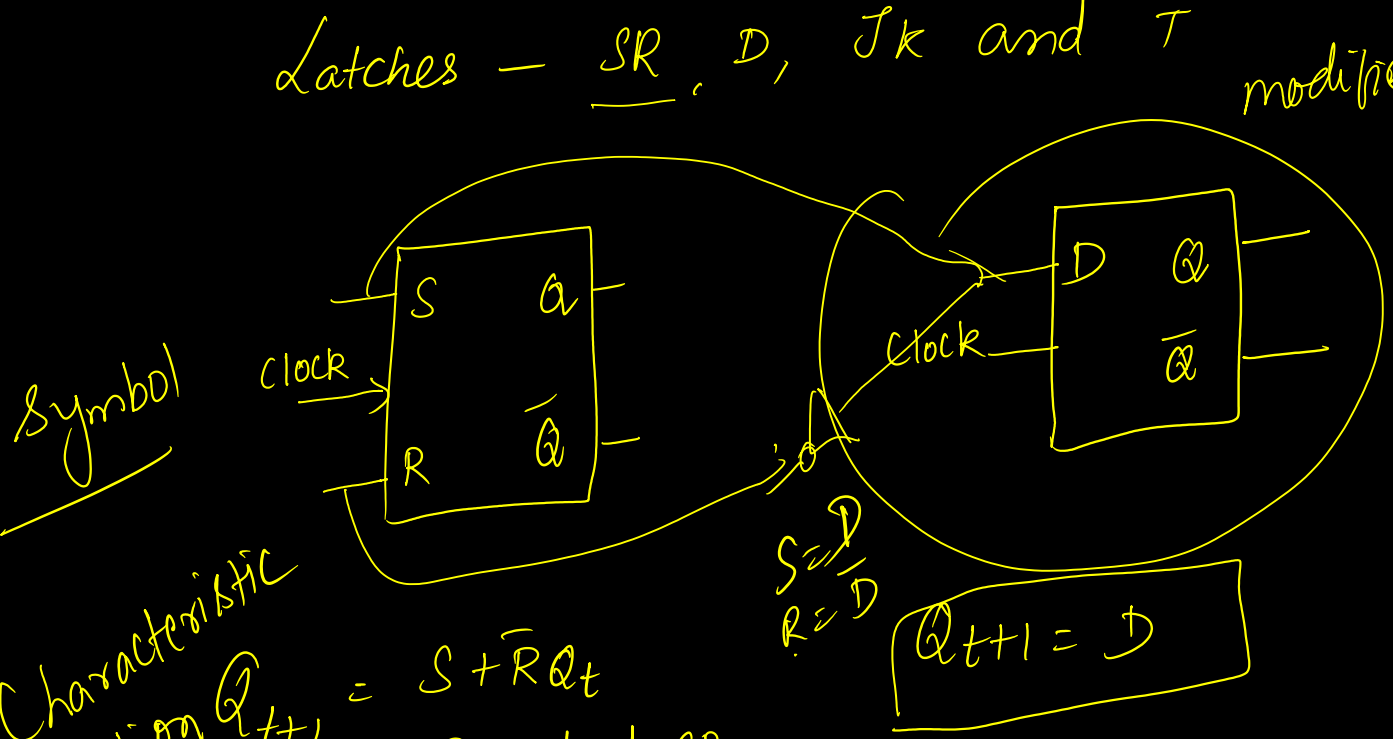
Our greatest weakness is giving up.
The most certain way to succeed
is always to try just one more time

- Thomas. A. Edison

Latches — SR, D, JK and T

modified

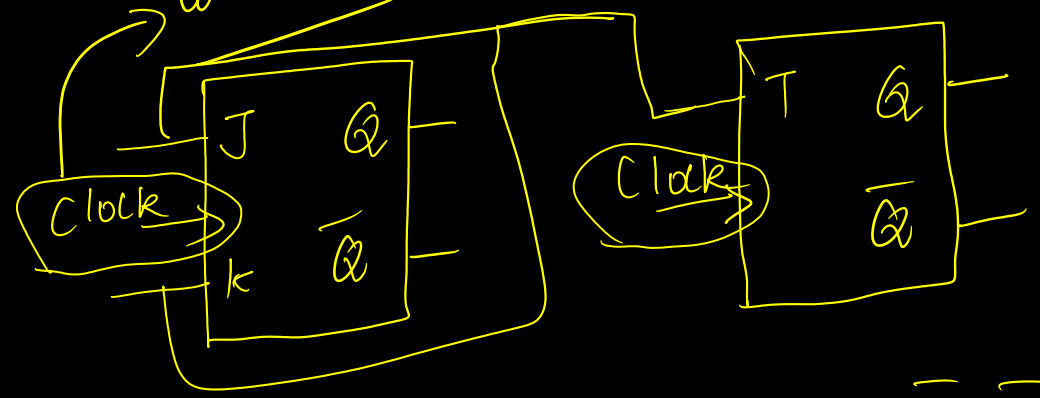


Characteristic equation $Q_{t+1} = S + \bar{R} Q_t$

Provided SR = 0

I/Ps S	R	P.S Q_t	N.S Q_{t+1}	
0	0	0	0	NC
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	X	Indeterminate avoided
1	1	1	X	

D	Q_t	Q_{t+1}
0	0	0
0	1	0
1	0	1
1	1	1



$Q_{t+1} = J\bar{Q}_t + \bar{K} Q_t$

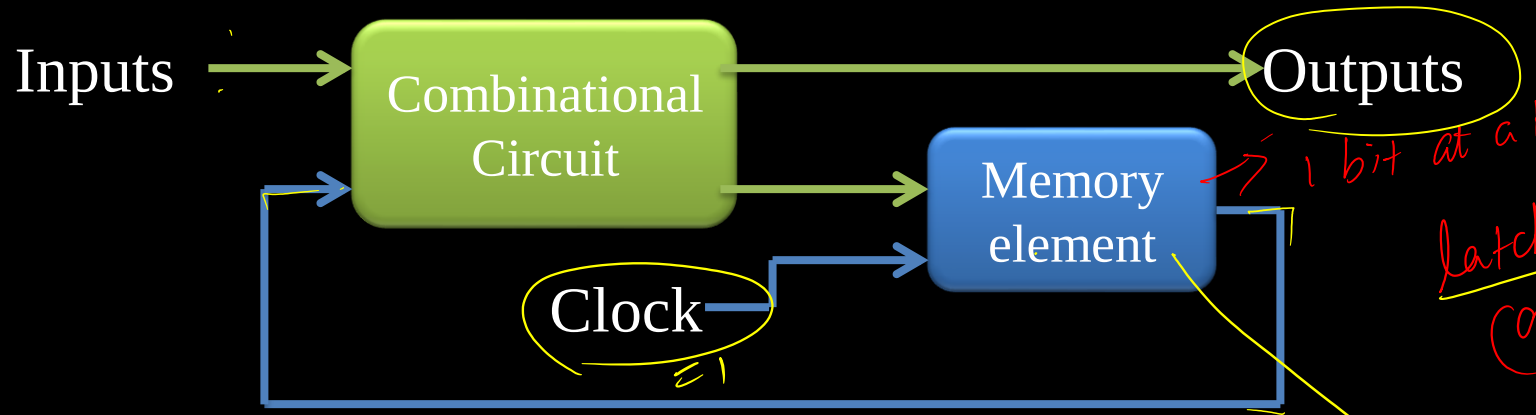
$Q_{t+1} = T\bar{Q}_t + \bar{T} Q_t$

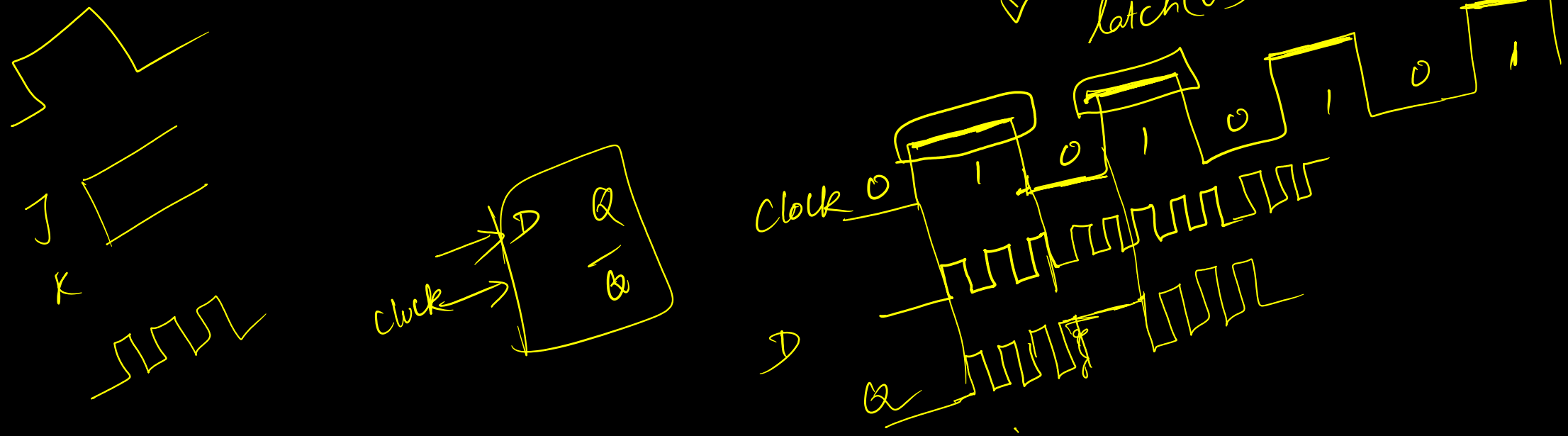
Clock J	K	Q_t	Q_{t+1}	
0	0	0	0	NC
0	0	1	1	
0	1	0	0	reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	1	toggle
1	1	1	0	

P.S

T	Q_t	Q_{t+1}	
0	0	0	NC
0	1	1	
1	0	1	Toggle
1	1	0	

Sequential Circuit





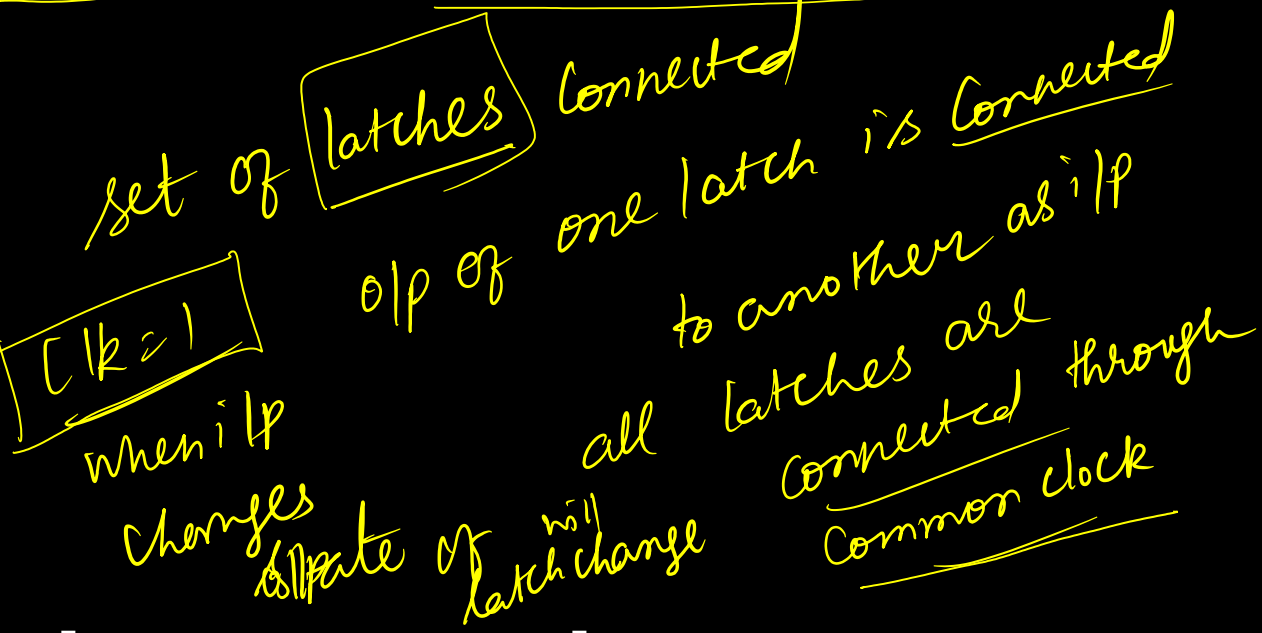
Latches are level sensitive, state transitions of latches start as soon as clock appears

As the output is connected to input of latches through combinational circuit

If input changes while the clock is still '1', the latches respond and give new o/p

Latches are "transparent" (any change on the inputs is seen at the outputs immediately).

This causes synchronization problems!

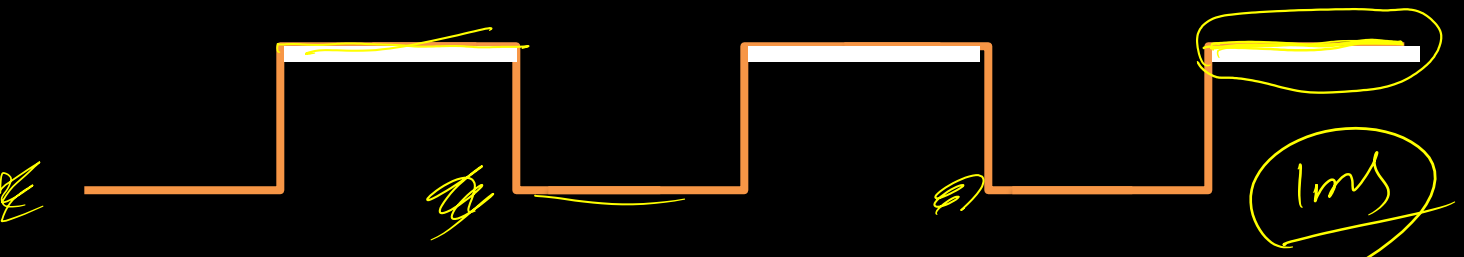


Unpredictable Behaviour –

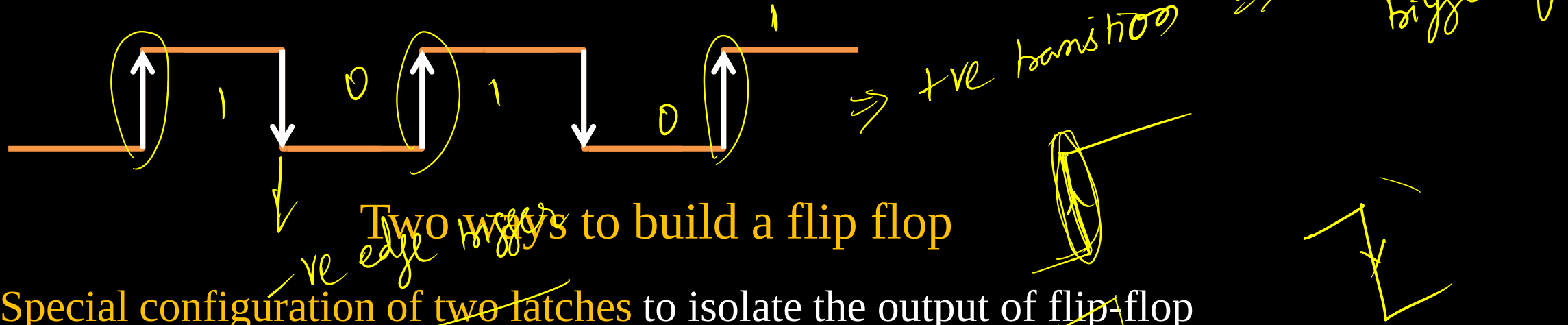
Solution: Use latches to create flip-flops that can Respond ONLY on SPECIFIC times

Sequential Circuits

Latch – Responds to change in level of clock pulse



The key to the proper operation of a flip flop is to trigger it only during signal transition.



Two ways to build a flip flop

Special configuration of two latches to isolate the output of flip-flop

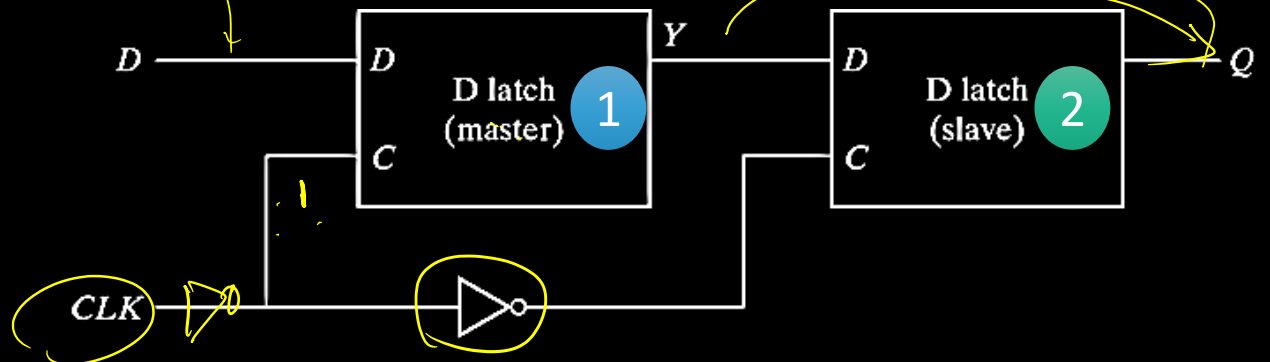
Gate based design which triggers only during signal transition of clock and is disabled during rest of clock pulse

Latch ⇒ (ff) ⇒ State change will occur only during Clock transition

how can we modify

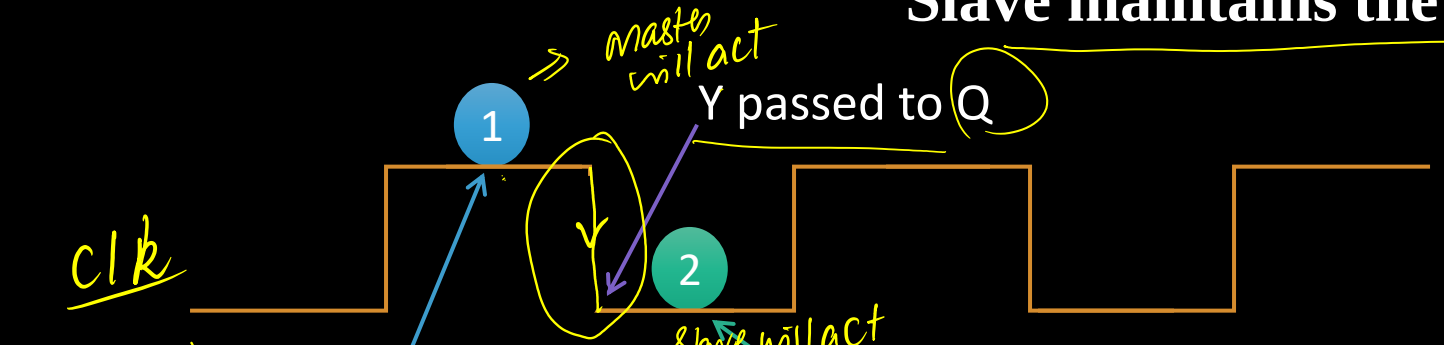
2 latches ⇒ o/p of the latch

Master Slave Configuration



What happens when CLK is logic 1

Master enabled and slave disabled
Slave maintains the output



If D changes

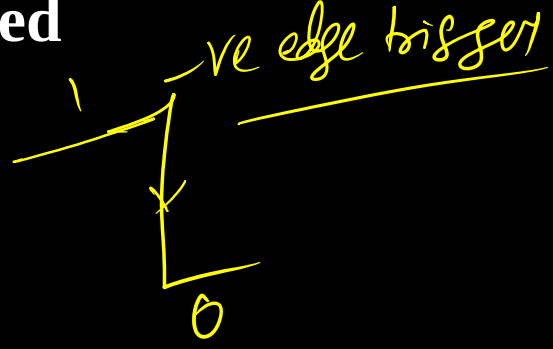
Y will be affected and not Q

Clock is 0

If D changes

Y remains unaffected and Q stable

Q = Y

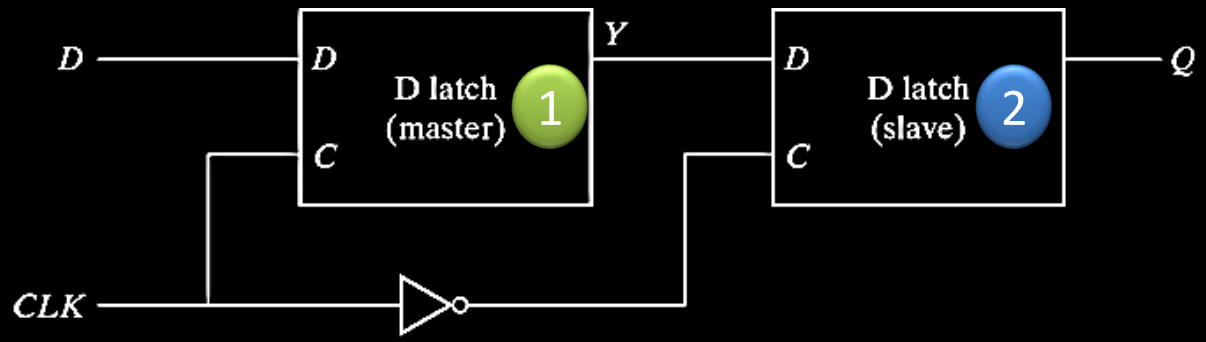


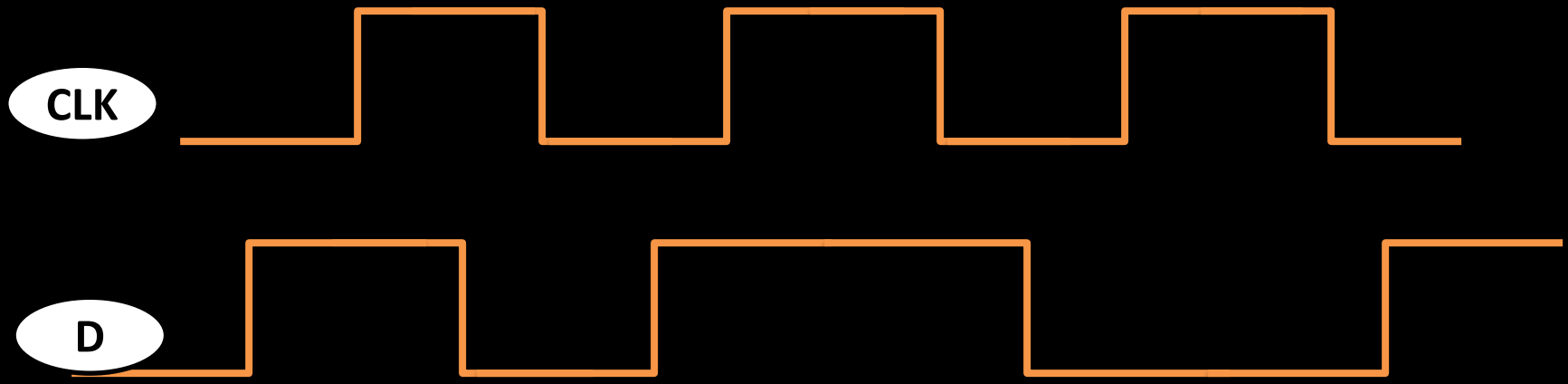
master is disabled

-ve Edge Triggered

+ve edge triggered

Master Slave Flip-flop





Edge Triggered D Flip-Flops

Master Slave Flip-flop