BIRLA INSTITUTE OF SCIENCE AND TECHNOLOGY PILANI, HYDERABAD CAMPUS

DIGITAL DESIGN LABORATORY (Session 2021-22)

Workbook

Experiment -6

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Complete ID of the student: 2020A7PS2081H

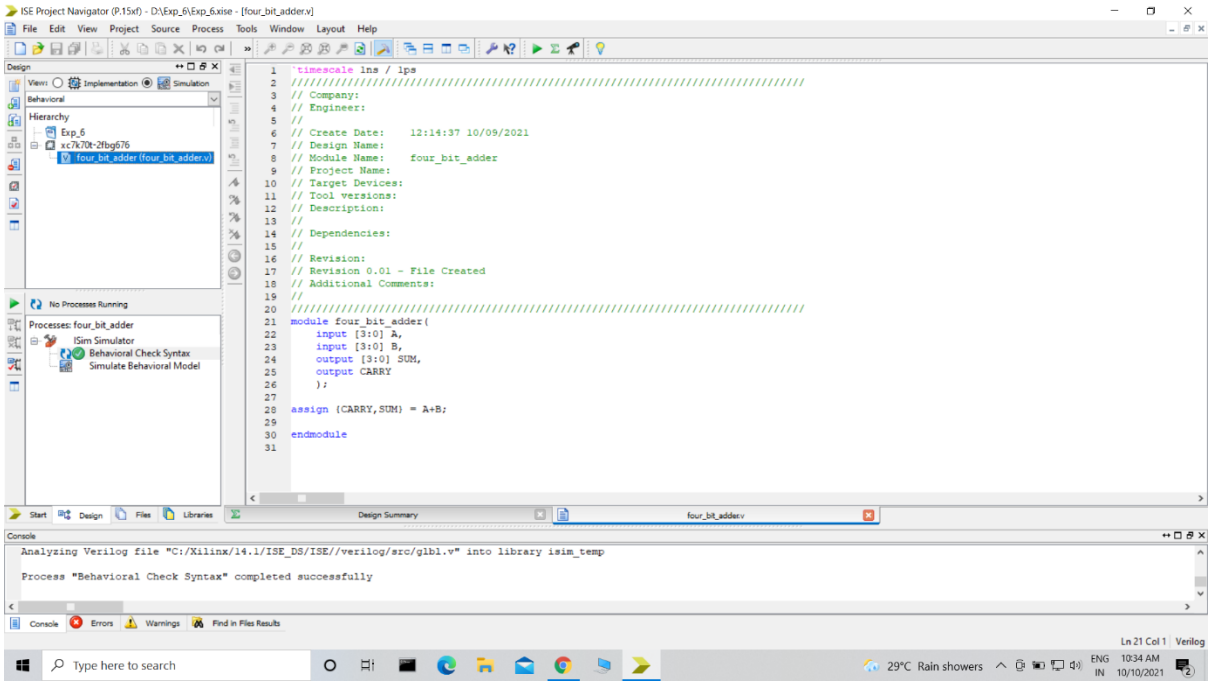
Title of Experiment: Dataflow Modelling Implementation of 4-Bit Adder & BCD Adder in Xilinx ISE

Problem 1:

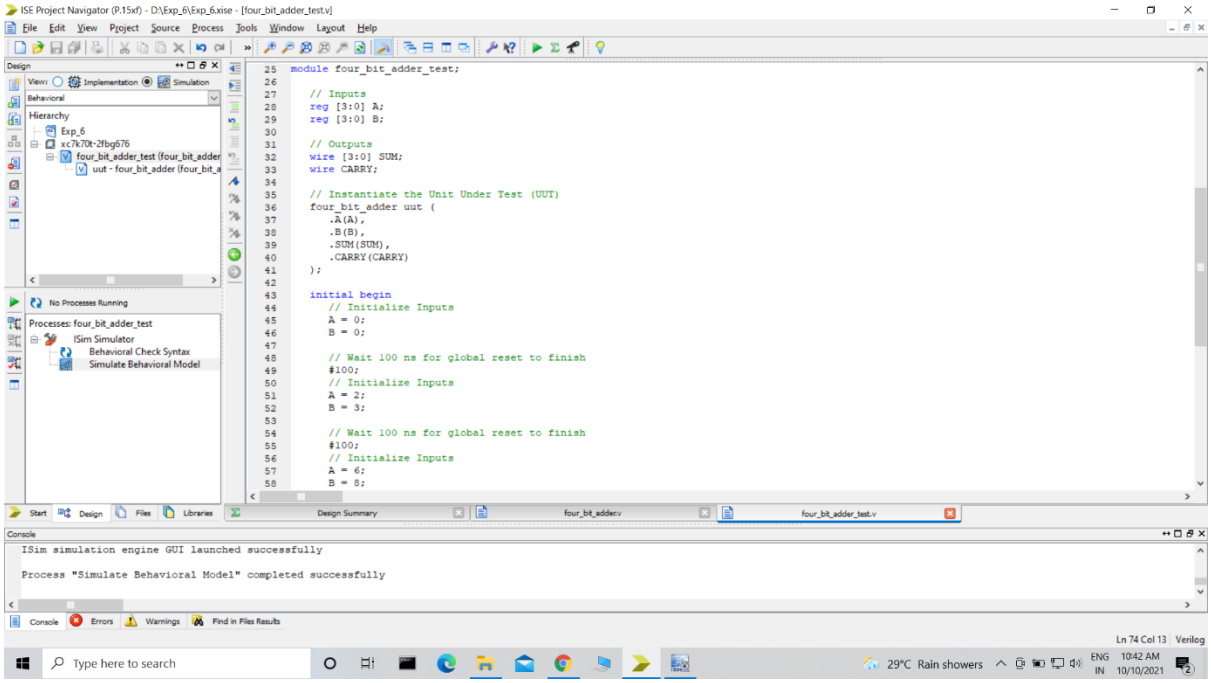
Implement the 4-bit Adder circuit using Xilinx ISE

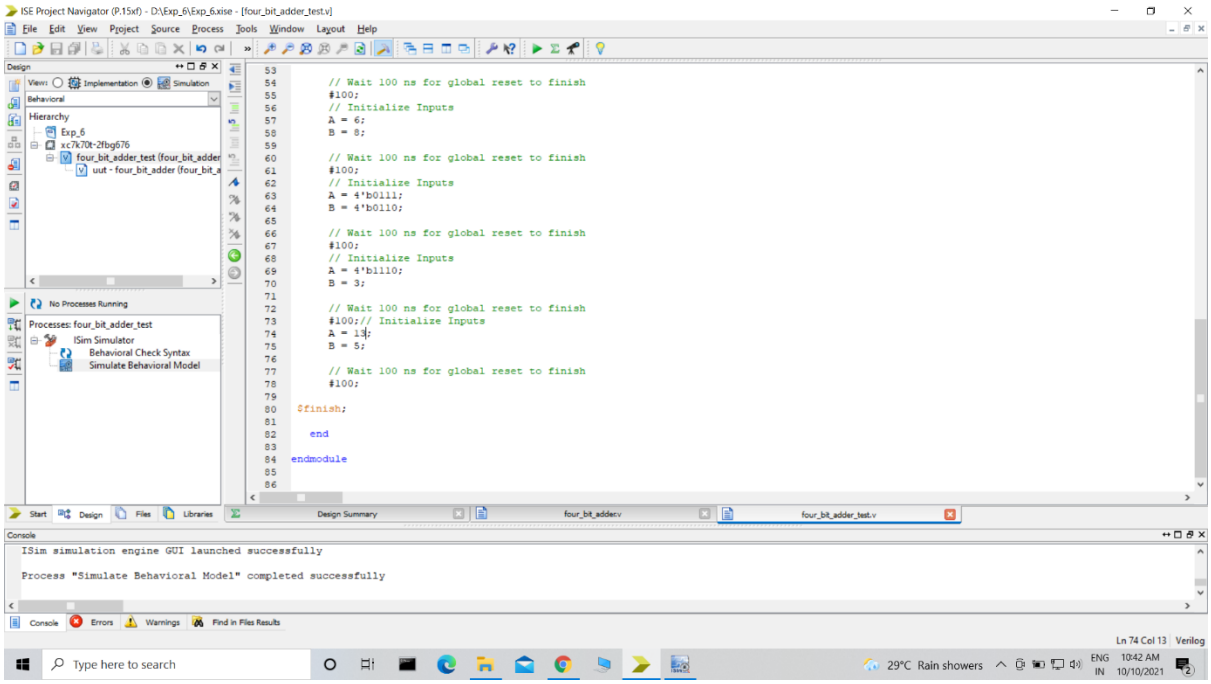
(Provide proper snapshots and Show the graphical output)

Code:

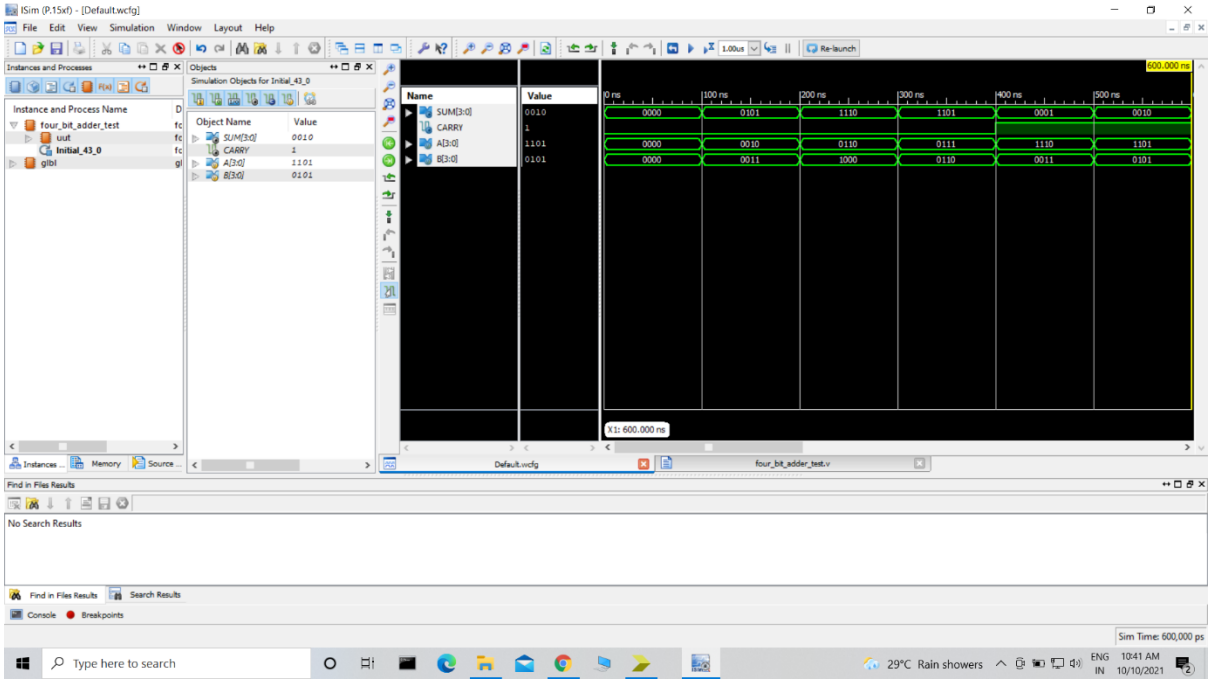


Test Bench:


ISE Project Navigator (P.15xf) - D:\Exp_6\Exp_6.xise - [four_bit_adder_test.v]
File Edit View Project Source Process Tools Window Layout Help
Hierarchy
Exp_6
xc7k70t-2fbg676
four_bit_adder_test (four_bit_adder
uut - four_bit_adder (four_bit_a
Processes: four_bit_adder_test
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
module four_bit_adder_test;
// Inputs
reg [3:0] A;
reg [3:0] B;
// Outputs
wire [3:0] SUM;
wire CARRY;
// Instantiate the Unit Under Test (UUT)
four_bit_adder uut (
.A(A),
.B(B),
.SUM(SUM),
.CARRY(CARRY)
);
initial begin
// Initialize Inputs
A = 0;
B = 0;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 2;
B = 3;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 6;
B = 8;
ISim simulation engine GUI launched successfully
Process "Simulate Behavioral Model" completed successfully
Console Errors Warnings Find in Files Results
Ln 74 Col 13 Verilog
Type here to search
29°C Rain showers
ENG IN 10:42 AM 10/10/2021


ISE Project Navigator (P.15xf) - D:\Exp_6\Exp_6.xise - [four_bit_adder_test.v]
File Edit View Project Source Process Tools Window Layout Help
Hierarchy
Exp_6
xc7k70t-2fbg676
four_bit_adder_test (four_bit_adder
uut - four_bit_adder (four_bit_a
Processes: four_bit_adder_test
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 6;
B = 8;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 4'b0111;
B = 4'b0110;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 4'b1110;
B = 3;
// Wait 100 ns for global reset to finish
#100;// Initialize Inputs
A = 13;
B = 5;
// Wait 100 ns for global reset to finish
#100;
$finish;
end
endmodule
ISim simulation engine GUI launched successfully
Process "Simulate Behavioral Model" completed successfully
Console Errors Warnings Find in Files Results
Ln 74 Col 13 Verilog
Type here to search
29°C Rain showers
ENG IN 10:42 AM 10/10/2021

Graph:

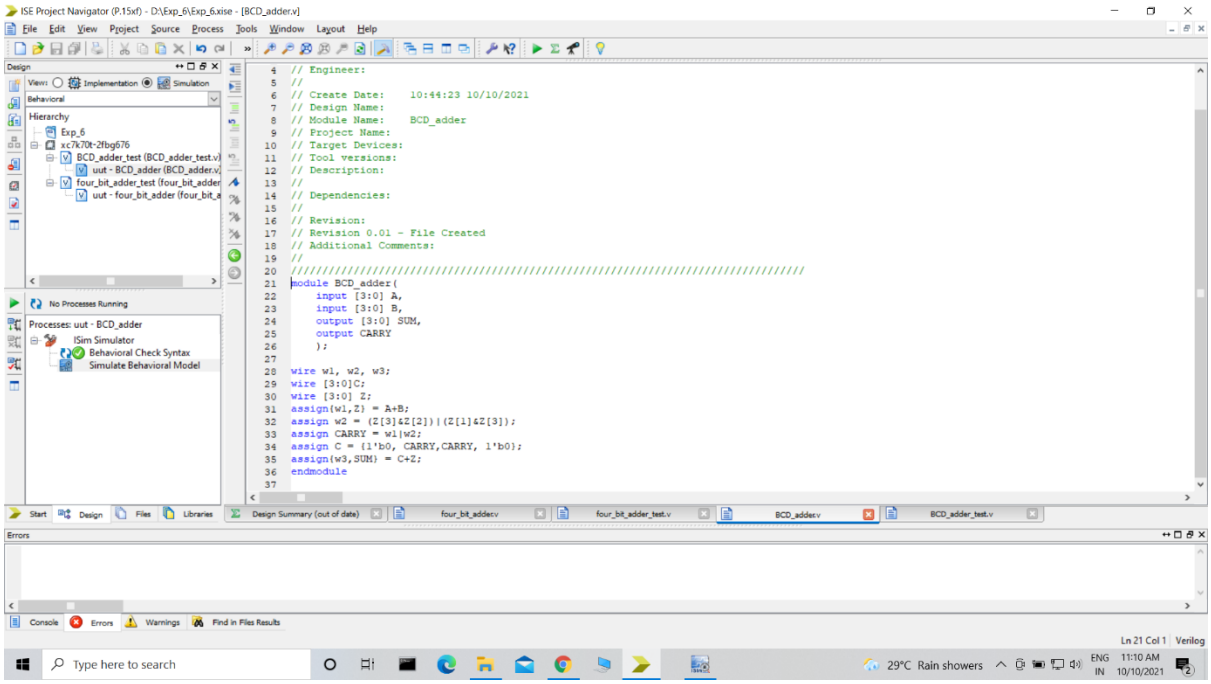


Problem 2:

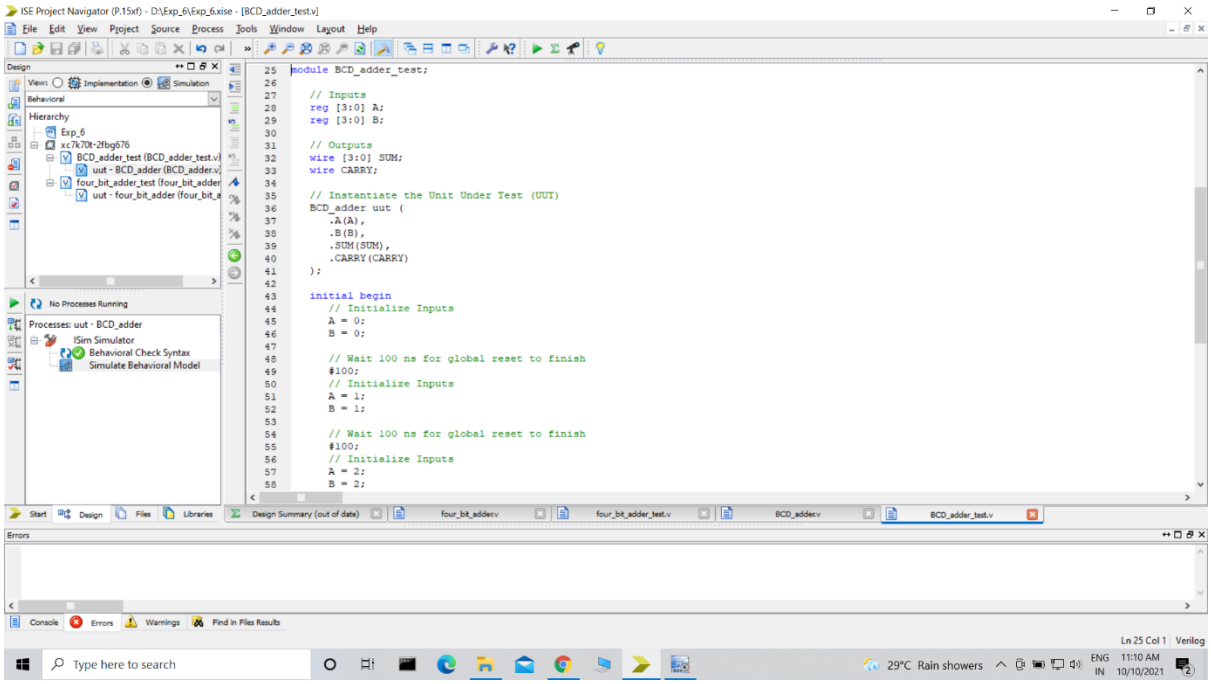
Implement BCD Adder using 4-bit Adder in Xilinx ISE

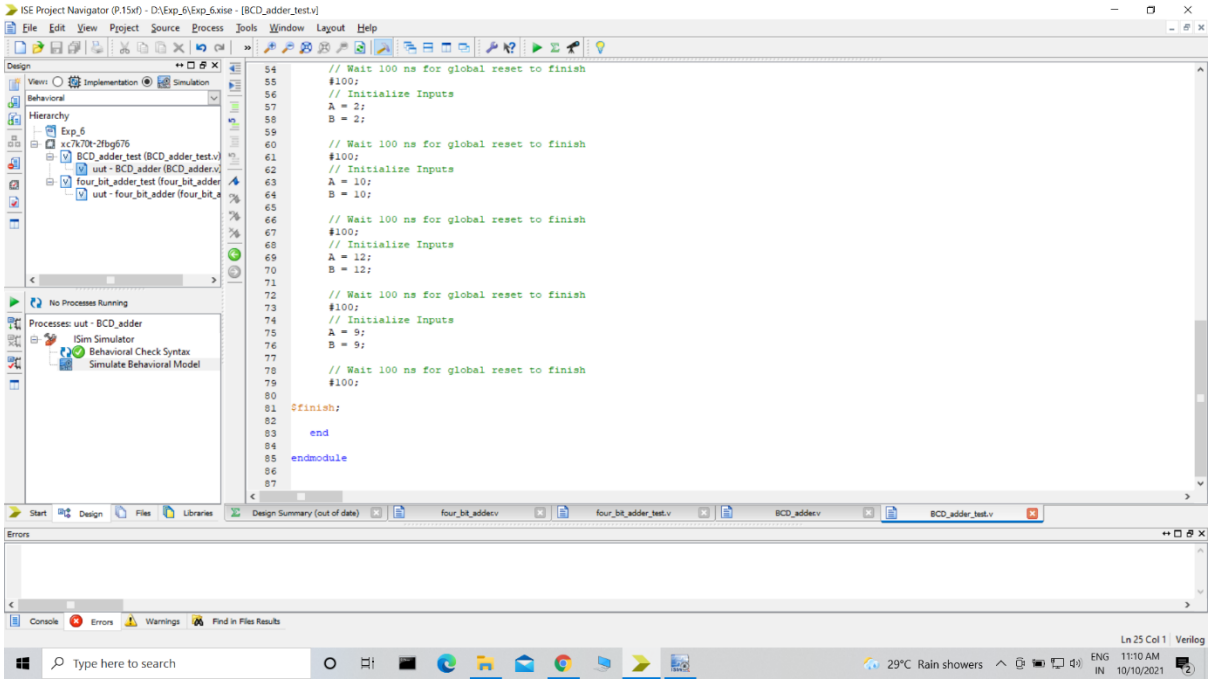
(Provide proper snapshots and show the graphical output)

Code:

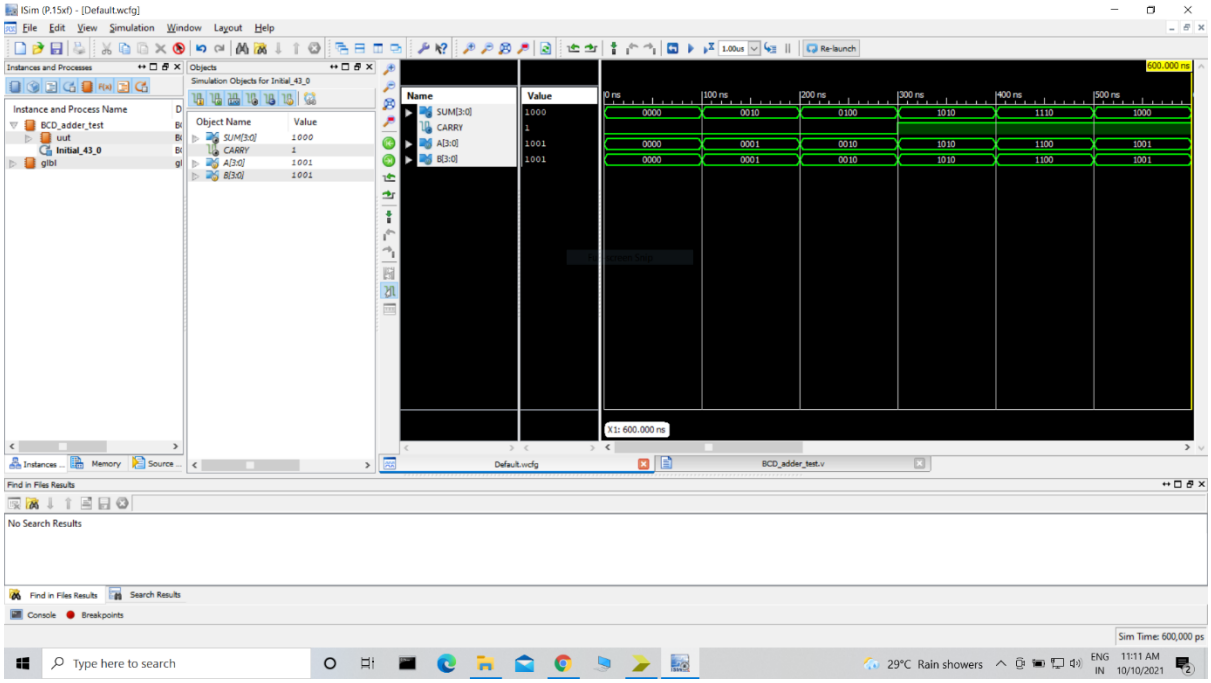

ISE Project Navigator (P.15xf) - D:\Exp_6\Exp_6.xise - [BCD_adder.v]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
Exp_6
xc7k70t-2fbg676
BCD_adder_test (BCD_adder_test.v)
uut - BCD_adder (BCD_adder.v)
four_bit_adder_test (four_bit_adder
uut - four_bit_adder (four_bit_a
No Processes Running
Processes: uut - BCD_adder
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
// Engineer:
//
// Create Date: 10:44:23 10/10/2021
// Design Name:
// Module Name: BCD_adder
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
module BCD_adder(
input [3:0] A,
input [3:0] B,
output [3:0] SUM,
output CARRY
);
wire w1, w2, w3;
wire [3:0]C;
wire [3:0] Z;
assign{w1,Z} = A+B;
assign w2 = (Z[3]&Z[2])|(Z[1]&Z[3]);
assign CARRY = w1|w2;
assign C = {1'b0, CARRY,CARRY, 1'b0};
assign{w3,SUM} = C+Z;
endmodule
Errors
Console Errors Warnings Find in Files Results
Ln 21 Col 1 Verilog
Type here to search
29°C Rain showers
ENG IN 11:10 AM 10/10/2021

Test Bench:


ISE Project Navigator (P.15xf) - D:\Exp_6\Exp_6.xise - [BCD_adder_test.v]
File Edit View Project Source Process Tools Window Layout Help
Hierarchy
Exp_6
xc7k70t-2fbg676
BCD_adder_test (BCD_adder_test.v)
uut - BCD_adder (BCD_adder.v)
four_bit_adder_test (four_bit_adder
uut - four_bit_adder (four_bit_a
Processes: uut - BCD_adder
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
module BCD_adder_test;
// Inputs
reg [3:0] A;
reg [3:0] B;
// Outputs
wire [3:0] SUM;
wire CARRY;
// Instantiate the Unit Under Test (UUT)
BCD_adder uut (
.A(A),
.B(B),
.SUM(SUM),
.CARRY(CARRY)
);
initial begin
// Initialize Inputs
A = 0;
B = 0;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 1;
B = 1;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 2;
B = 2;
Type here to search
29°C Rain showers
ENG IN
11:10 AM
10/10/2021


ISE Project Navigator (P.15xf) - D:\Exp_6\Exp_6.xise - [BCD_adder_test.v]
File Edit View Project Source Process Tools Window Layout Help
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 2;
B = 2;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 10;
B = 10;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 12;
B = 12;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 9;
B = 9;
// Wait 100 ns for global reset to finish
#100;
$finish;
end
endmodule
Type here to search
29°C Rain showers
ENG IN
11:10 AM
10/10/2021

Graph:

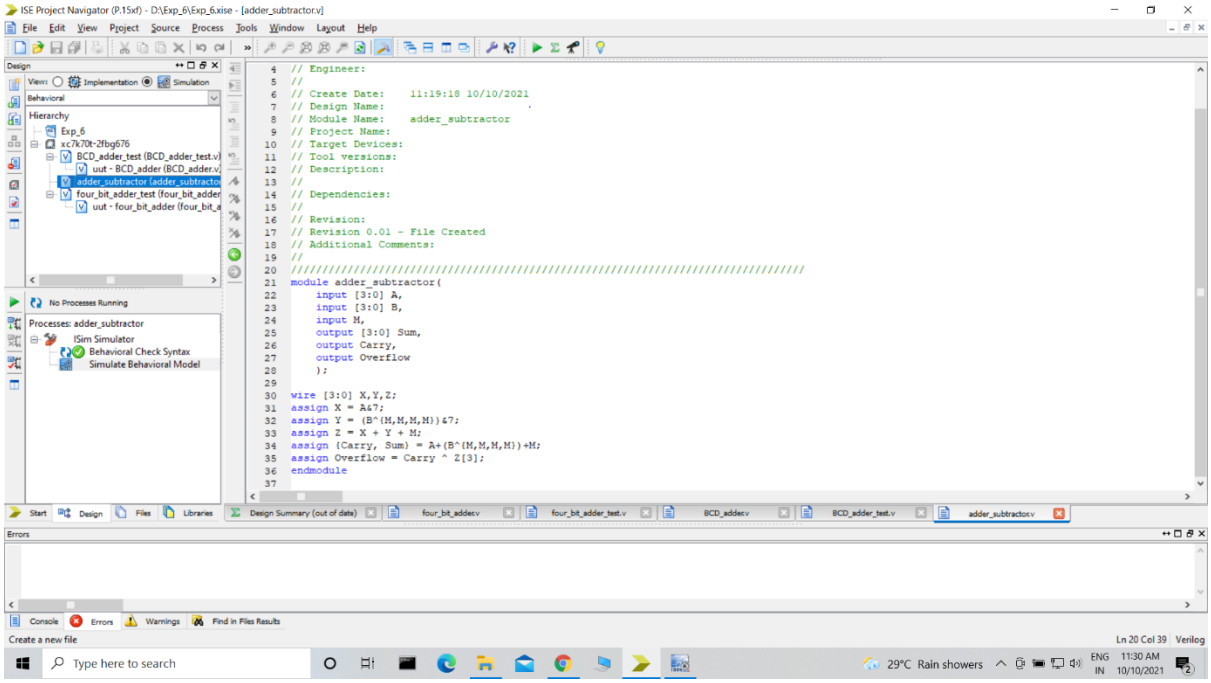

ISim (P.15xf) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Instances and Processes
Objects
Simulation Objects for Initial_43_0
Instance and Process Name
BCD_adder_test
uut
Initial_43_0
glbl
Object Name
Value
SUM[3:0]
CARRY
A[3:0]
B[3:0]
Name
Value
1000
1
1001
1001
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600.000 ns
0000
0010
0100
1010
1110
1000
0000
0001
0010
1010
1100
1001
0000
0001
0010
1010
1100
1001
X1: 600.000 ns
Default.wcfg
BCD_adder_test.v
Find in Files Results
No Search Results
Console
Breakpoints
Sim Time: 600,000 ps
Type here to search
29°C Rain showers
ENG
IN
11:11 AM
10/10/2021

Problem 3:

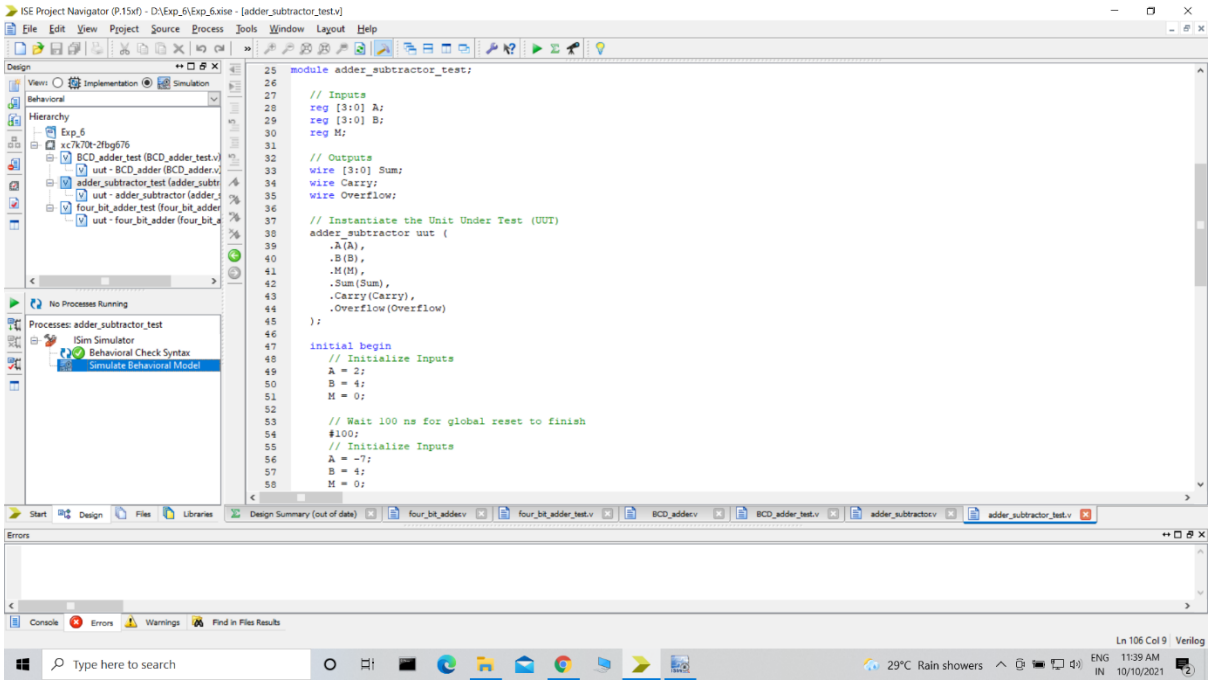
Implement 4-bit BCD Adder-Subtractor in Xilinx ISE

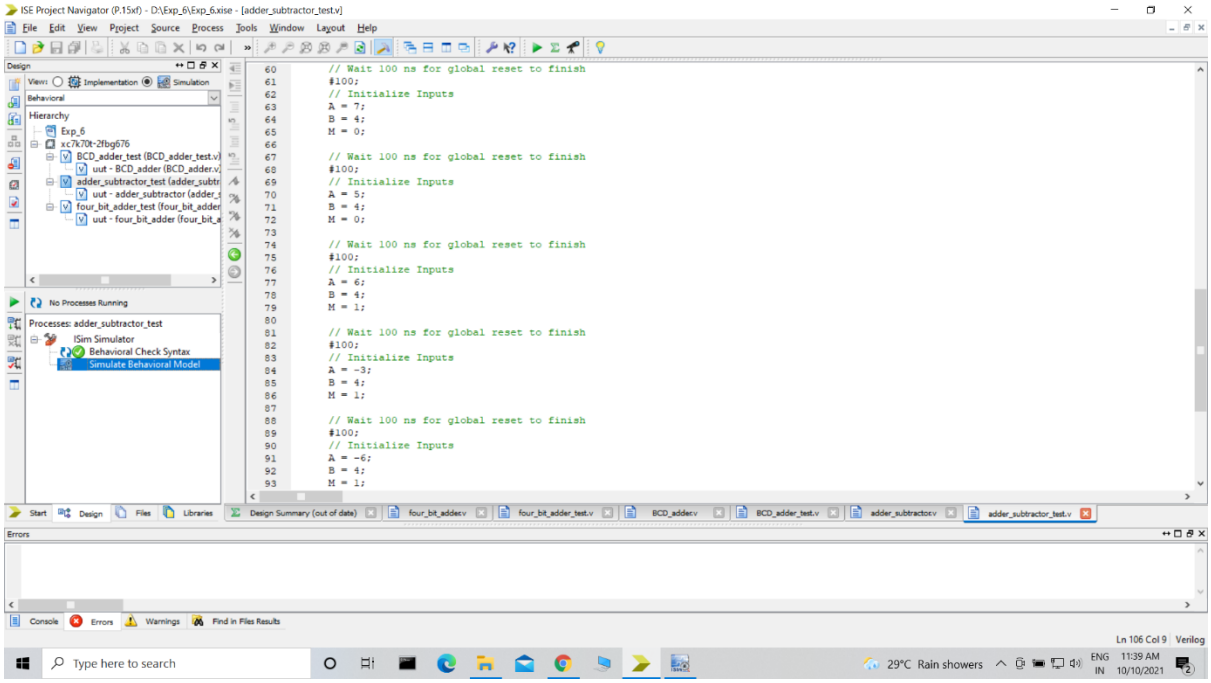
(Provide proper snapshots and show the graphical output)

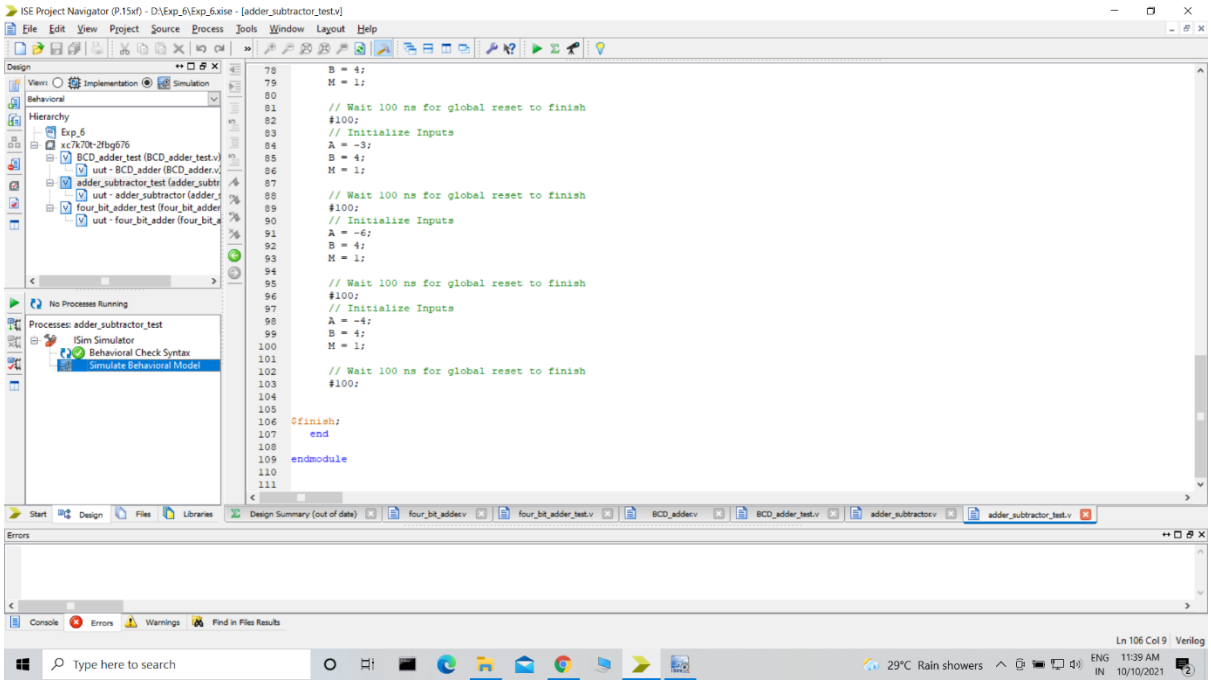
Code:



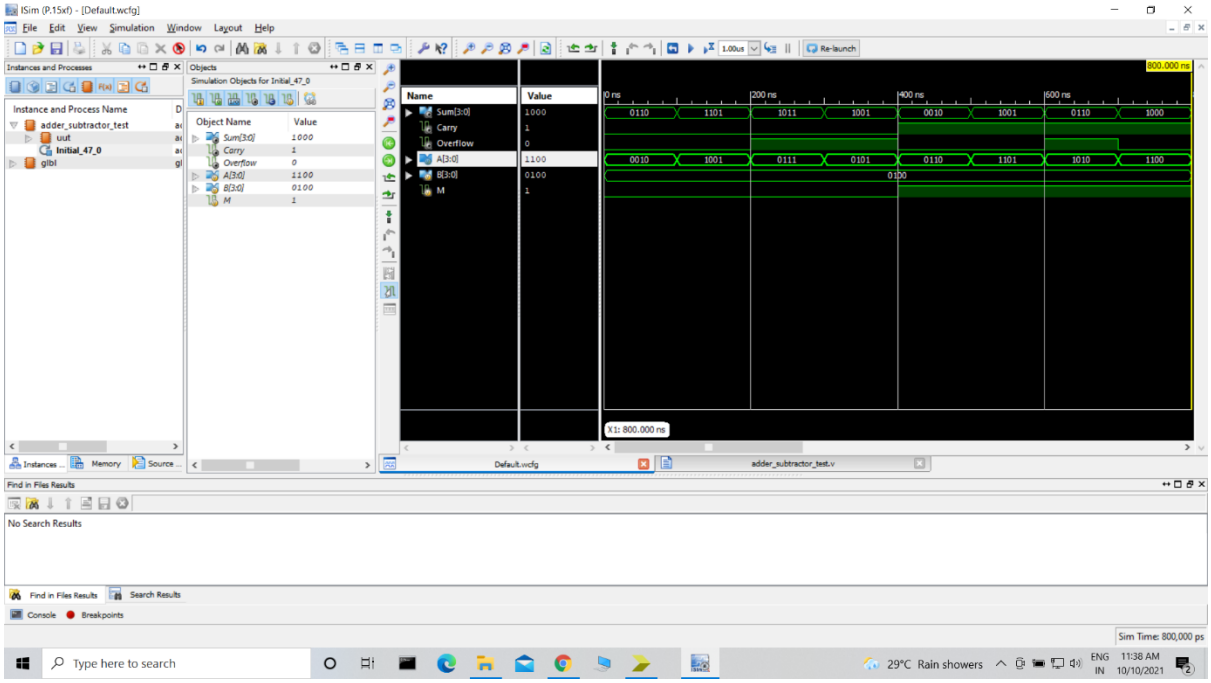
Test Bench:


ISE Project Navigator (P.15xf) - D:\Exp_6\Exp_6.xise - [adder_subtractor_test.v]
File Edit View Project Source Process Tools Window Layout Help
Hierarchy
Exp_6
xc7k70t-2fbg676
BCD_adder_test (BCD_adder_test.v)
uut - BCD_adder (BCD_adder.v)
adder_subtractor_test (adder_subtr
uut - adder_subtractor (adder_
four_bit_adder_test (four_bit_adder
uut - four_bit_adder (four_bit_a
No Processes Running
Processes: adder_subtractor_test
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
module adder_subtractor_test;
// Inputs
reg [3:0] A;
reg [3:0] B;
reg M;
// Outputs
wire [3:0] Sum;
wire Carry;
wire Overflow;
// Instantiate the Unit Under Test (UUT)
adder_subtractor uut (
.A(A),
.B(B),
.M(M),
.Sum(Sum),
.Carry(Carry),
.Overflow(Overflow)
);
initial begin
// Initialize Inputs
A = 2;
B = 4;
M = 0;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = -7;
B = 4;
M = 0;
Design Summary (out of date)
four_bit_adder.v
four_bit_adder_test.v
BCD_adder.v
BCD_adder_test.v
adder_subtractor.v
adder_subtractor_test.v
Errors
Console
Warnings
Find in Files Results
Ln 106 Col 9
Verilog
Type here to search
29°C Rain showers
ENG IN
11:39 AM
10/10/2021


ISE Project Navigator (P.15xf) - D:\Exp_6\Exp_6.xise - [adder_subtractor_test.v]
File Edit View Project Source Process Tools Window Layout Help
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 7;
B = 4;
M = 0;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 5;
B = 4;
M = 0;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = 6;
B = 4;
M = 1;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = -3;
B = 4;
M = 1;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = -6;
B = 4;
M = 1;
Ln 106 Col 9
Verilog
Type here to search
29°C Rain showers
ENG IN
11:39 AM
10/10/2021


ISE Project Navigator (P.15xf) - D:\Exp_6\Exp_6.xise - [adder_subtractor_test.v]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
Exp_6
xc7k70t-2fbg676
BCD_adder_test (BCD_adder_test.v)
uut - BCD_adder (BCD_adder.v)
adder_subtractor_test (adder_subtr
uut - adder_subtractor (adder_
four_bit_adder_test (four_bit_adder
uut - four_bit_adder (four_bit_a
No Processes Running
Processes: adder_subtractor_test
ISim Simulator
Behavioral Check Syntax
Simulate Behavioral Model
B = 4;
M = 1;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = -3;
B = 4;
M = 1;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = -6;
B = 4;
M = 1;
// Wait 100 ns for global reset to finish
#100;
// Initialize Inputs
A = -4;
B = 4;
M = 1;
// Wait 100 ns for global reset to finish
#100;
$finish;
end
endmodule
Design Summary (out of date)
four_bit_adder.v
four_bit_adder_test.v
BCD_adder.v
BCD_adder_test.v
adder_subtractor.v
adder_subtractor_test.v
Errors
Console Errors Warnings Find in Files Results
Ln 106 Col 9 Verilog
Type here to search
29°C Rain showers
ENG IN 11:39 AM 10/10/2021

Graph:


ISim (P.15xf) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Instances and Processes
Objects
Simulation Objects for Initial_47_0
Instance and Process Name
adder_subtractor_test
uut
Initial_47_0
glbl
Object Name
Value
Sum[3:0]
Carry
Overflow
A[3:0]
B[3:0]
M
Name
Value
0 ns
200 ns
400 ns
600 ns
800.000 ns
X1: 800.000 ns
Default.wcfg
adder_subtractor_test.v
Find in Files Results
No Search Results
Console
Breakpoints
Sim Time: 800,000 ps
Type here to search
29°C Rain showers
ENG IN
11:38 AM
10/10/2021