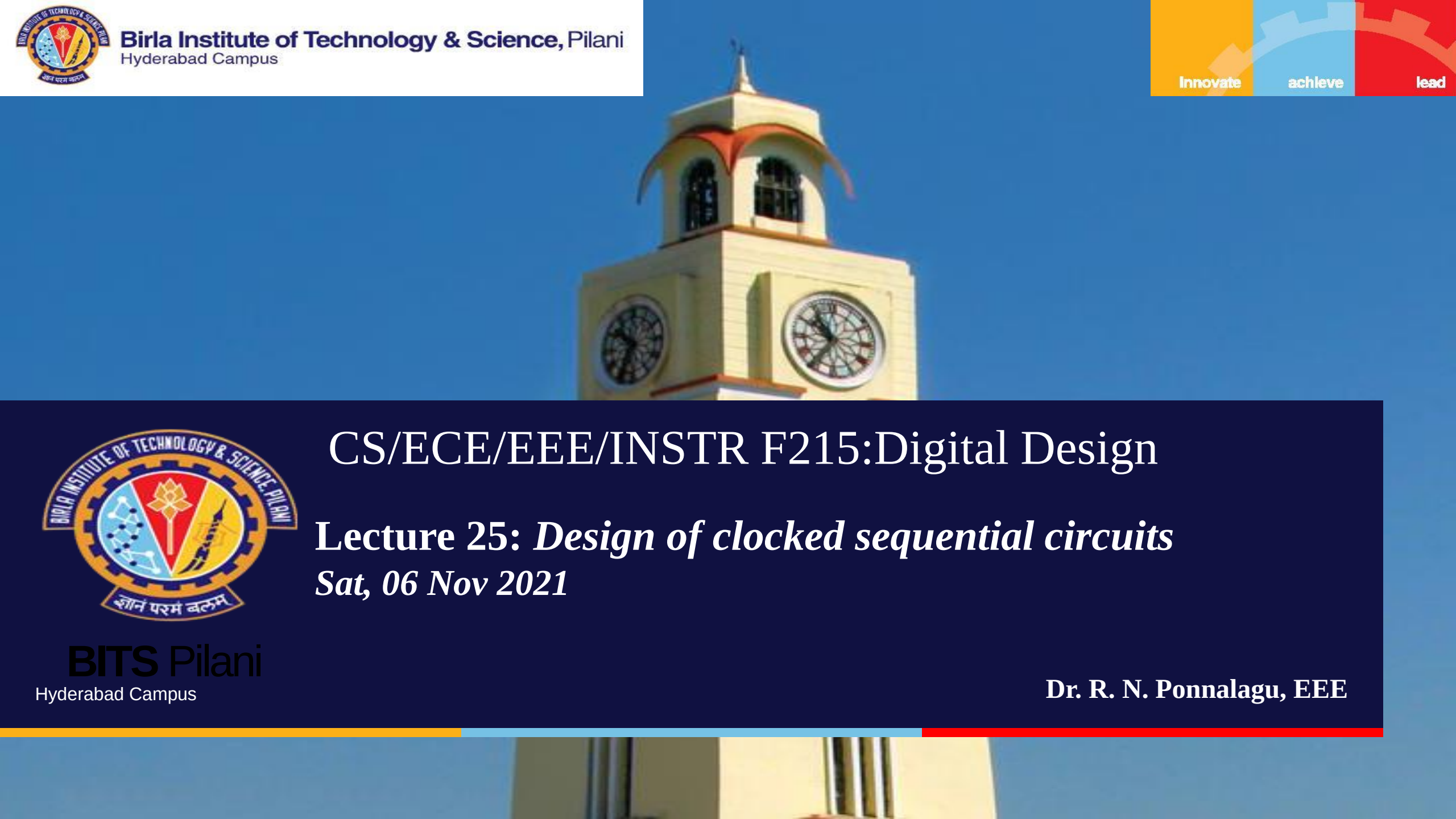


CS/ECE/EEE/INSTR F215:Digital Design

Lecture 25: *Design of clocked sequential circuits*

Sat, 06 Nov 2021

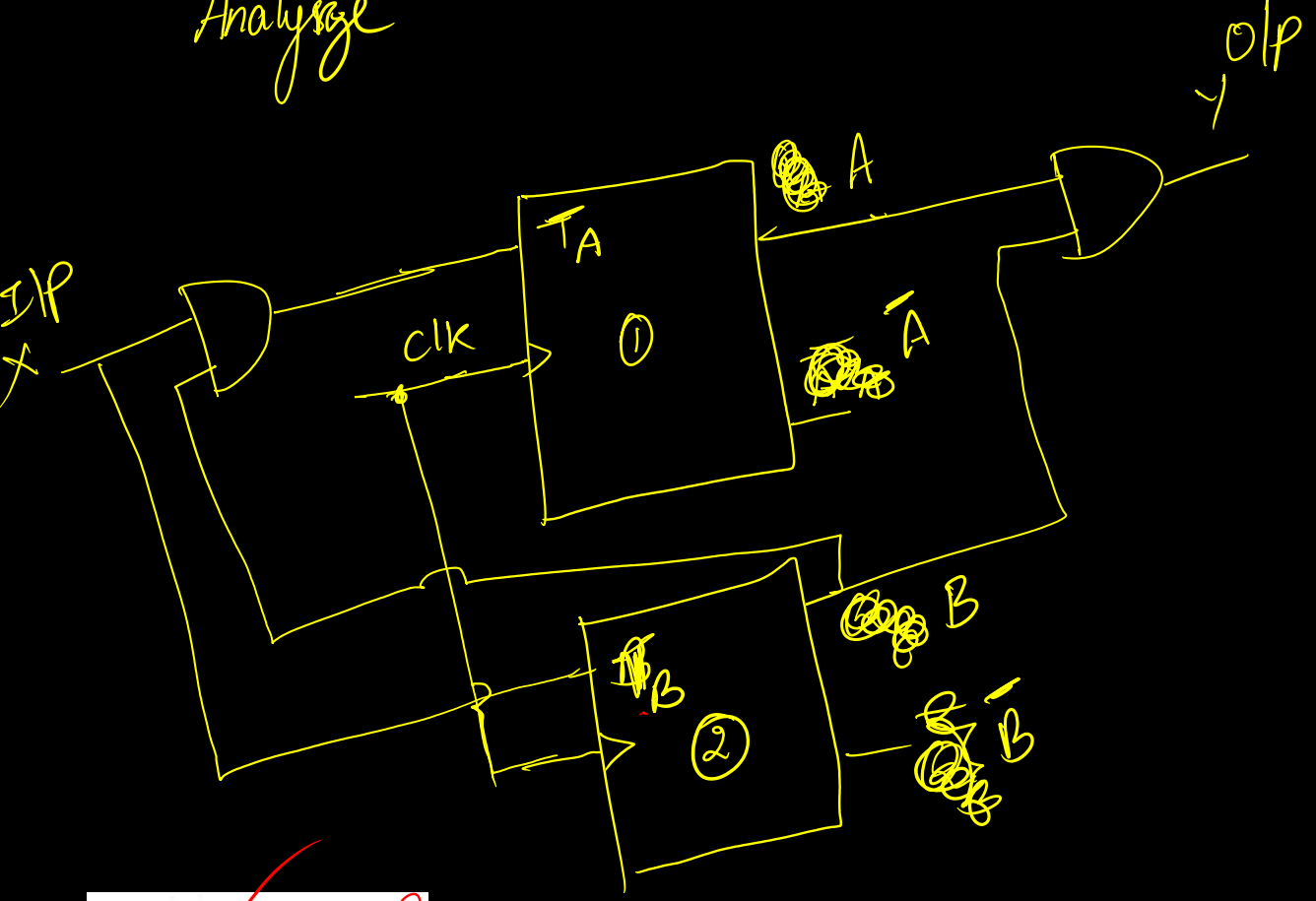
BITS Pilani
Hyderabad Campus

Dr. R. N. Ponnalagu, EEE

Before You hit You must target

If you are taking a single step with confidence
and strong belief towards your goal,
definitely majority of the obstacles you face
will take their way directing you to move
towards your target to hit it powerfully

Analysis



$T_A = Bx$

$T_B = x$

} I/p eqns

$Y = AB$ → O/p

Characteristic equation of T flip flop

$Q_{(t+1)} = T\bar{Q}_t + \bar{T}Q_t$ → next state

here

$A_{(t+1)} = T_A\bar{A} + \bar{T}_A A$

$B_{(t+1)} = T_B\bar{B} + \bar{T}_B B$

Substituting T_A & T_B values

$A_{(t+1)} = \bar{A}Bx + A\bar{B} + A\bar{x}$

$B_{(t+1)} = \bar{B}x + B\bar{x}$

State equations

depends on Present values of A & B & also on i/p x

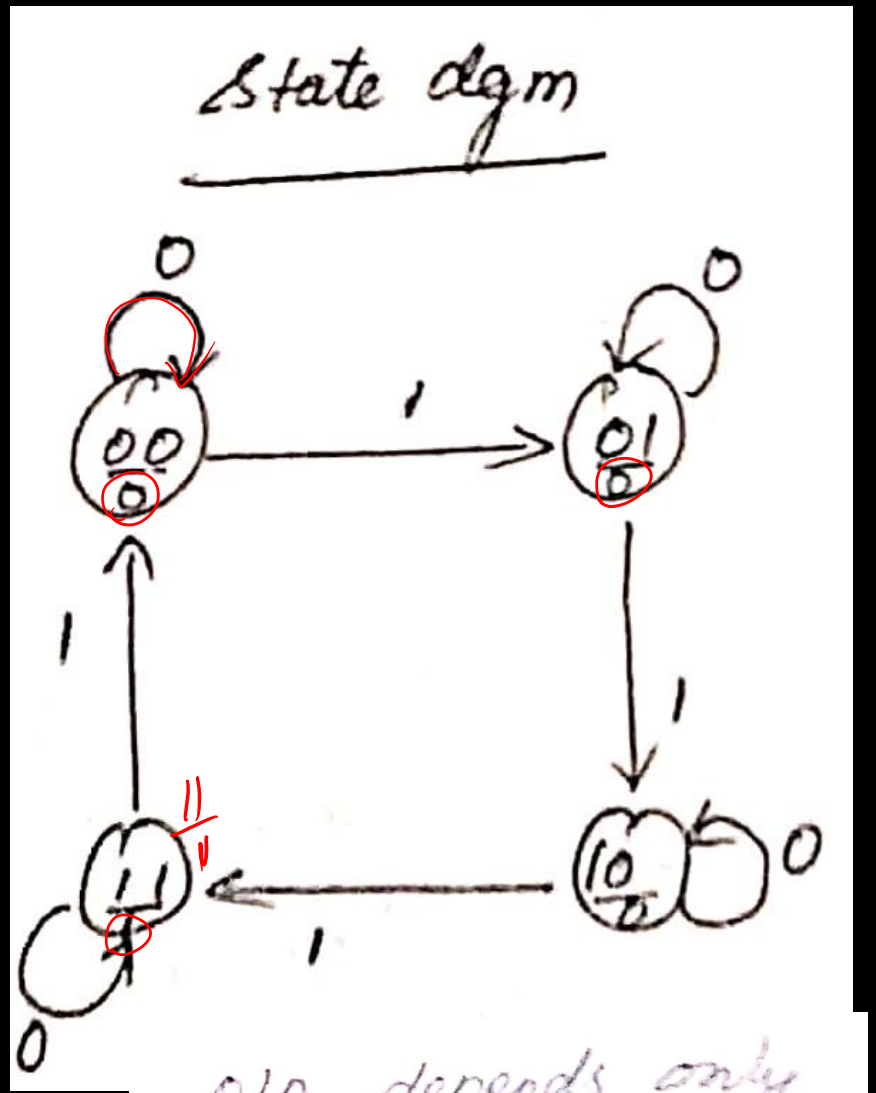
State table

P.S		I/P	N.S		O/P
A	B	x	A	B	Y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	0	1

Not depends on x

$Y = AB$

Present state values



O/p depends only on present state values A & B

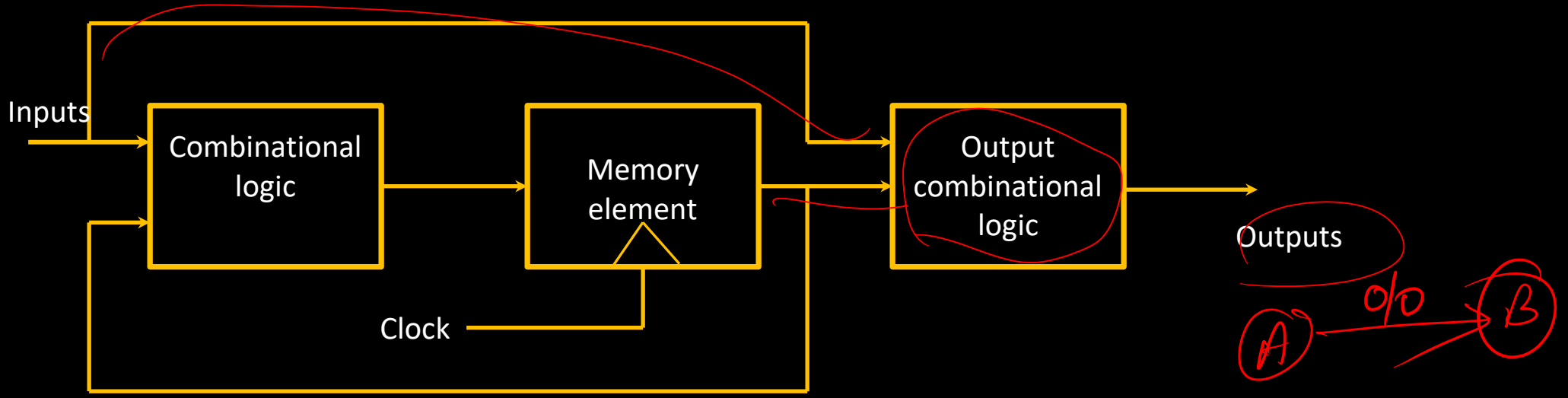
This is Moore model

O/ps are indicated along with states

Moore Machine

Models of sequential circuits

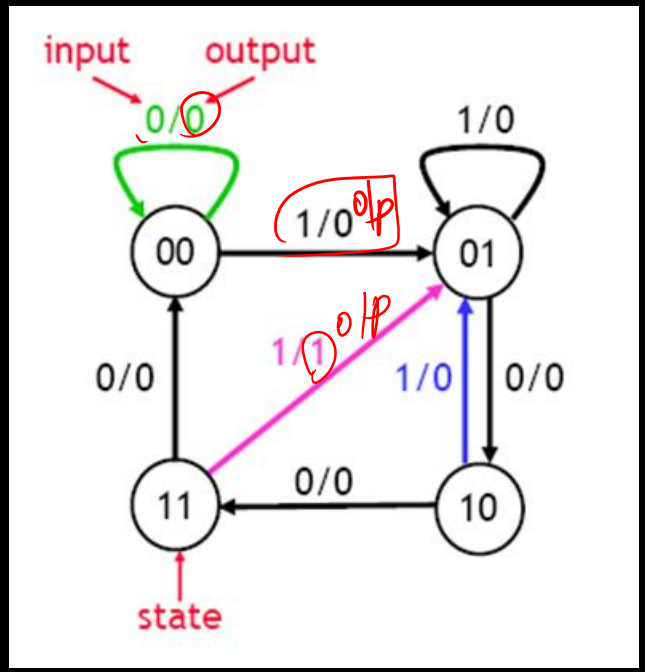
Mealy Model – output depends on present state and input



Changes in input may affect the output of the circuit.

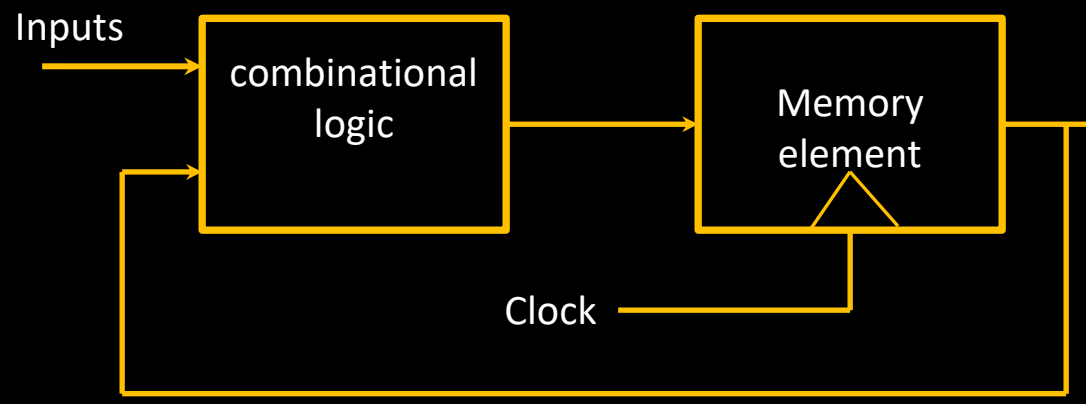
To avoid, inputs should be allowed to change only during clock transition.

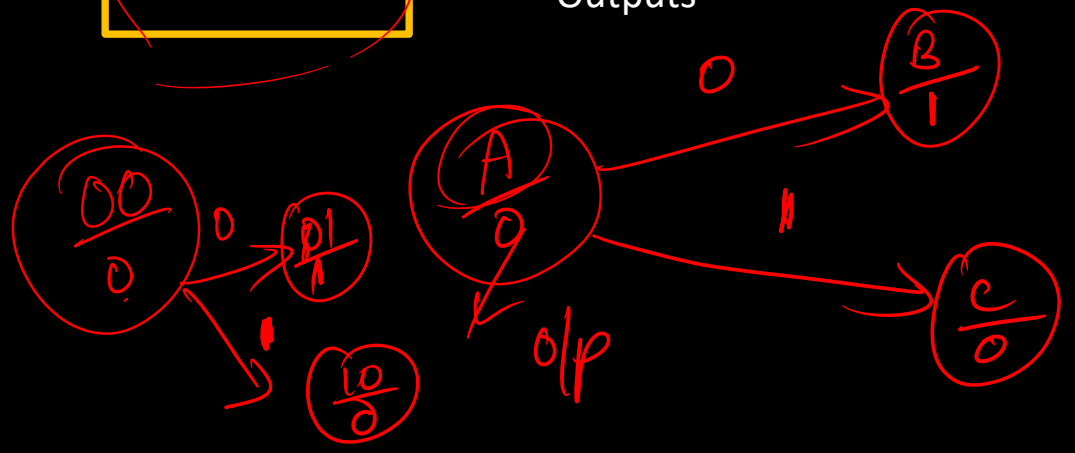
In state diagram representation, outputs are indicated along with inputs in the lines showing transition between the states.


input
output
0/0
1/0
1/0
00
01
0/0
1/0
1/1
1/0
0/0
11
0/0
10
state

Models of sequential circuits

Moore Model – output depends only on present state only





Changes in inputs does not affect the output.

Outputs synchronized with clock

In state diagram representation, outputs are indicated within the circle below the present state

CKV

Sequential Circuits

Analysis Given a circuit

Derive state equations

State table

State diagram

Flip Flop State diagram Try for SR, D, JK and T

State diagram of SR FF

P.S | SR | N.S
0 | 00 | 0
0 | 01 | 1
0 | 10 | 0
0 | 11 | X
1 | 00 | 1
1 | 01 | 0
1 | 10 | 0
1 | 11 | X

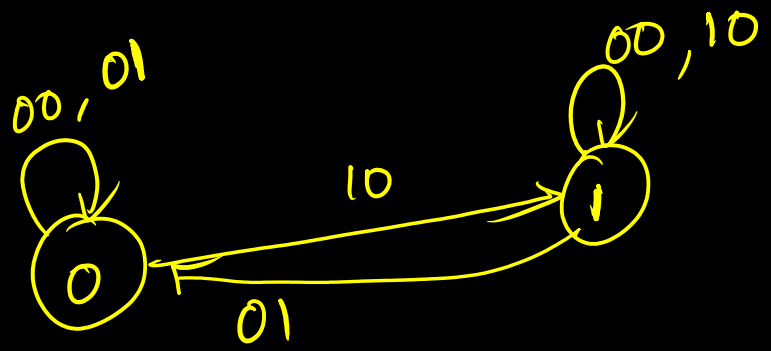
⇒ forbidden

I/P characteristic table

P.S		N.S	
S	R	Q_t	$Q_{(t+1)}$
0	0	0	0
1	0	0	1
X	0	1	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

set state (1)
reset " (0)

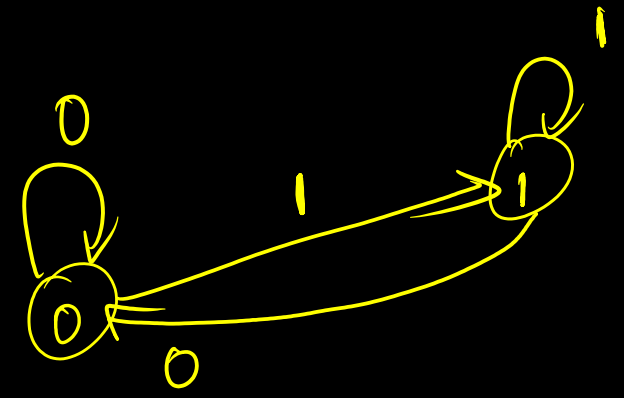
P.S I/P N.S



$Q_{(t+1)} = D$

P.S Q_t	I/P D	N.S $Q_{(t+1)}$
0	0	0
0	1	1
1	0	0
1	1	1

JK ff
&
T ff



DESIGN OF CLOCKED SEQUENTIAL CIRCUITS

Design of sequential Circuits

Given a Functionality/problem description

1. Derive State diagram / state table which ever is easy
   State reduction (if possible)
   Decide on No. of flipflops (depends on no. of states)
   Assign Flipflops
   Write Boolean equations for the inputs and outputs using K-map
   Logic diagram / Circuit

① i) state table
② ii) state diagram
ii) State table
reducing state table

SR, D, JK & T

5 states = 3 FF
4 states = 2 FF

8 states ⇒ 3 FF
4 states ⇒ 2 FF

2 states ⇒ 1 FF
0 & 1
4 states ⇒ 2 FF

n FF
2^n states
2^n states ⇒ n FF

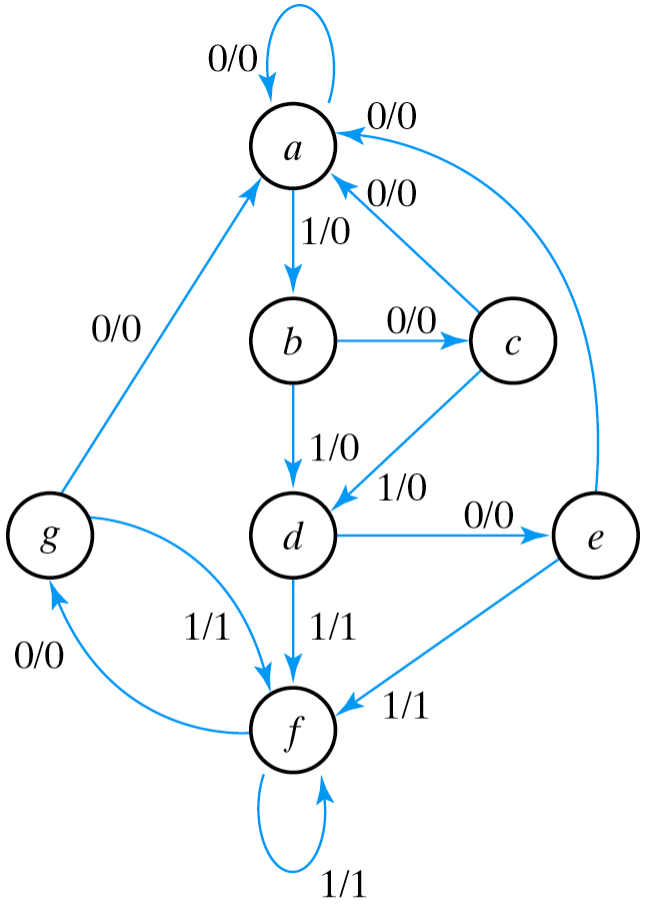
STATE REDUCTION

* Reduces No. of states
* Inturn reduces no. of flip flops
  - ↳ n flipflops ⇒ 2^n states

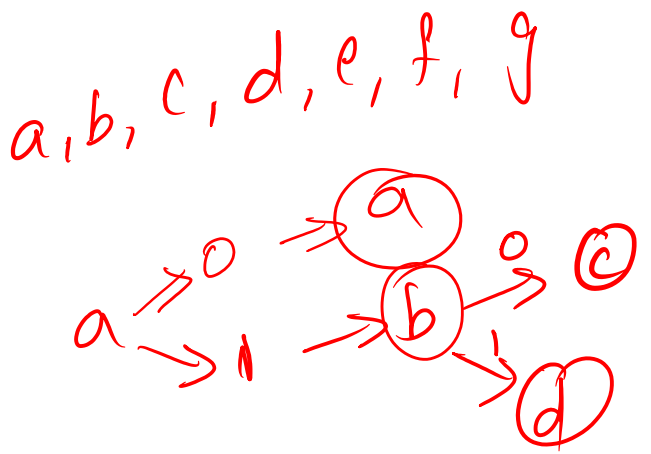
* **Algorithm:** Two states are said to be equivalent if every possible set of i/ps generate exactly same o/p & same next state.

When 2 states are equivalent, one of them can be removed.....

P.S



State Diagram



STATE TABLE

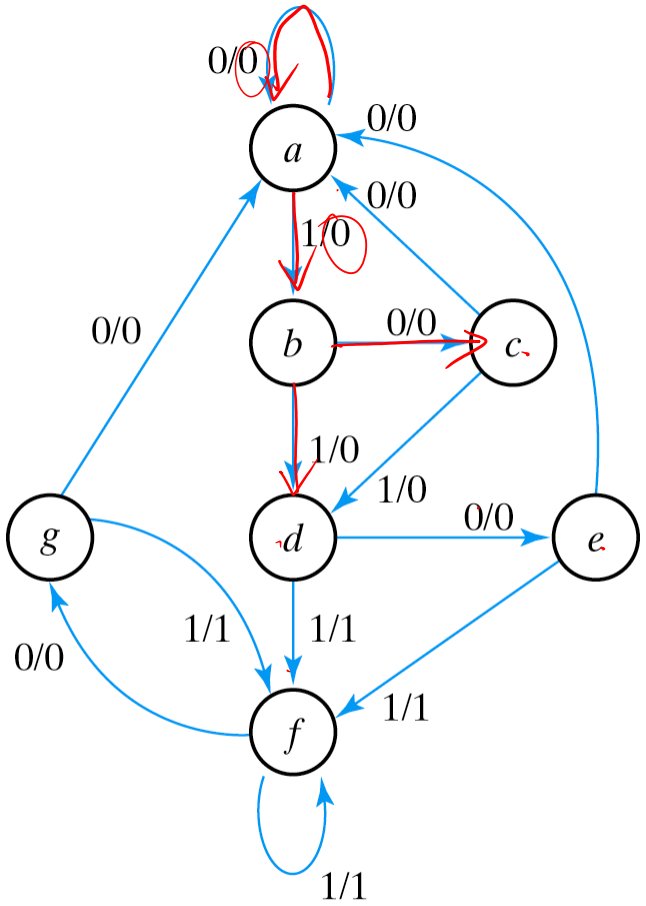


Fig. 5-22 State Diagram

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

STATE TABLE

e ≡ g

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	g	f	0	1
g	a	f	0	1

STATE TABLE

remove g
replace g with e

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	~~g~~ e	f	0	1
~~g~~	a	f	0	1

STATE TABLE

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	f	0	1
e	a	f	0	1
f	e	f	0	1

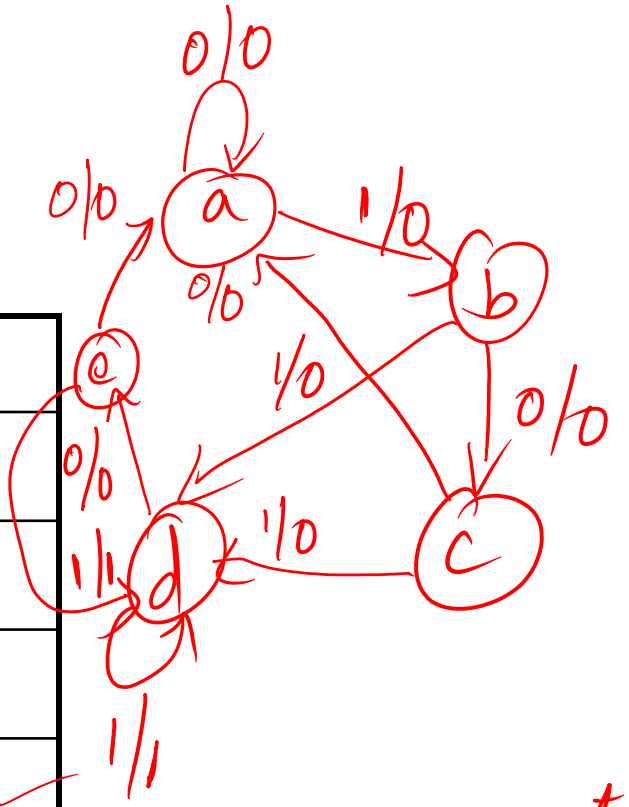
STATE TABLE

d ≡ f

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	~~f~~ d	0	1
e	a	~~f~~ d	0	1
~~f~~	~~e~~	~~f~~	~~0~~	~~1~~

STATE TABLE

Present state	Next State		Output	
	X=0	X=1	X=0	X=1
a	a	b	0	0
b	c	d	0	0
c	a	d	0	0
d	e	d	0	1
e	a	d	0	1



No more reduction possible

3 FFs

a → 000
b → 001
c → 010

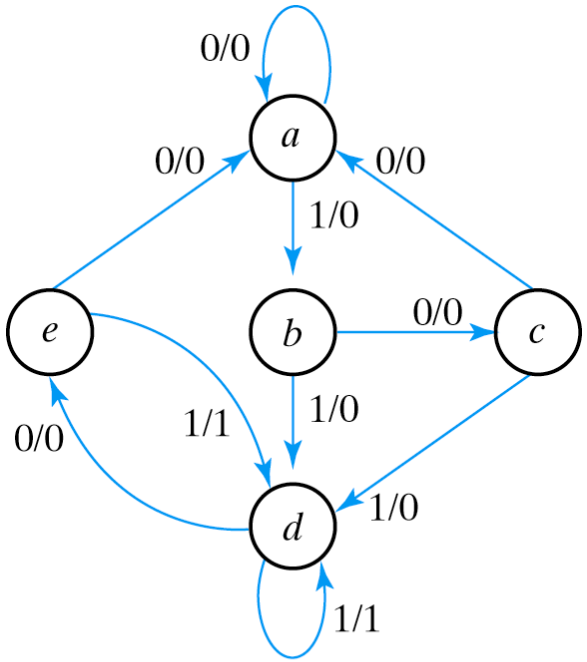
d → 011
e → 100

state assignment

binary assignment

000
010
000
110

reduced state diagram



Sequence Detector

- A Sequence Detector (Recogniser) look for a specific bit pattern in an input string.

- In the example it has an input line called X. One bit of input is applied on every clock and for example it would take 20 clock cycles to enter a 20 bit string.
- It has one output Z which is 1 when a desired pattern is found.

- To detect a pattern 1001

  Ex: Input: 11100110100100110

  Output: 00000100000100100

  One input and one output appear on each clock
- The circuit need to remember bits to recognise a pattern