CS/ECE/EEE/INSTR F215:Digital Design

Lecture 28: *Registers*

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The Capacity to learn is a gift;

The Ability to learn is a skill;

The willingness to learn is a choice!

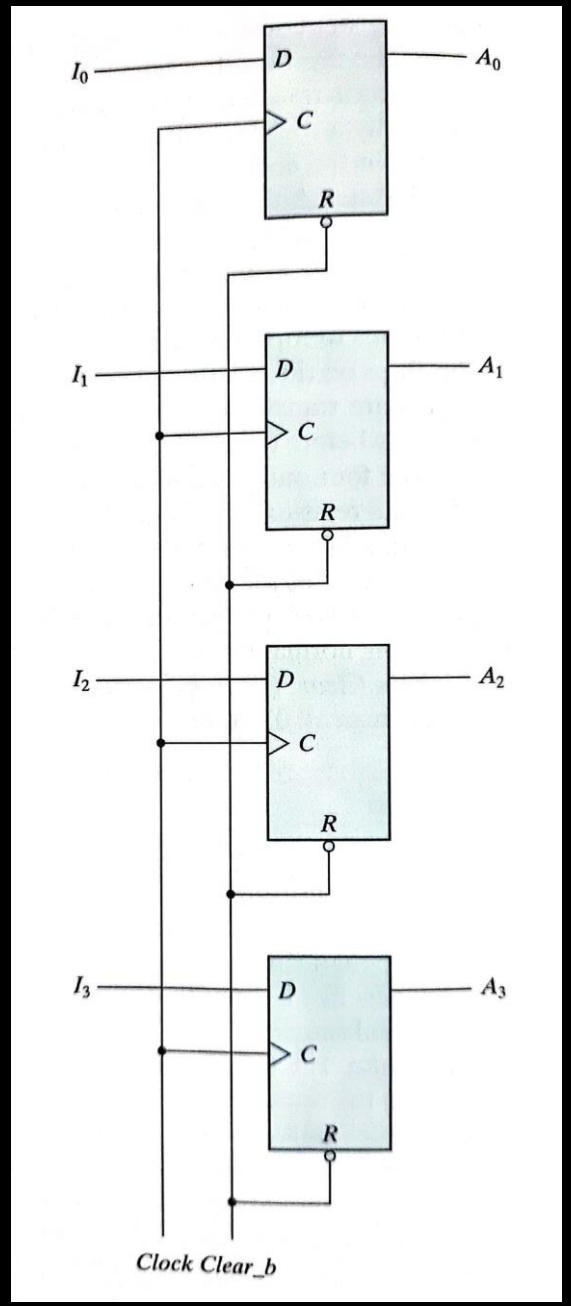
- Brian Herbert

Registers

- Register is an extension of a Flip-flop that can store multiple bits

Register consists of group of flip-flops and some combinational gates. Each FF is capable of storing one bit of information.
N-bit register has group of n-FFs capable of storing n-bits of binary information. The logic gates determine how the information is transferred into the register.

- Ex: Used as a Temporary storage element in Microprocessors



Register constructed using four D-FFs
Clock pulse triggers all the FFs
Binary values available at $I_0I_1I_2I_3$ transferred to register and available as $A_0A_1A_2A_3$

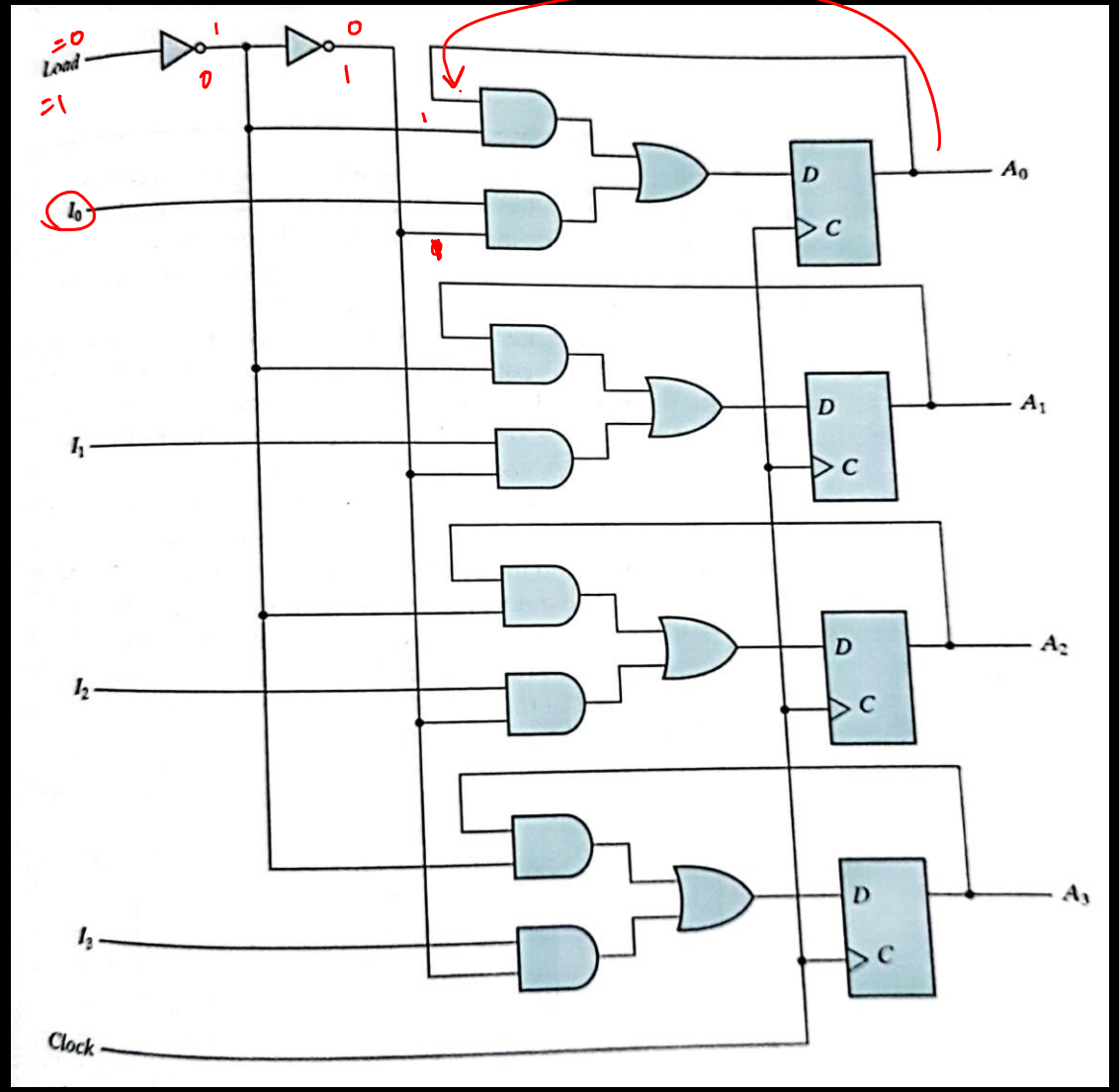
Four outputs can be sampled at any time to obtain the binary information stored in the register.

Clear input clears all the FFs

How can we store the contents of the register for more than one cycle?

Either inputs must be held constant or clock must be inhibited from the circuit by connecting external gates (this will involve uneven propagation delays and result in clock skew affect synchronization)

Controlling the operation of register by controlling the inputs is better than controlling the clock



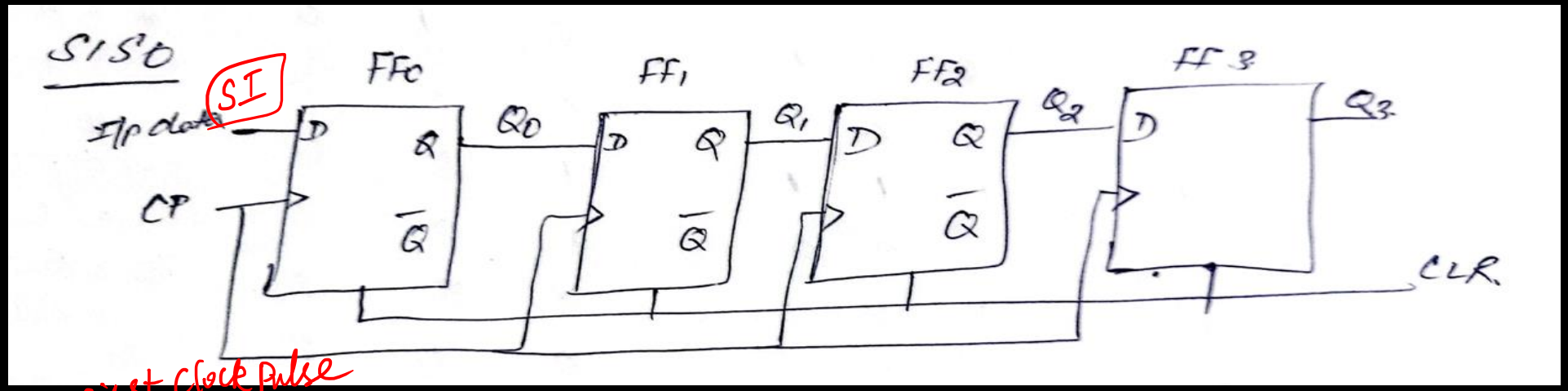
Load =1 means data at the four ext. i/p transferred to register with the next positive edge of the clock.

Load = 0 means outputs of the FFs are connected to their respective inputs.
This implies no change condition leaving the output unchanged.

Shift register: A register capable of shifting its binary information in one or both directions is called shift registers. It consists of chain of FFs in cascade with output of one connected to i/p of next. All FFs receive common CP which activate shift from one stage to next.

Serial Mode- information altered or manipulated one bit at a time

A shift register "shifts" its output once every clock cycle. SI is an input that supplies a new bit to shift "into" the register.



After first clock pulse

$Q0(t+1) = SI$
$Q1(t+1) = Q0(t)$
$Q2(t+1) = Q1(t)$
$Q3(t+1) = Q2(t)$

Here is one example transition.

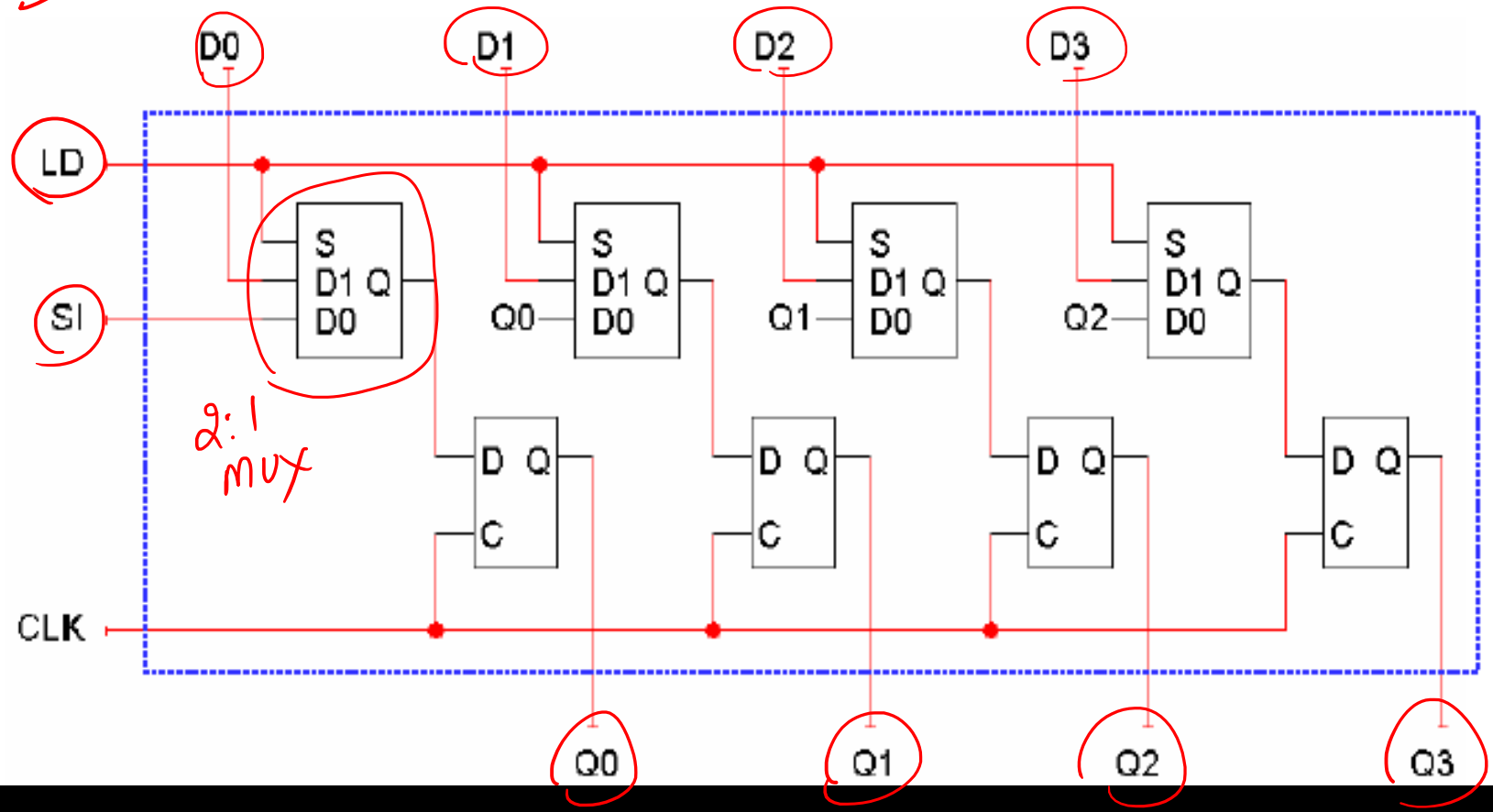
Present State Q0-Q3	Input SI	Next State Q0-Q3
0110	1	1011

The current Q3 (0 in this example) will be lost on the next cycle.

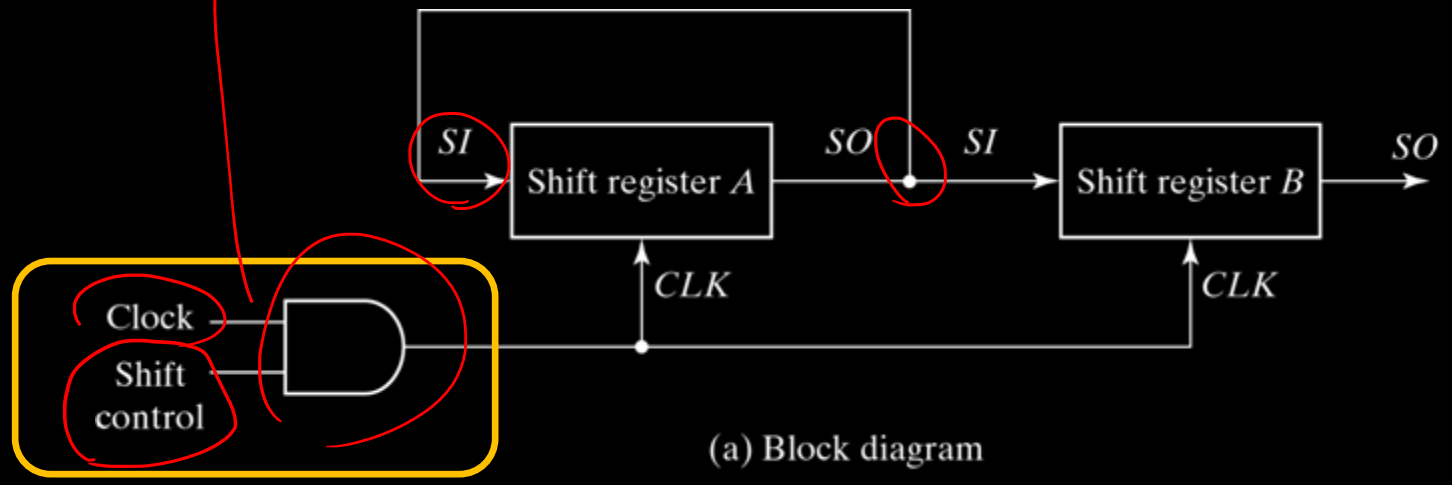
Applications of shift register – serial data transfer (e.g. USB, UART)

Shift registers with parallel load

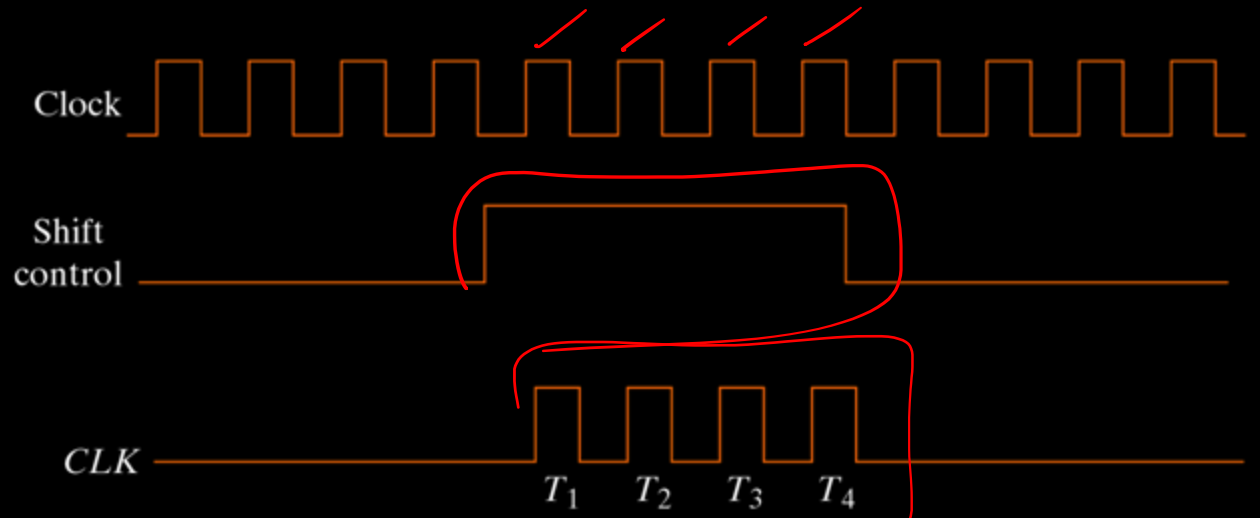
- We can add a parallel load operation, just as we did for regular registers.
  - When LD = 0 the flip-flop inputs will be SIQ0Q1Q2, so the register will shift on the next positive clock edge.
  - When LD = 1, the flip-flop inputs are D0-D3, and a new value is loaded into the register on the next positive clock edge.



Serial Transfer

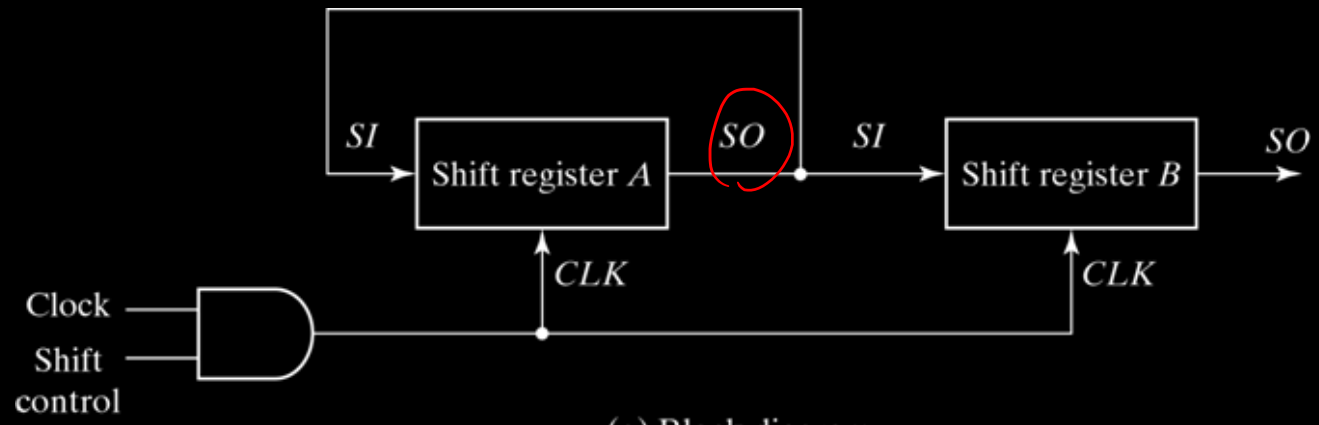


(a) Block diagram

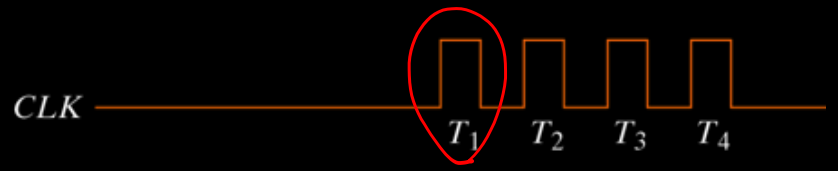


Serial Transfer

Operation assuming 4-bit shift register



(a) Block diagram



Timing pulse	Shift Register A	Shift Register B
Initial value	1 0 1 1	0 0 1 0
After T_1	1 1 0 1	1 0 0 1
After T_2	1 1 1 0	1 1 0 0
After T_3	0 1 1 1	0 1 1 0
After T_4	1 0 1 1	1 0 1 1

Universal Shift register

Capabilities of Universal shift register

- Clear signal to clear the register to 0
- Clock input to synchronize
- Shift-right
- Shift-left

  } Bidirectional shift Register

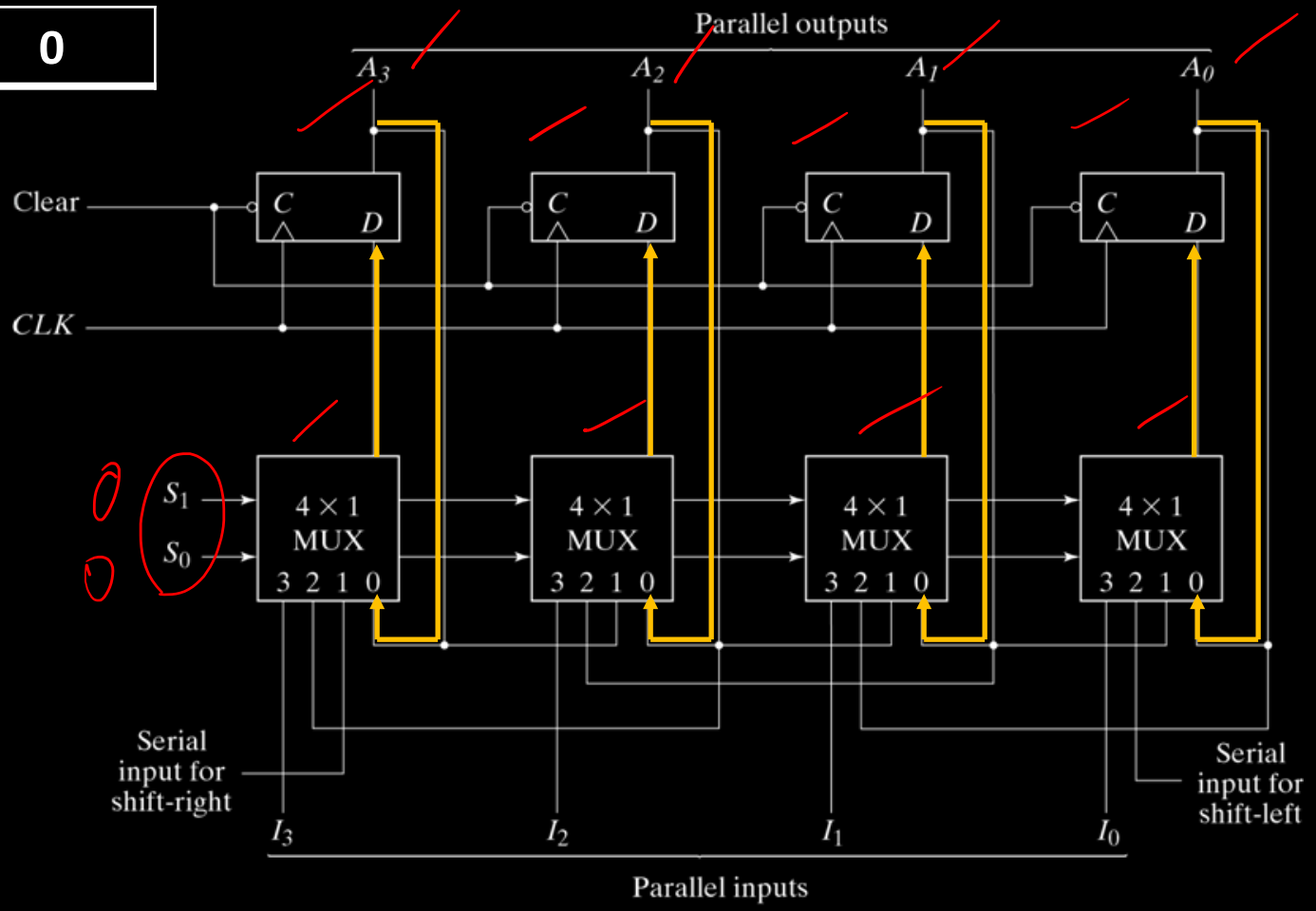
- Parallel load
- Parallel out
- Control state to leave information in register unchanged

Universal Shift register

Mode control		Register operation
S_1	S_0	
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

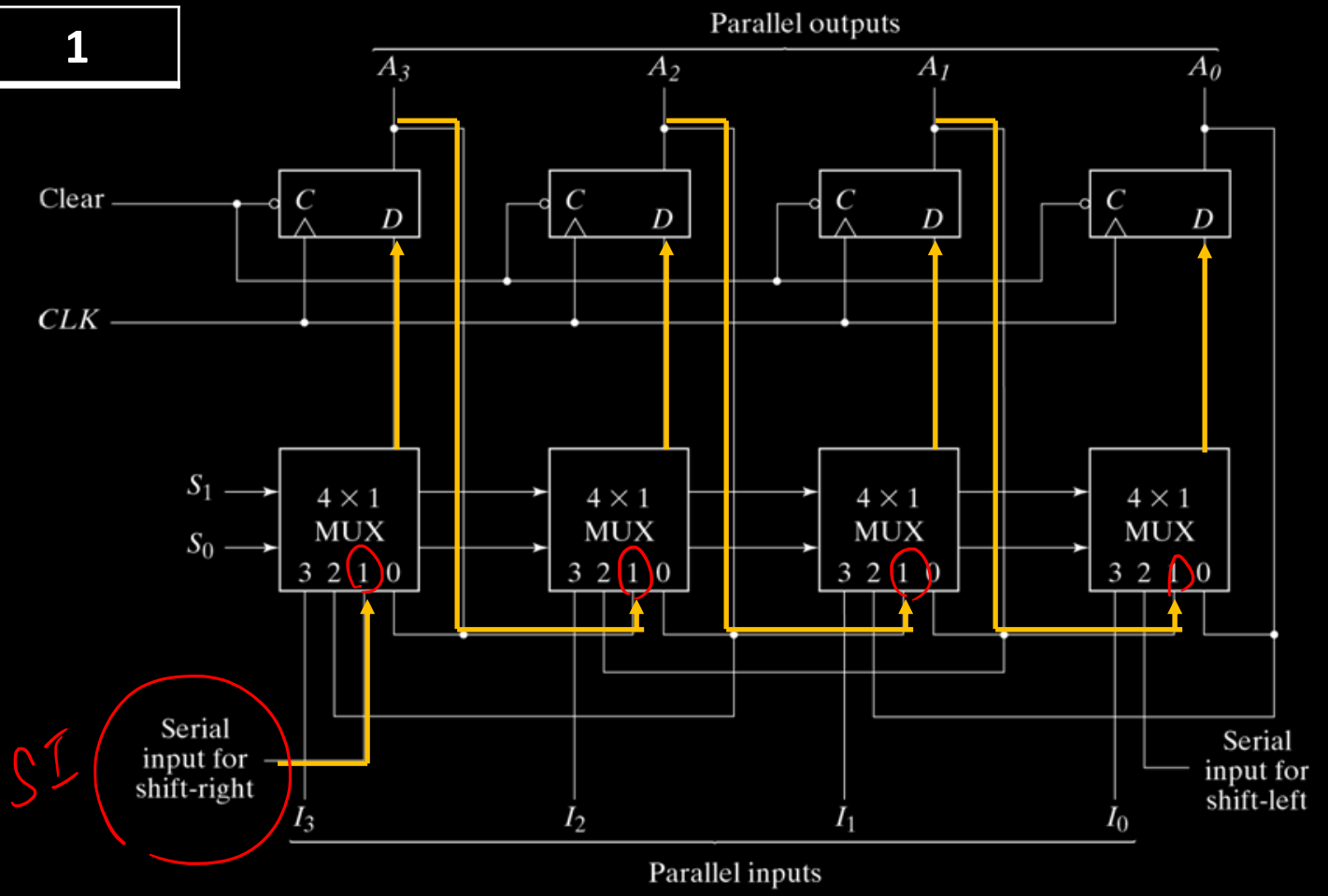
Universal Shift register

0	0



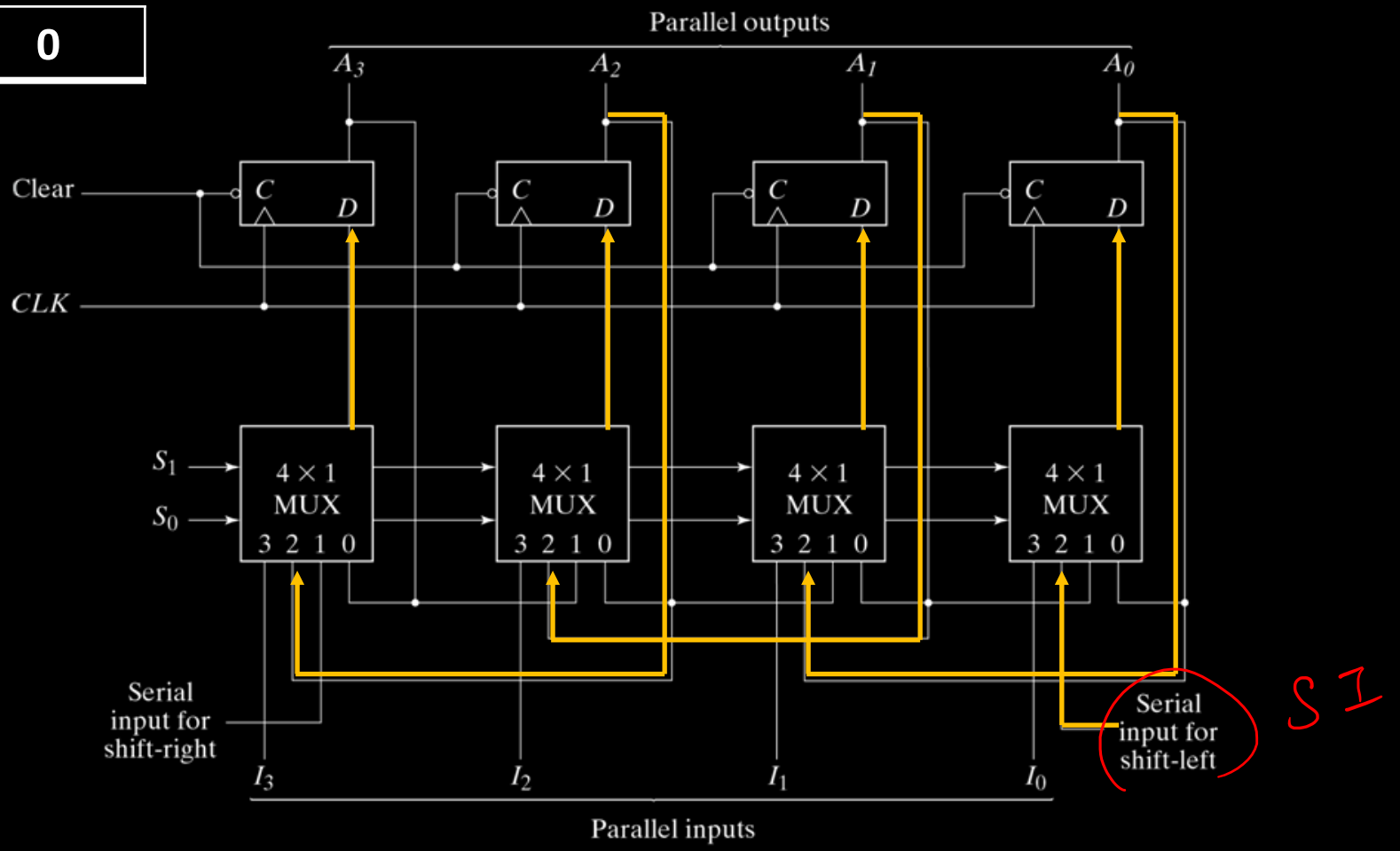
Universal Shift register

0	1



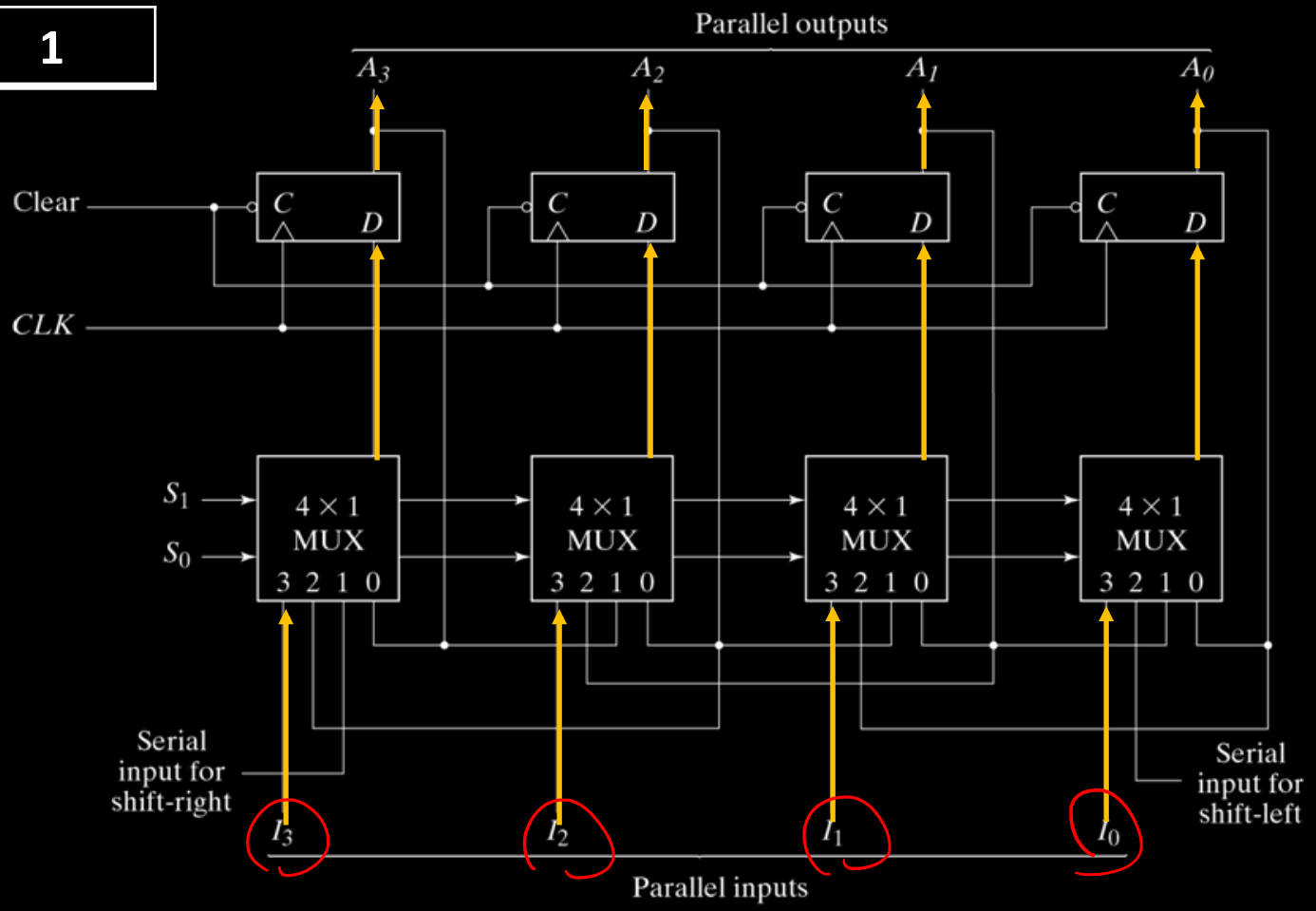
Universal Shift register

1	0



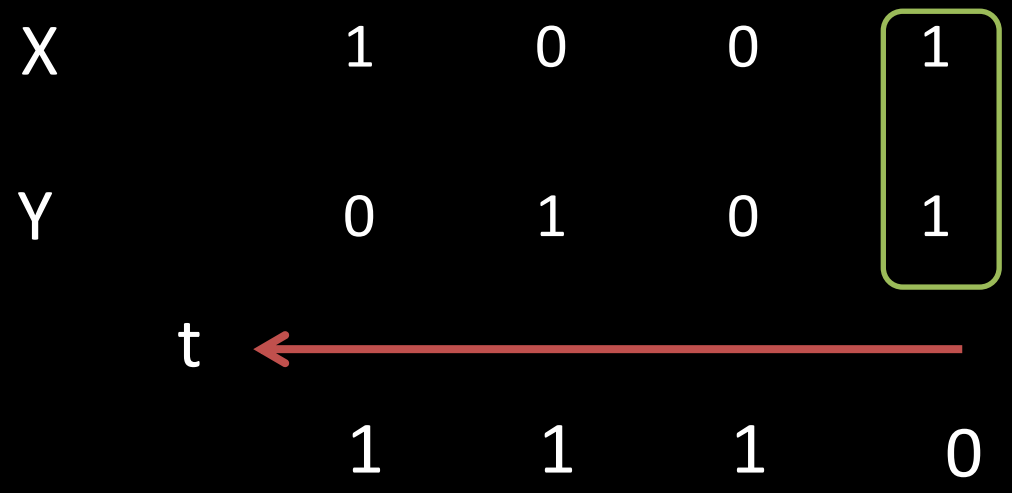
Universal Shift register

1	1

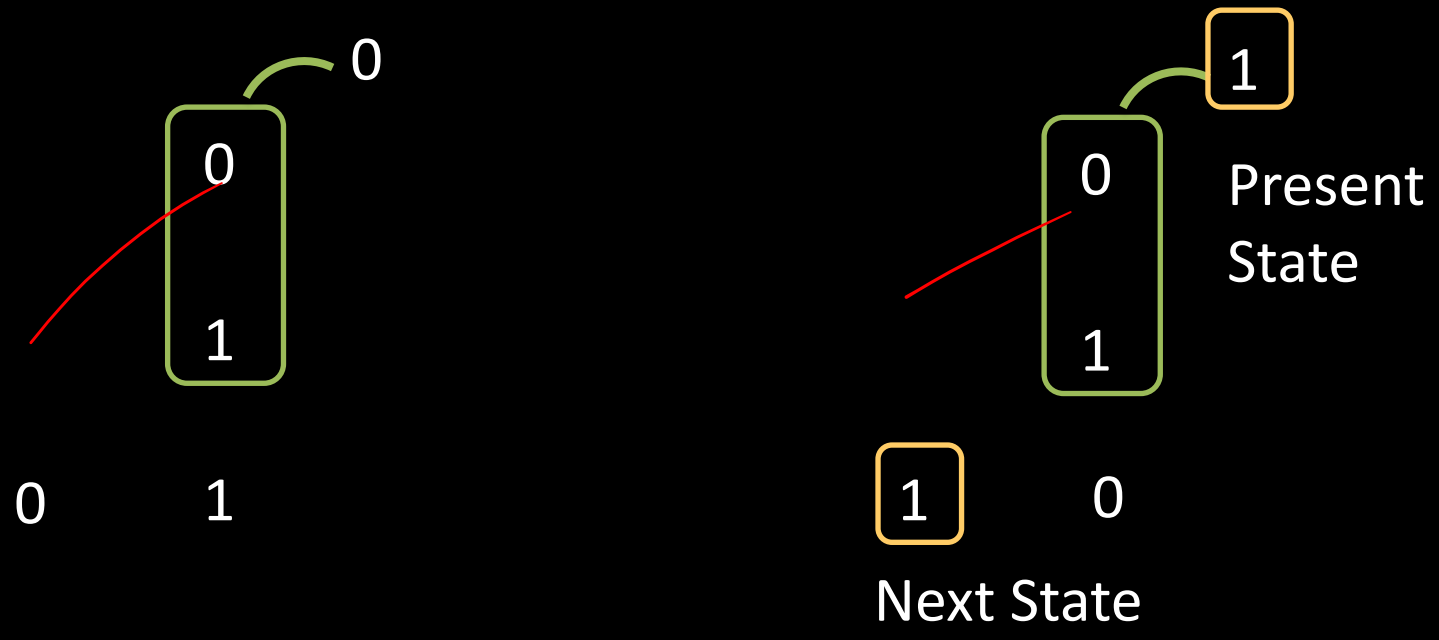


Serial Adder

bit by bit



Serial Adder



Define two states S0 and S1

S0 indicates carry = 0

S1 indicates carry = 1

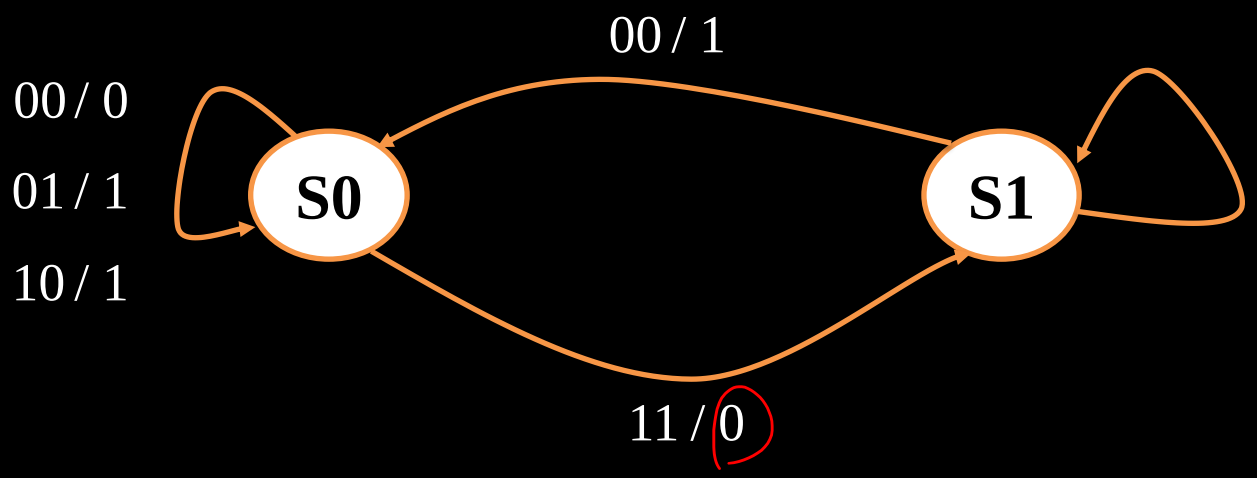
Serial Adder

Define two states S0 and S1

S0 indicates carry = 0

S1 indicates carry = 1

X and Y indicates inputs, Sum is output



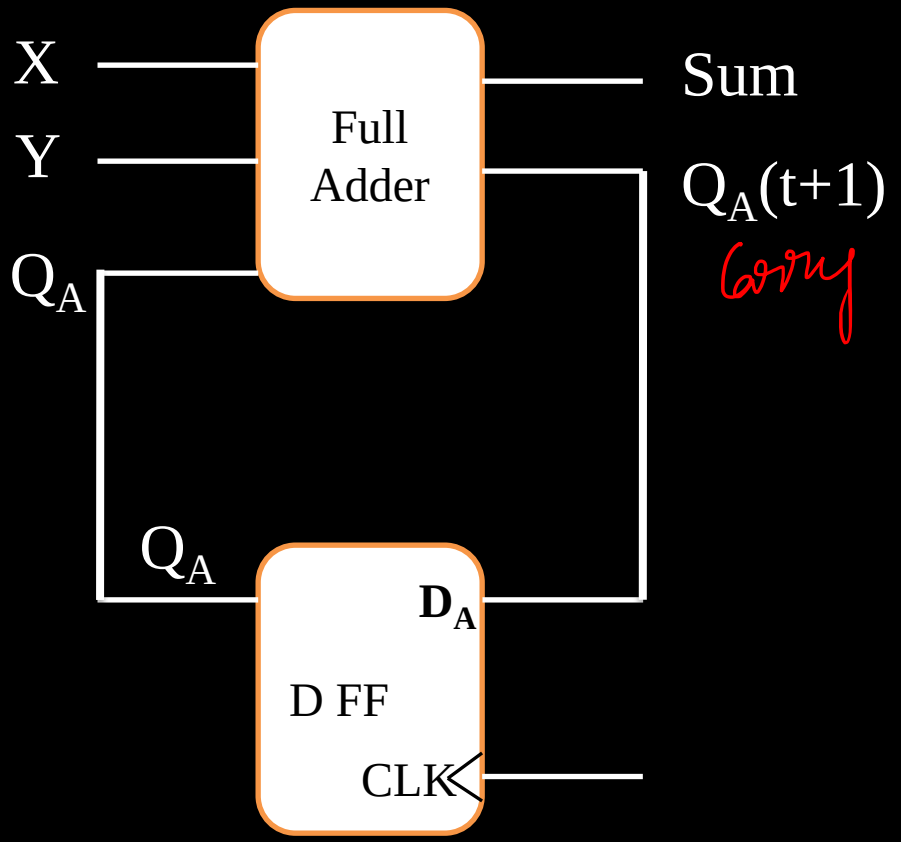
Serial Adder

Present State				Next State		Out
	Q_A	X	Y		$Q_{A(t+1)}$	Sum
S0	0	0	0	S0	0	0
S0	0	0	1	S0	0	1
S0	0	1	0	S0	0	1
S0	0	1	1	S1	1	0
S1	1	0	0	S0	0	1
S1	1	0	1	S1	1	0
S1	1	1	0	S1	1	0
S1	1	1	1	S1	1	1

$$Q_A(t+1) = Q_AX + XY + Q_AY$$

$$\text{Sum} = Q_A \oplus X \oplus Y$$

Serial Adder

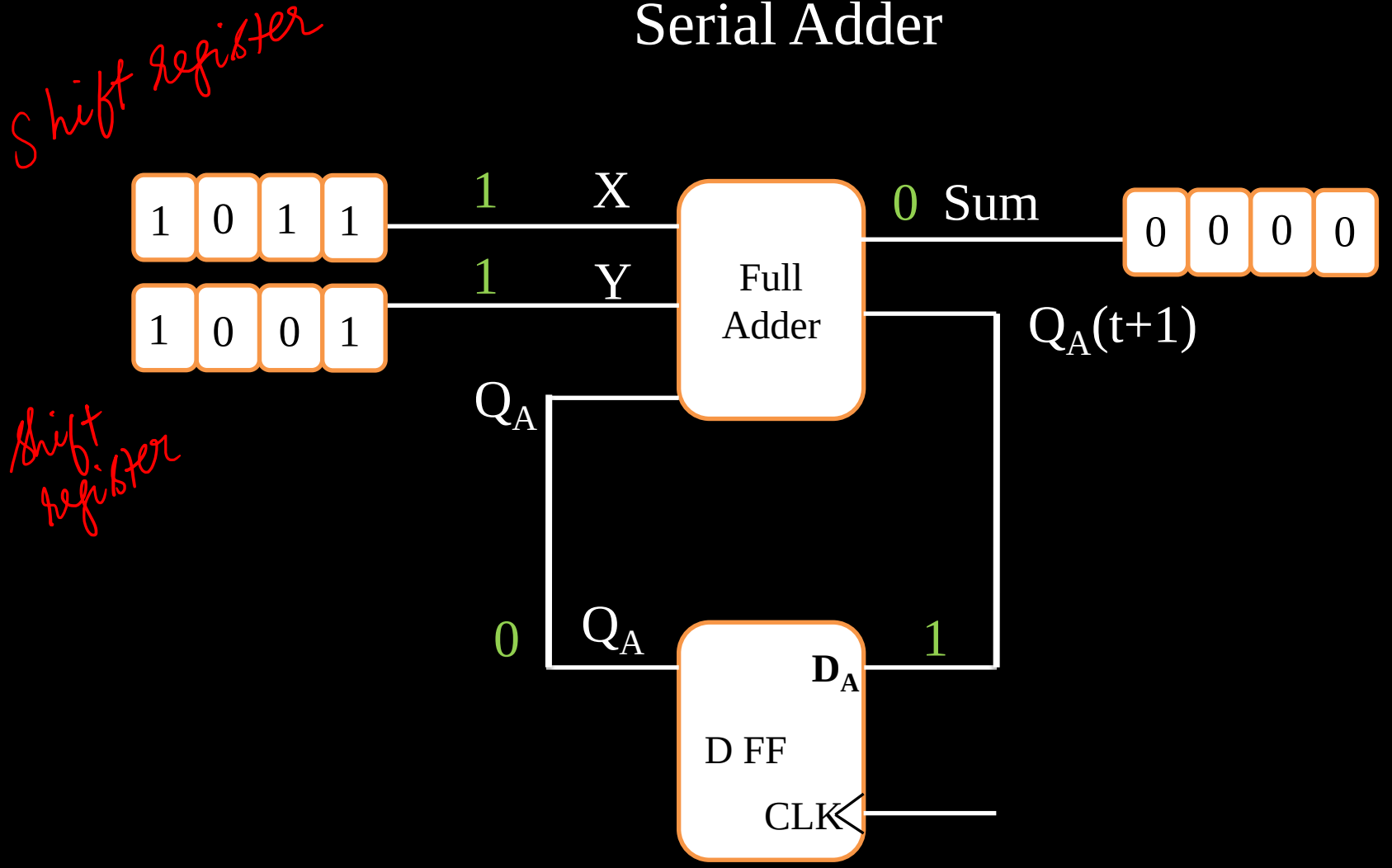


$$Q_A(t+1) = Q_AX + XY + Q_AY$$

$$Sum = Q_A \oplus X \oplus Y$$

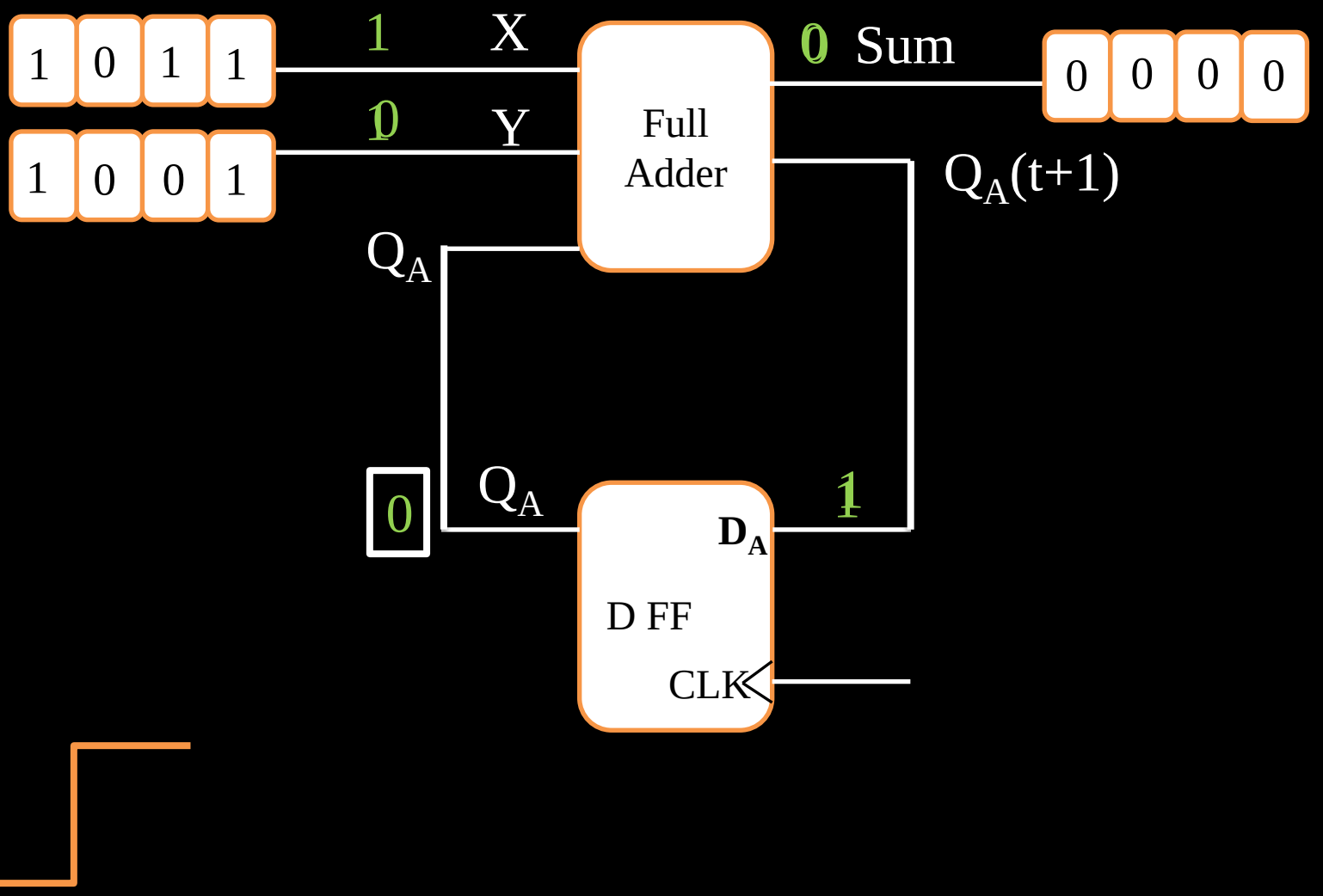
How to control X and Y ?

Serial Adder

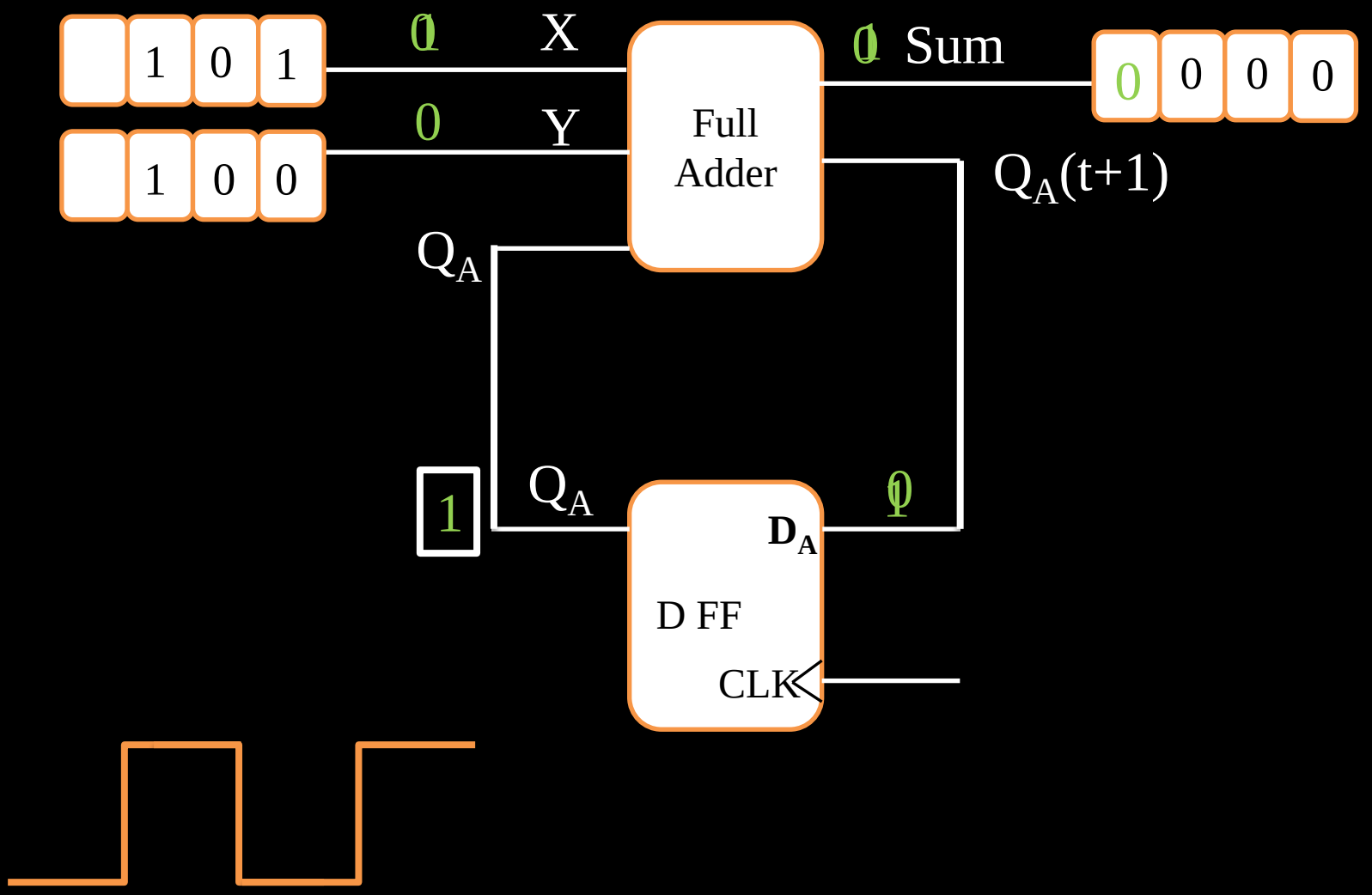


Before any clock pulses

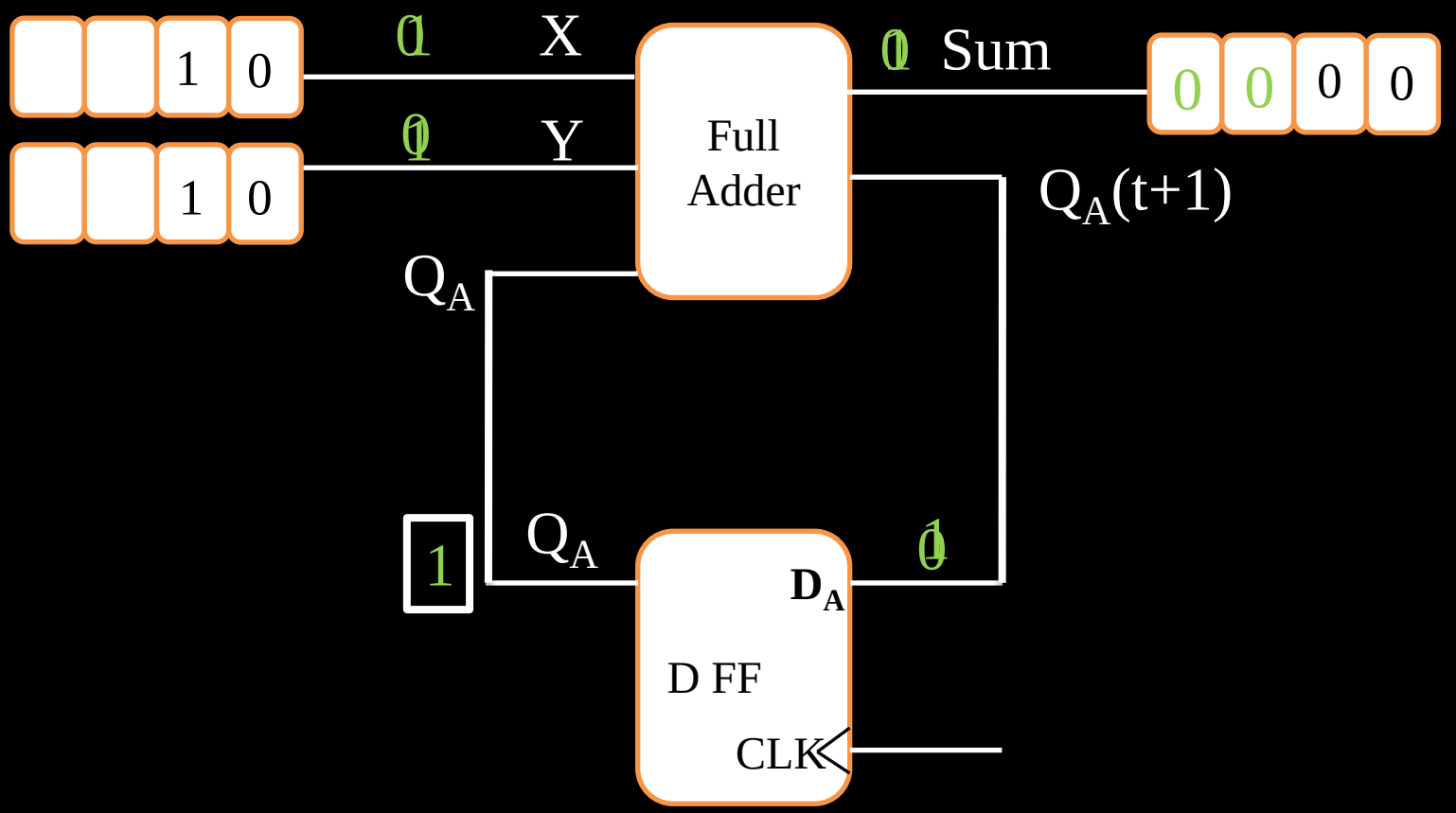
Serial Adder



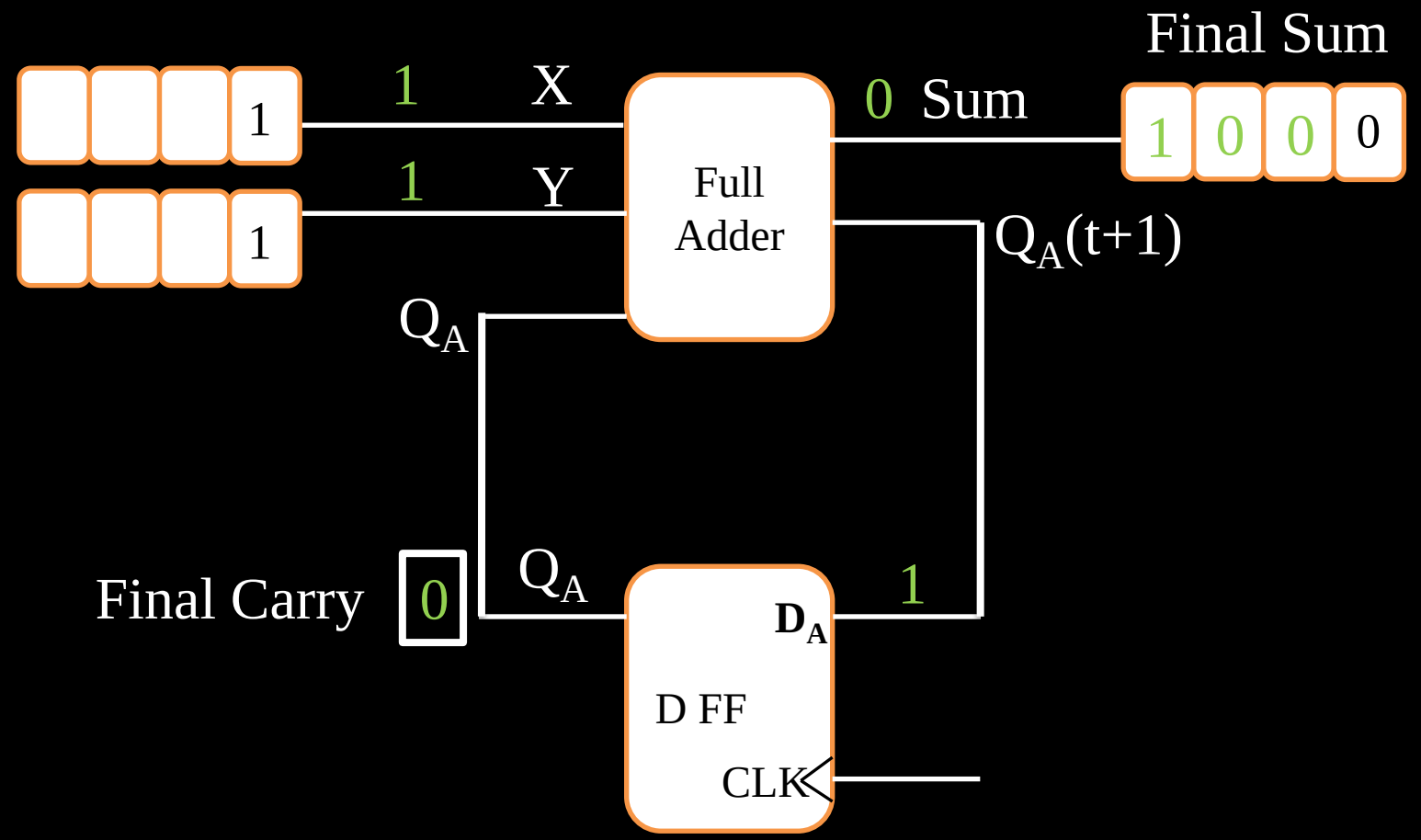
Serial Adder



Serial Adder



Serial Adder



Serial Adder

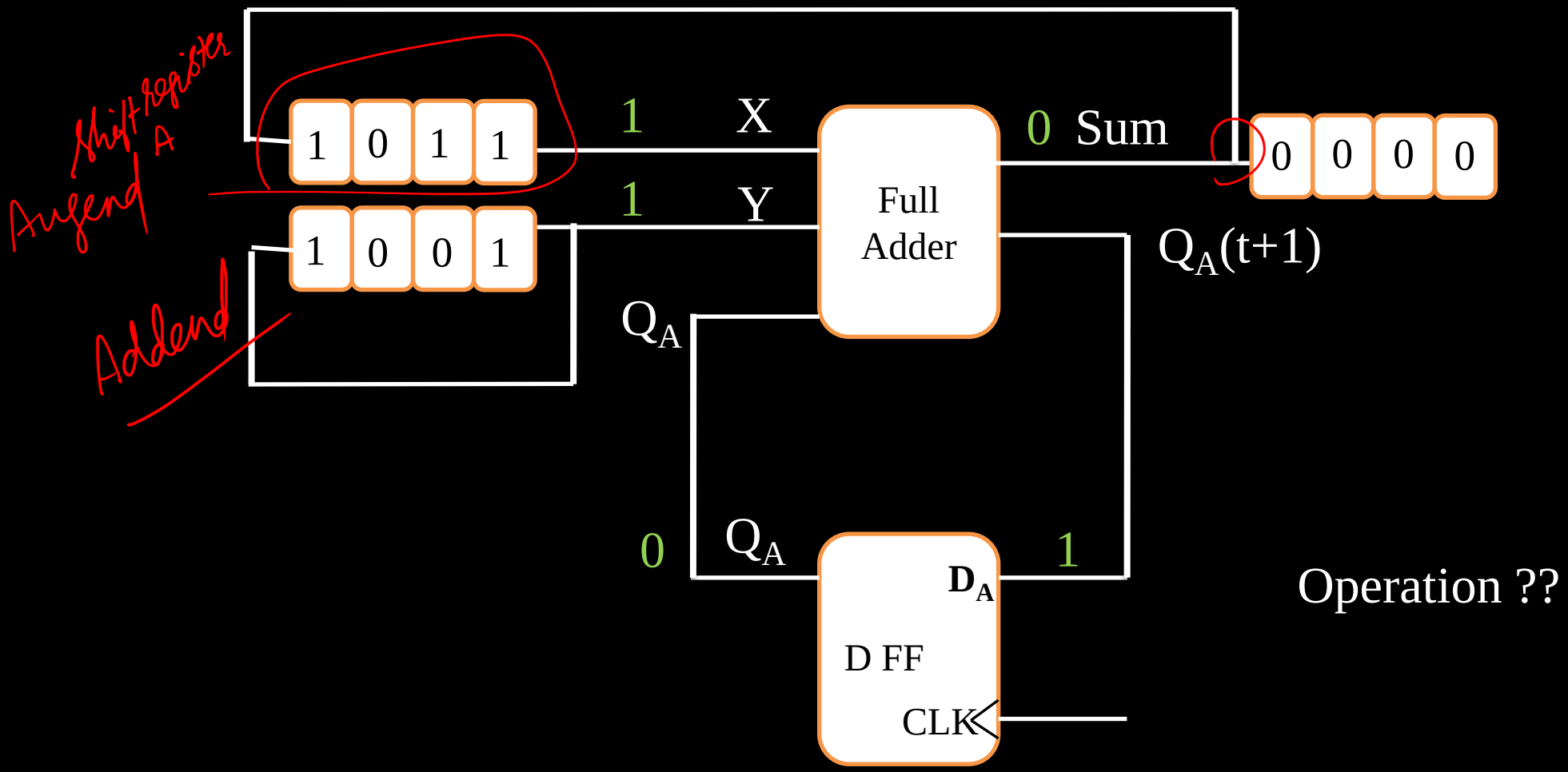
A 1- bit full adder is sufficient for n-bit addition

N-clock cycles for N-bit addition

Complex control circuitry

More memory elements required

Serial Adder



Shift registers will have additional control signals like load, shift control