BIRLA INSTITUTE OF SCIENCE AND TECHNOLOGY PILANI, HYDERABAD CAMPUS

DIGITAL DESIGN LABORATORY (Session 2021-22)

Workbook

Experiment -2

Full Name of the Student:

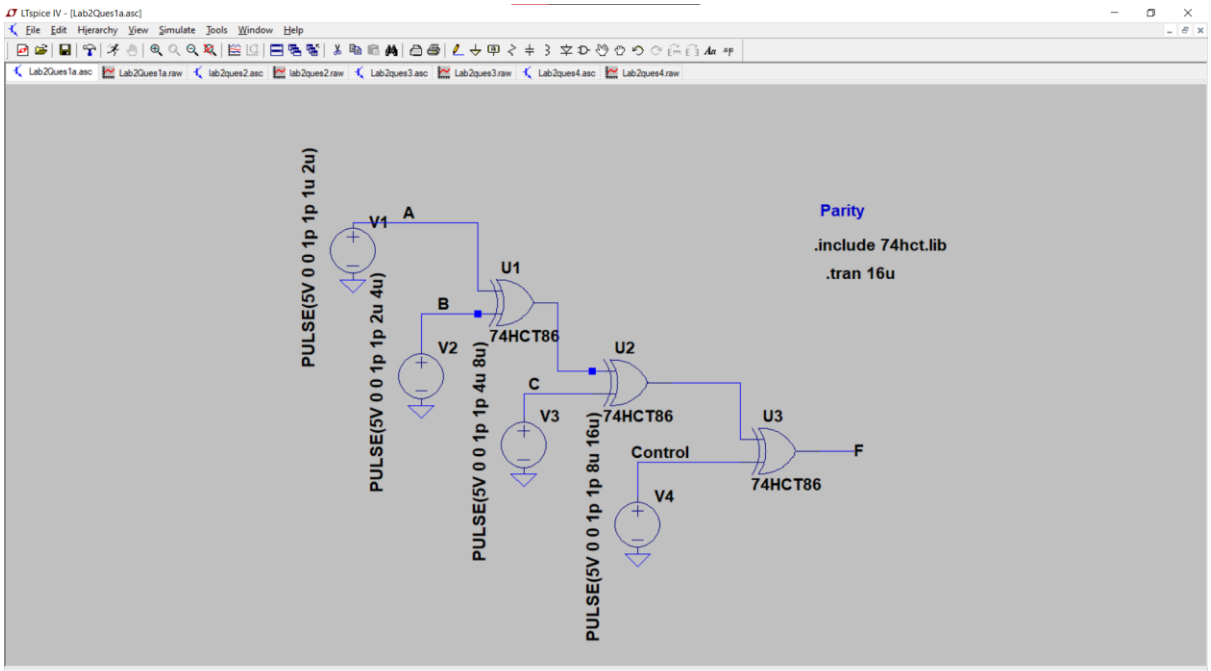
Complete ID of the student:

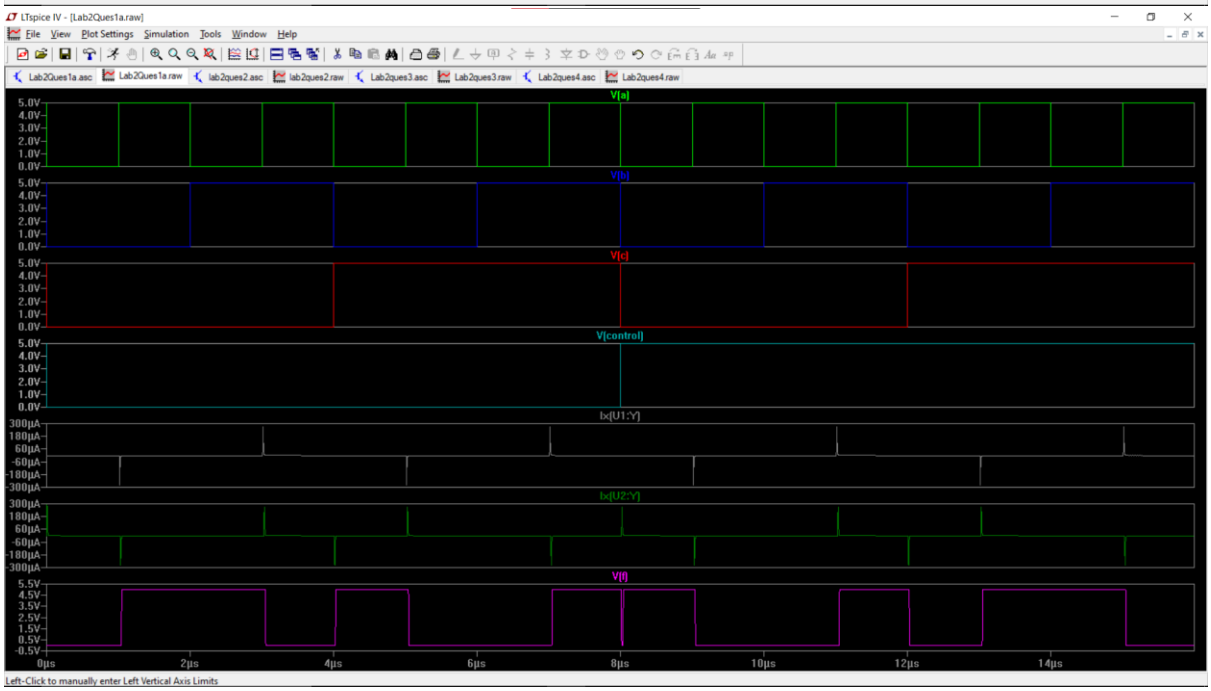
Title of Experiment:

Problem 1:

Implement the three variable (X,Y,Z) based 'Odd Parity' and 'Even Parity' Generator circuits using EX-OR Gates on LT-SPICE simulation platform.

(Provide proper LTSPICE model snapshot with neat levelling and show the graphical output at all the logic gates used in the circuit)

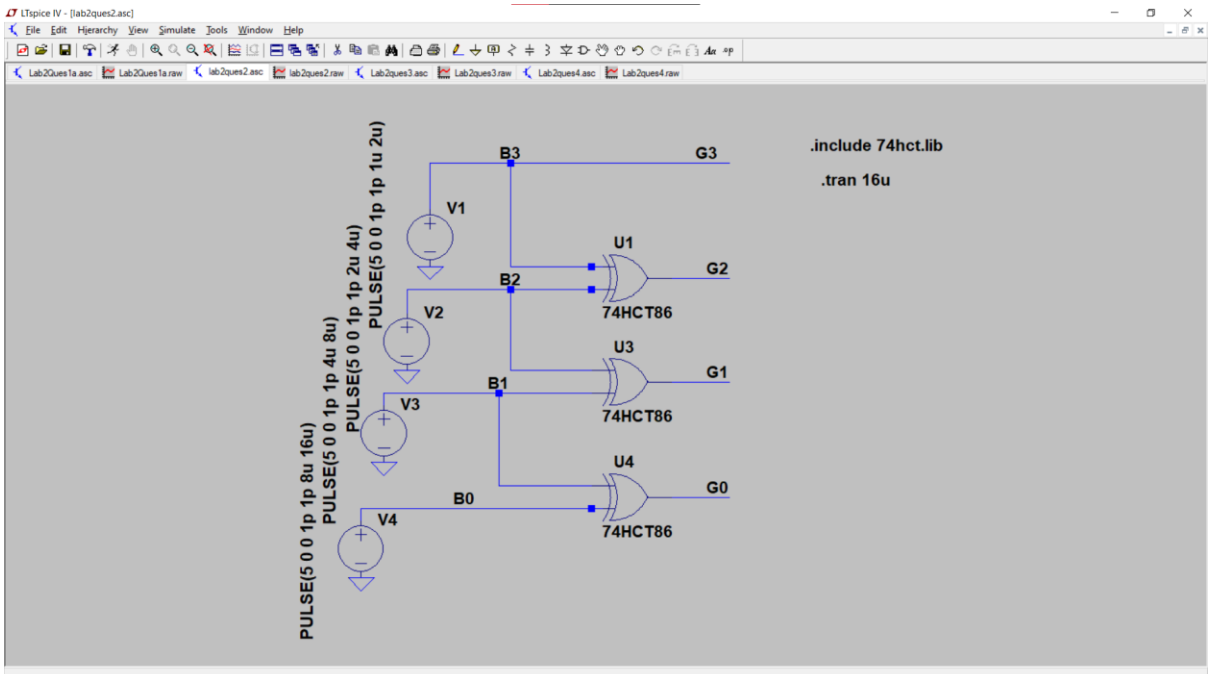

LTspice IV - [Lab2Ques1a.asc]
File Edit Hierarchy View Simulate Tools Window Help
Lab2Ques1a.asc Lab2Ques1a.raw lab2ques2.asc lab2ques2.raw Lab2ques3.asc Lab2ques3.raw Lab2ques4.asc Lab2ques4.raw
PULSE(5V 0 0 1p 1p 1u 2u)
V1
A
U1
PULSE(5V 0 0 1p 1p 2u 4u)
B
74HCT86
V2
U2
C
PULSE(5V 0 0 1p 1p 4u 8u)
V3
74HCT86
U3
Control
F
74HCT86
V4
PULSE(5V 0 0 1p 1p 8u 16u)
Parity
.include 74hct.lib
.tran 16u

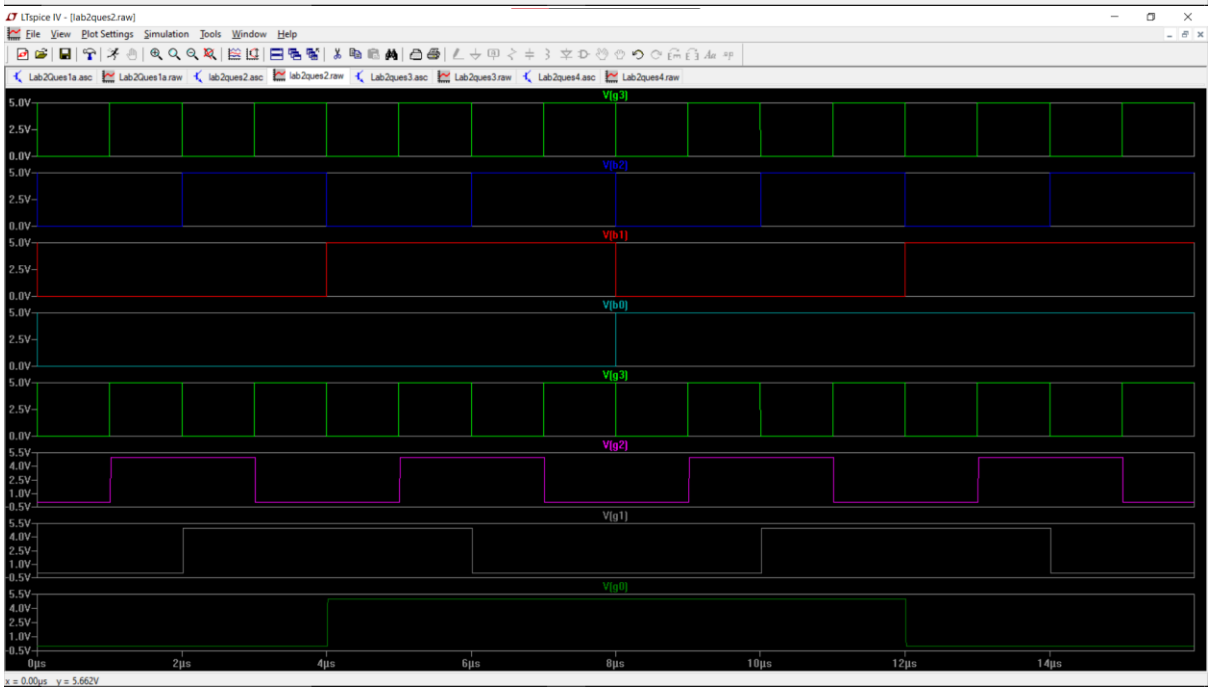

LTspice IV - [Lab2Ques1a.raw]
File View Plot Settings Simulation Tools Window Help
Lab2Ques1a.asc Lab2Ques1a.raw lab2ques2.asc lab2ques2.raw Lab2ques3.asc Lab2ques3.raw Lab2ques4.asc Lab2ques4.raw
V(a)
V(b)
V(c)
V(control)
Ix(U1:Y)
Ix(U2:Y)
V(f)
0µs 2µs 4µs 6µs 8µs 10µs 12µs 14µs
Left-Click to manually enter Left Vertical Axis Limits

Problem 2:

Design and implement '4-bit Binary to Grey code converter' with the help of Truth–Table on LT-SPICE simulation platform.

(Provide proper LTSPICE model snapshot with neat levelling and show the graphical output)

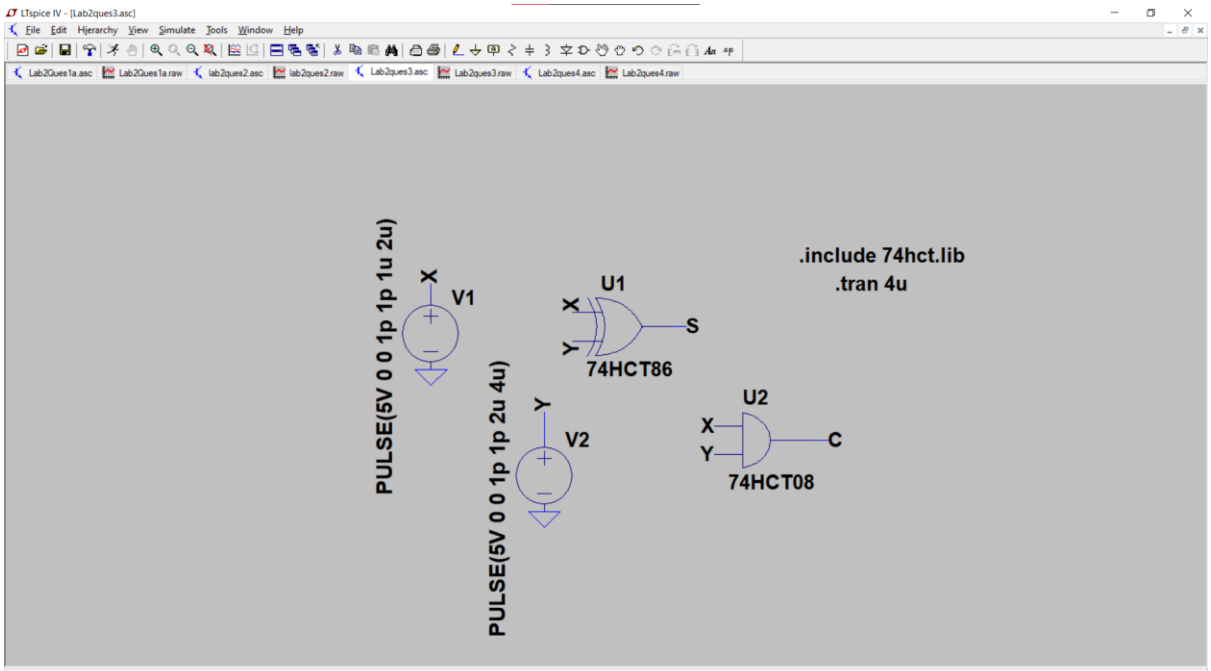

LTspice IV - [lab2ques2.asc]
File Edit Hierarchy View Simulate Tools Window Help
Lab2Ques1a.asc Lab2Ques1a.raw lab2ques2.asc lab2ques2.raw Lab2ques3.asc Lab2ques3.raw Lab2ques4.asc Lab2ques4.raw
B3
G3
V1
PULSE(5 0 0 1p 1p 1u 2u)
U1
G2
B2
V2
PULSE(5 0 0 1p 1p 2u 4u)
74HCT86
U3
G1
B1
V3
PULSE(5 0 0 1p 1p 4u 8u)
74HCT86
U4
G0
B0
V4
PULSE(5 0 0 1p 1p 8u 16u)
74HCT86
.include 74hct.lib
.tran 16u


LTspice IV - [lab2ques2.raw]
File View Plot Settings Simulation Tools Window Help
Lab2Ques1a.asc Lab2Ques1a.raw lab2ques2.asc lab2ques2.raw Lab2ques3.asc Lab2ques3.raw Lab2ques4.asc Lab2ques4.raw
V(g3)
V(b2)
V(b1)
V(b0)
V(g3)
V(g2)
V(g1)
V(g0)
5.0V
2.5V
0.0V
5.5V
4.0V
1.0V
-0.5V
0µs
2µs
4µs
6µs
8µs
10µs
12µs
14µs
x = 0.00µs y = 5.662V

Problem 3:

Design and implement a two input Half- Adder circuit on LTSPICE platform.

(Provide proper LTSPICE model snapshot with neat levelling and show the graphical result containing the Inputs and Sum with Carry)

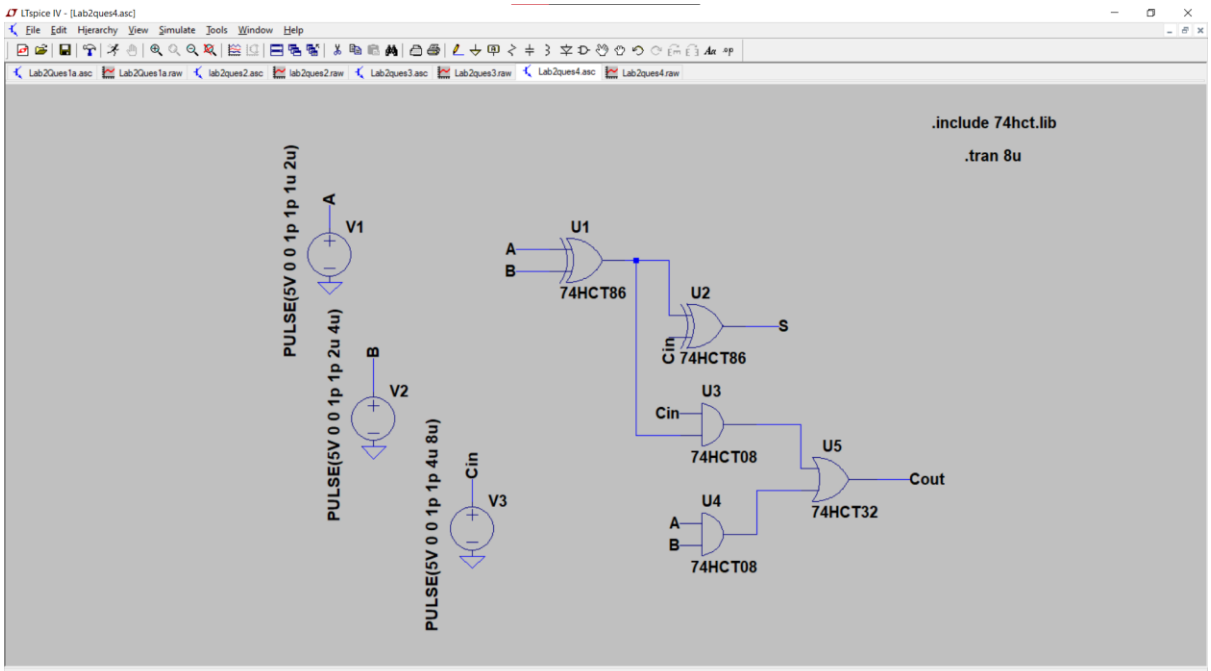

LTspice IV - [Lab2ques3.asc]
File Edit Hierarchy View Simulate Tools Window Help
Lab2Ques1a.asc Lab2Ques1a.raw lab2ques2.asc lab2ques2.raw Lab2ques3.asc Lab2ques3.raw Lab2ques4.asc Lab2ques4.raw
PULSE(5V 0 0 1p 1p 1u 2u)
V1
X
U1
X
Y
S
74HCT86
.include 74hct.lib
.tran 4u
PULSE(5V 0 0 1p 1p 2u 4u)
V2
Y
U2
X
Y
C
74HCT08

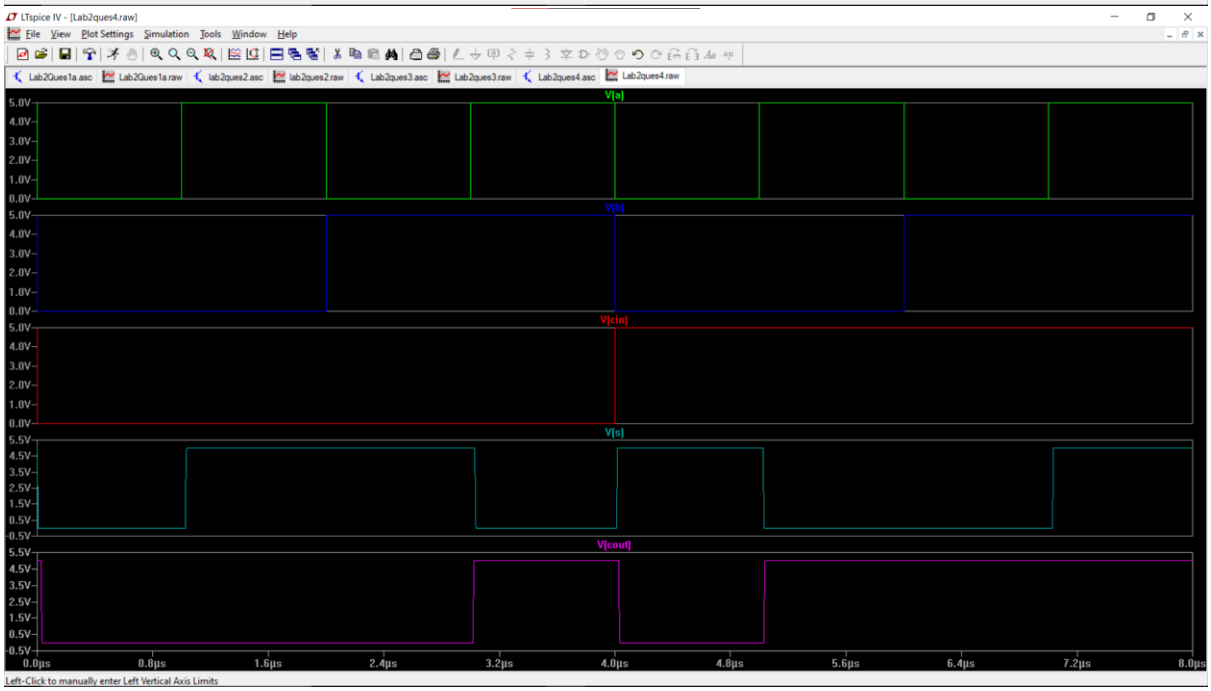

LTspice IV - [Lab2ques3.raw]
File View Plot Settings Simulation Tools Window Help
Lab2Ques1a.asc Lab2Ques1a.raw lab2ques2.asc lab2ques2.raw Lab2ques3.asc Lab2ques3.raw Lab2ques4.asc Lab2ques4.raw
V(x)
V(y)
V(s)
V(c)
0.0µs 0.4µs 0.8µs 1.2µs 1.6µs 2.0µs 2.4µs 2.8µs 3.2µs 3.6µs 4.0µs
Left-Click to manually enter Left Vertical Axis Limits

Problem 4:

Design and implement a two input Full- Adder circuit on LTSPICE platform.

(Provide proper LTSPICE model snapshot with neat levelling and show the graphical result containing the Inputs and Sum with Carry)


LTspice IV - [Lab2ques4.asc]
File Edit Hierarchy View Simulate Tools Window Help
Lab2Ques1a.asc Lab2Ques1a.raw lab2ques2.asc lab2ques2.raw Lab2ques3.asc Lab2ques3.raw Lab2ques4.asc Lab2ques4.raw
.include 74hct.lib
.tran 8u
A
V1
PULSE(5V 0 0 1p 1p 1u 2u)
B
V2
PULSE(5V 0 0 1p 1p 2u 4u)
Cin
V3
PULSE(5V 0 0 1p 1p 4u 8u)
U1
A
B
74HCT86
U2
Cin
74HCT86
S
U3
Cin
74HCT08
U4
A
B
74HCT08
U5
74HCT32
Cout


LTspice IV - [Lab2ques4.raw]
File View Plot Settings Simulation Tools Window Help
Lab2Ques1a.asc Lab2Ques1a.raw lab2ques2.asc lab2ques2.raw Lab2ques3.asc Lab2ques3.raw Lab2ques4.asc Lab2ques4.raw
V[a]
V[b]
V[cin]
V[s]
V[cout]
0.0µs 0.8µs 1.6µs 2.4µs 3.2µs 4.0µs 4.8µs 5.6µs 6.4µs 7.2µs 8.0µs
Left-Click to manually enter Left Vertical Axis Limits