CS/ECE/EEE/INSTR F215:Digital Design

Lecture 30: *Counters_2*

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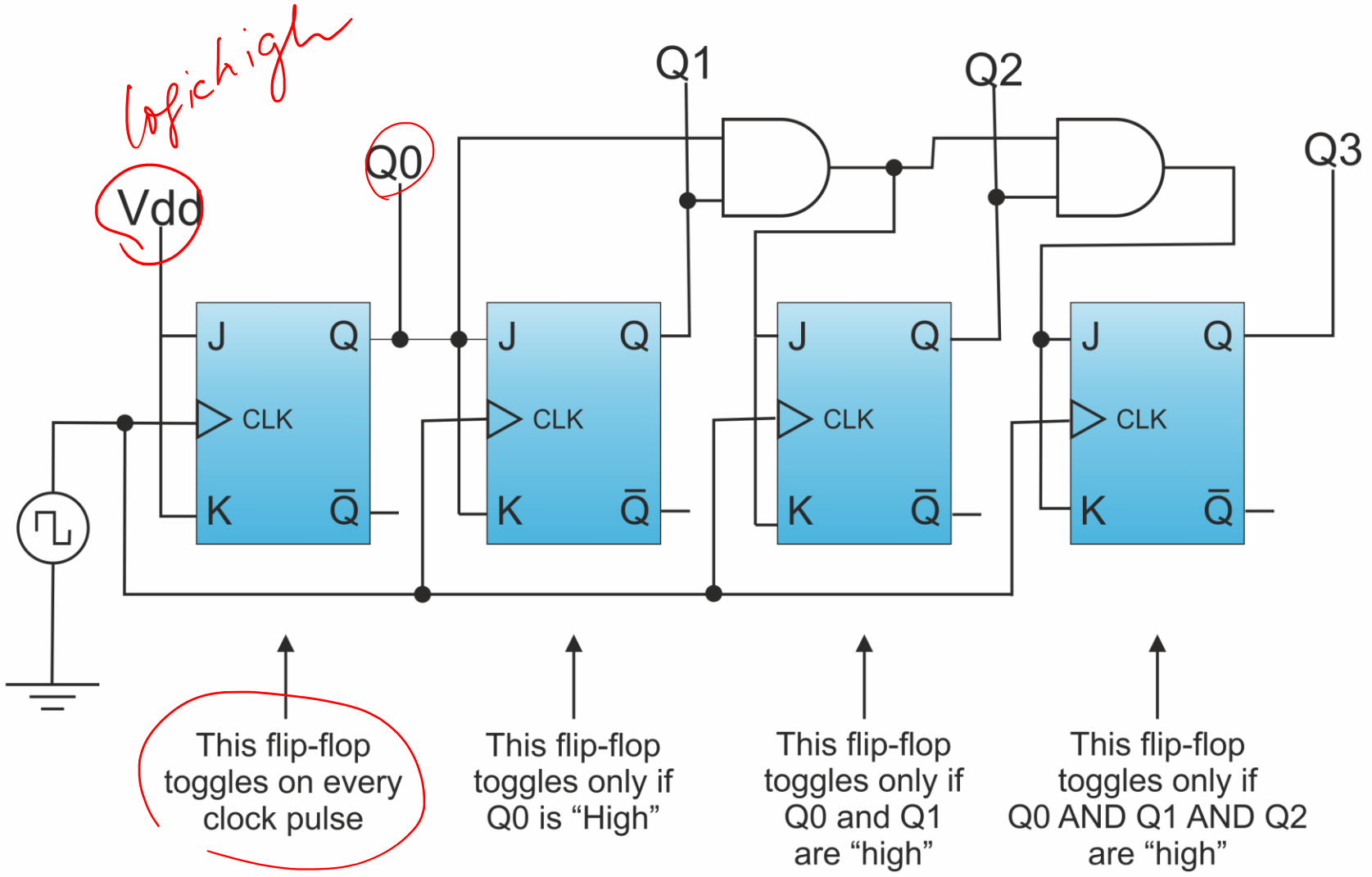
I find that the harder I work,
the more luck I seem to have.

-Thomas Jefferson

J-K Flip Flop Design of a 4-bit Binary Up Counter

Present state				Next state				Flip-flop inputs							
Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J_{Q3}	K_{Q3}	J_{Q2}	K_{Q2}	J_{Q1}	K_{Q1}	J_{Q0}	K_{Q0}
0	0	0	0	0	0	0	1	0	×	0	×	0	×	1	×
0	0	0	1	0	0	1	0	0	×	0	×	1	×	×	1
0	0	1	0	0	0	1	1	0	×	0	×	×	0	1	×
0	0	1	1	0	1	0	0	0	×	1	×	×	1	×	1
0	1	0	0	0	1	0	1	0	×	×	0	0	×	1	×
0	1	0	1	0	1	1	0	0	×	×	0	1	×	×	1
0	1	1	0	0	1	1	1	0	×	×	0	×	0	1	×
0	1	1	1	1	0	0	0	1	×	×	1	×	1	×	1
1	0	0	0	1	0	0	1	×	0	0	×	0	×	1	×
1	0	0	1	1	0	1	0	×	0	0	×	1	×	×	1
1	0	1	0	1	0	1	1	×	0	0	×	×	0	1	×
1	0	1	1	1	1	0	0	×	0	1	×	×	1	×	1
1	1	0	0	1	1	0	1	×	0	×	0	0	×	1	×
1	1	0	1	1	1	1	0	×	0	×	0	1	×	×	1
1	1	1	0	1	1	1	1	×	0	×	0	×	0	1	×
1	1	1	1	0	0	0	0	×	1	×	1	×	1	×	1

4-BIT SYNCHRONOUS "UP" COUNTER



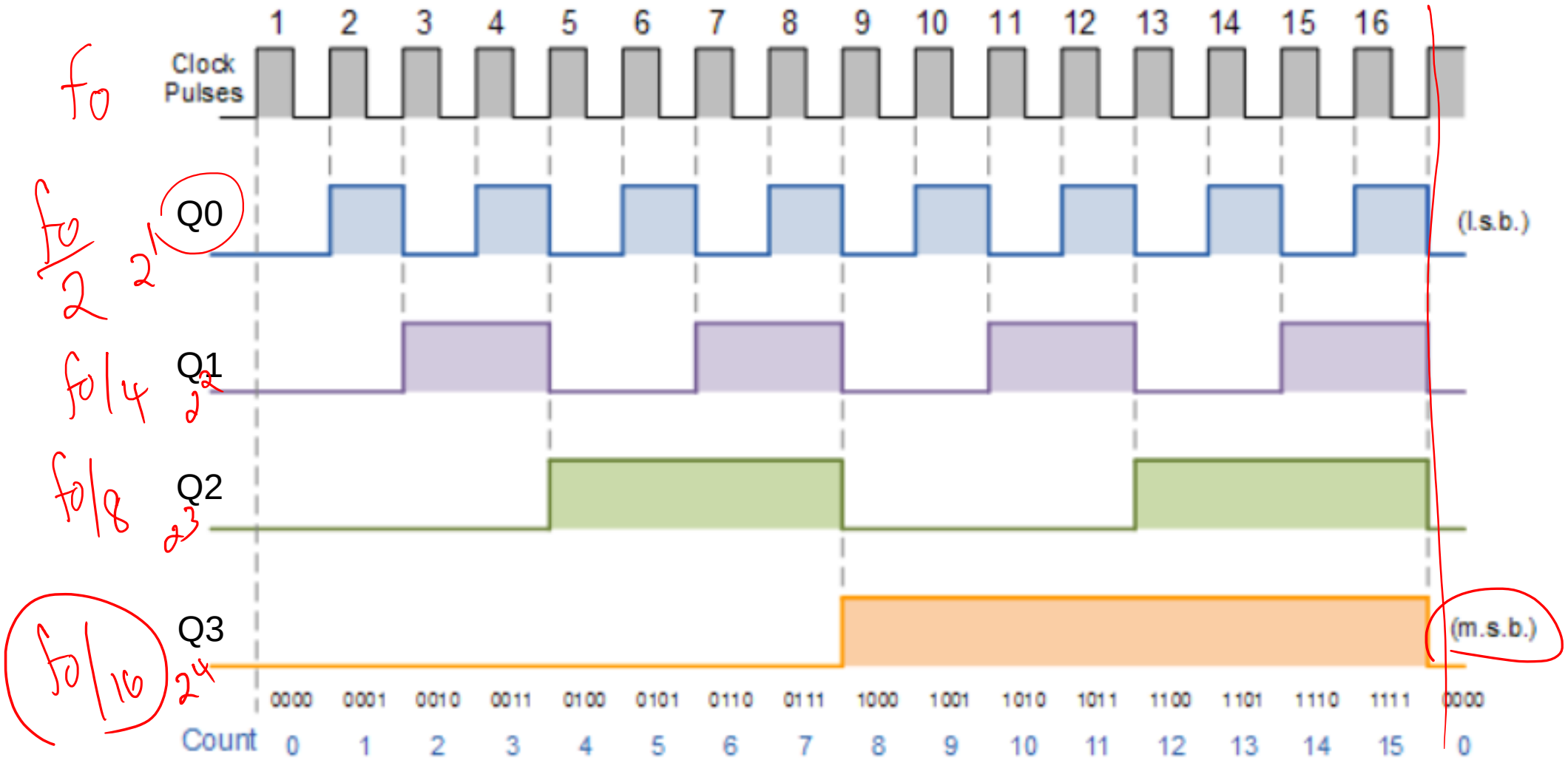
$J_{Q0} = 1$
$K_{Q0} = 1$

$J_{Q1} = Q_0$
$K_{Q1} = Q_0$

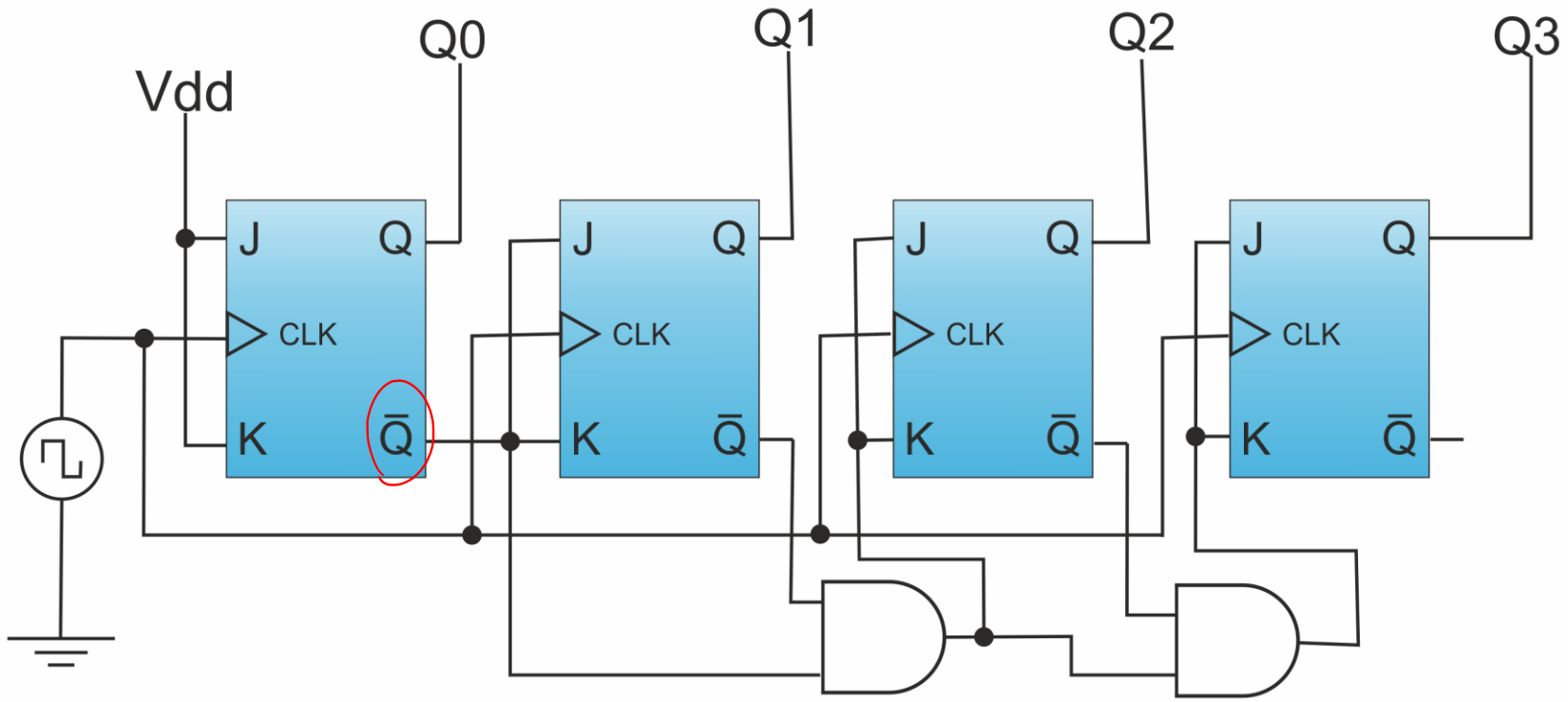
$J_{Q2} = Q_0 Q_1$
$K_{Q2} = Q_0 Q_1$

$J_{Q3} = Q_0 Q_1 Q_2$
$K_{Q3} = Q_0 Q_1 Q_2$

4-bit Synchronous Counter Waveform Timing Diagram



4-BIT SYNCHRONOUS “DOWN” COUNTER

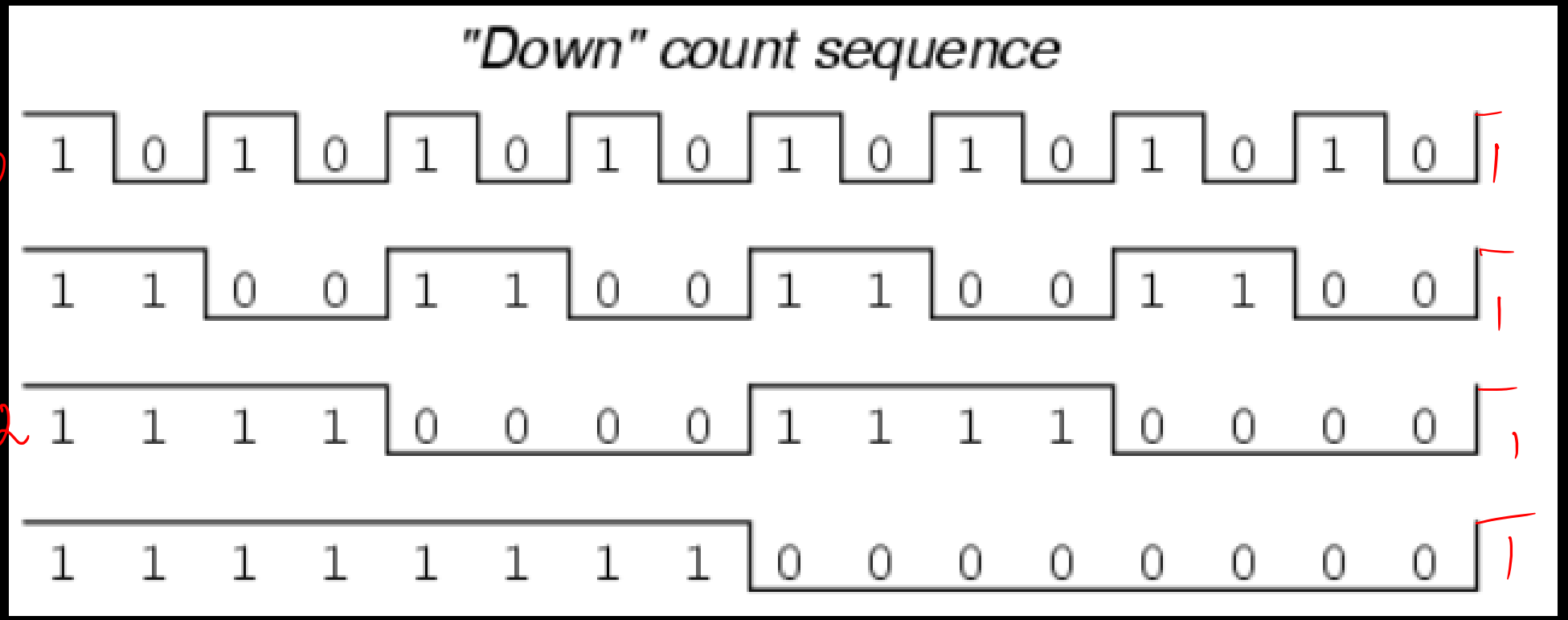


This flip-flop toggles on every clock pulse

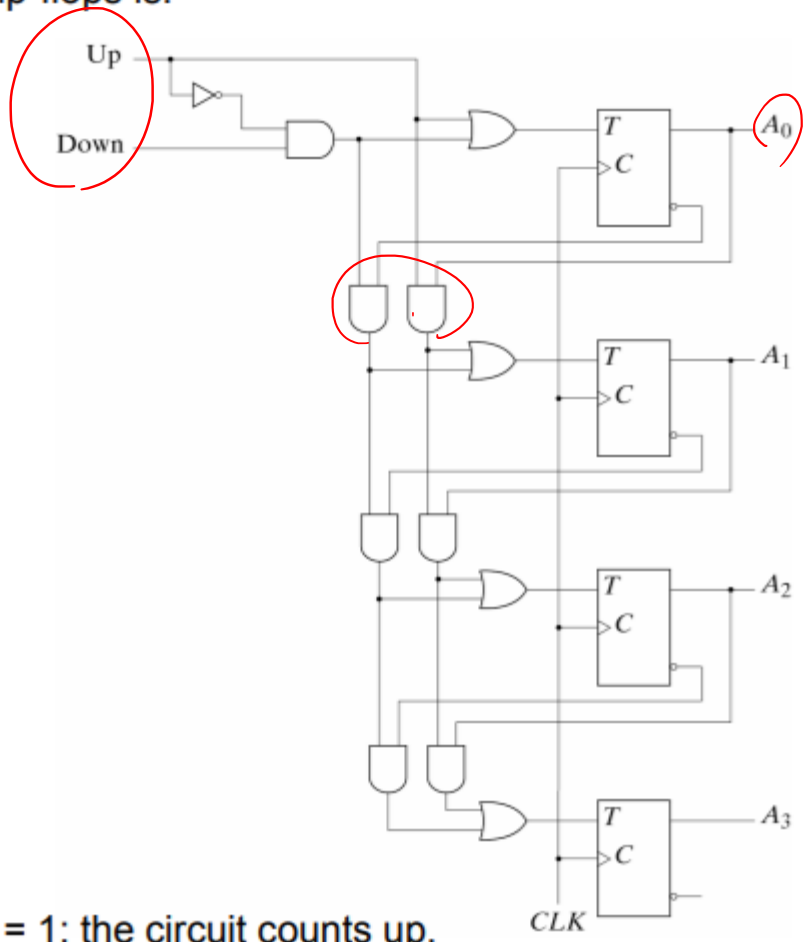
This flip-flop toggles only if $\overline{Q0}$ is “High”

This flip-flop toggles only if $\overline{Q0}$ and $\overline{Q1}$ are “high”

This flip-flop toggles only if $\overline{Q0}$ AND $\overline{Q1}$ AND $\overline{Q2}$ are “high”

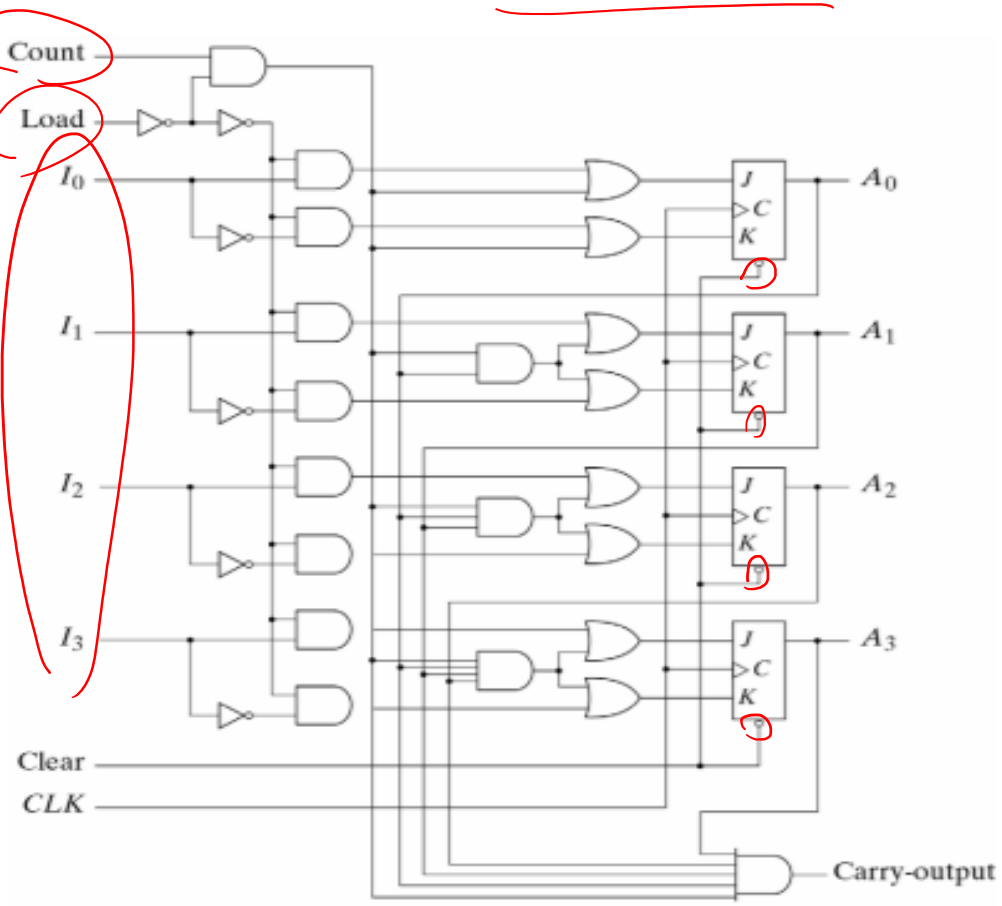

"Down" count sequence
Q0
1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0
Q1
1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0
Q2
1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0
Q3
1 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0

The circuit of a 4-bit up-down binary counter with *T* flip-flops is:



Up = 1; the circuit counts up.
Down = 1, *Up* = 0; the circuit counts down.
Up = 0, *Down* = 0; the circuit doesn't change state.
Up = 1, *Down* = 1, the circuit counts up.

A 4-bit binary counter with parallel load capability:

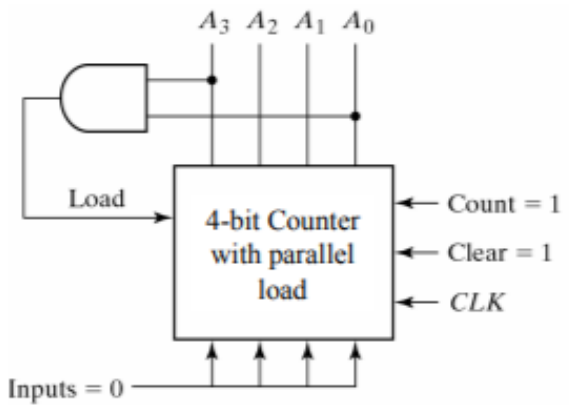


Its operation is summarized in the following table:

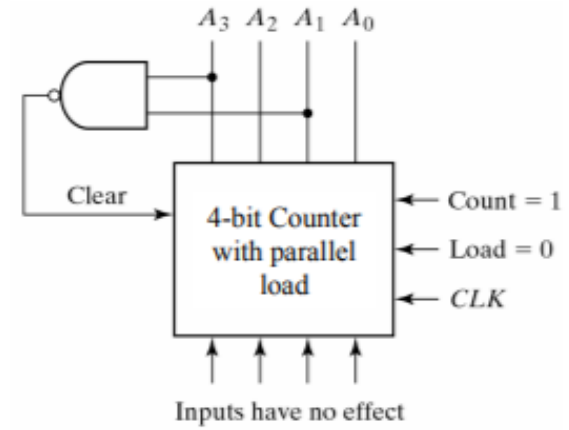
Clear	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

A counter with parallel load can be used to create any desired count sequence. For example, the 4-bit counter with parallel load shown previously can be used to generate a BCD count in two ways:

1. Using the load input:



2. Using the clear input:



BCD Counter using T ffs

0000 → 0001 → 0010 → 0011 → 0100 → 0101 → 0110 → 0111 → 1000 → 1001 → 0000

D ⇒ LSB

A ⇒ MSB

P.S

A	B	C	D
0	0	0	0
0	0	0	1
⋮			
0	1	1	1
1	0	0	0
1	0	0	1

N.S

A	B	C	D
0	0	0	1
0	0	1	0
⋮			
1	0	0	0
1	0	0	1
0	0	0	0

ff i/p's

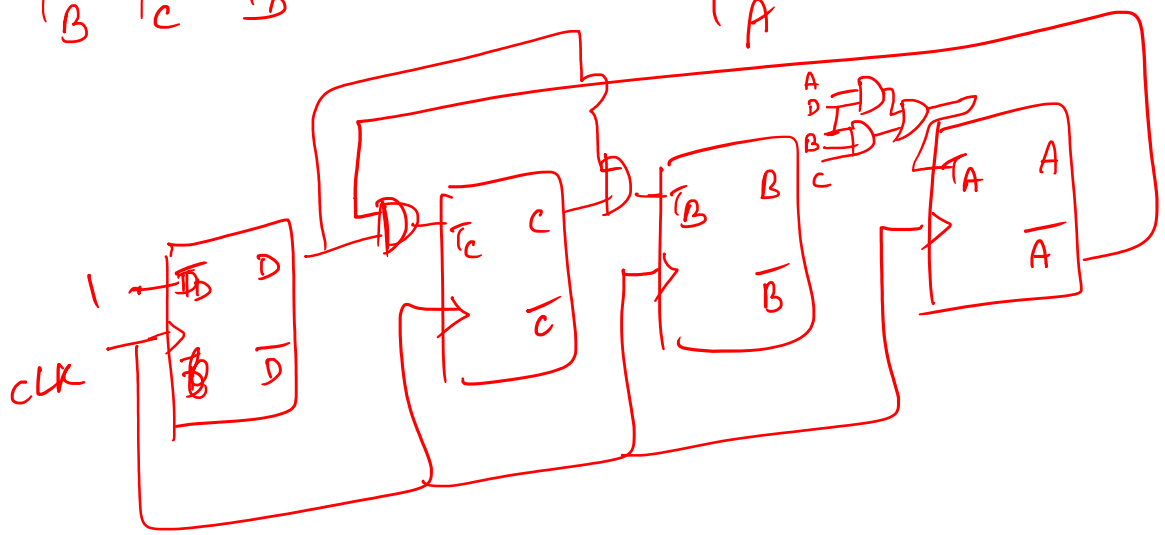
T_A T_B T_C T_D

$T_D = 1$

$T_C = \bar{A}D$

$T_B = CD$

$T_A = AD + BCD$



Mod-3 Counter

① 00 ⇒ ② 01 ⇒ ③ 10 ⇒ 00

P.S

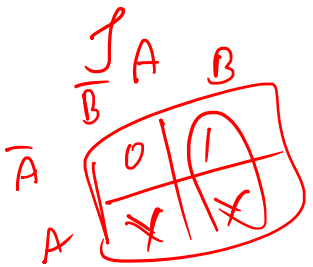
A	B
0	0
0	1
1	0
1	1

N.S

A	B
0	1
1	0
0	0
x	x

ff i/p

J_A	K_A	J_B	K_B
0	x	1	x
1	x	x	1
x	1	0	x
x	x	x	x



$J_A = B$

$J_B = \bar{A}$

$K_A = 1$

$K_B = 1$

using JK ffs

Mod 6

0, 1, 2, 3, 4, 5

using D ffs

$D_A = AC + B\bar{C}$

$D_B = \bar{A}C$

$D_C = 1$

Design a counter to go through the sequence 0, 1, 2, 4, 5, 6 & repeat

0, 1, 2, 4, 5, 6 and repeats

Counters with unused states

P.S A B C	N.S A B C	T_A	T_B	T_C
0 0 0	0 0 1	0	0	1
0 0 1	0 1 0	0	1	0
0 1 0	1 0 0	1	1	0
0 1 1	x x x	x	x	x
1 0 0	1 0 1	1	0	1
1 0 1	1 1 0	1	1	0
1 1 0	0 0 0	0	0	0
1 1 1	x x x	x	x	x

unused states

$T_A = B$

$T_B = B + C$

$T_C = \bar{B}$

Self Correcting Counter

P.S ABC ⇒ 011

$T_A = 1$ $T_B = 1$ $T_C = 0$

N.S ABC = 101

011

111

if P.S ABC ⇒ 111

$T_A = 1$ $T_B = 1$ $T_C = 0$

N.S ABC ⇒ 001

0, 1, 3, 7, 6, 4 & Repeats

T ffs

ff i/ps

P.S A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

N.S A	B	C
0	0	1
0	1	1
x	x	x
1	1	1
0	0	0
x	x	x
1	0	0

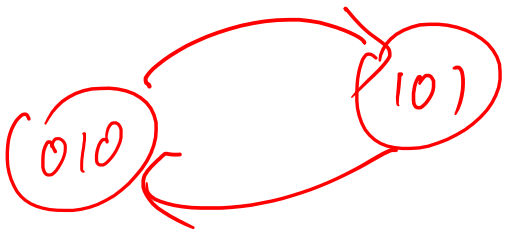
011

110

T_A	T_B	T_C
0	0	1
0	1	0
x	x	x
1	0	0
1	0	0
x	x	x
0	1	0
0	0	1

0, 1, 3, 7, 6, 4, 2

0 1 x 2 3 7 6 4



T_A

$\bar{A}$	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	0	1	X
A	1	X	0	0

$T_A = A \oplus B$

T_B

0	1	0	x	
0	x	0	1	

$T_B = B \oplus C$

T_C

1	0	0	x
0	x	1	0

$T_C = A \oplus C$

010 & 101

P.S ABC ⇒ 010

$T_A = 1$

$T_B = 1$

$T_C = 1$

N.S ABC ⇒ 101

P.S ABC ⇒ 101

$T_A = 1$

$T_B = 1$

$T_C = 1$

N.S ABC ⇒ 010