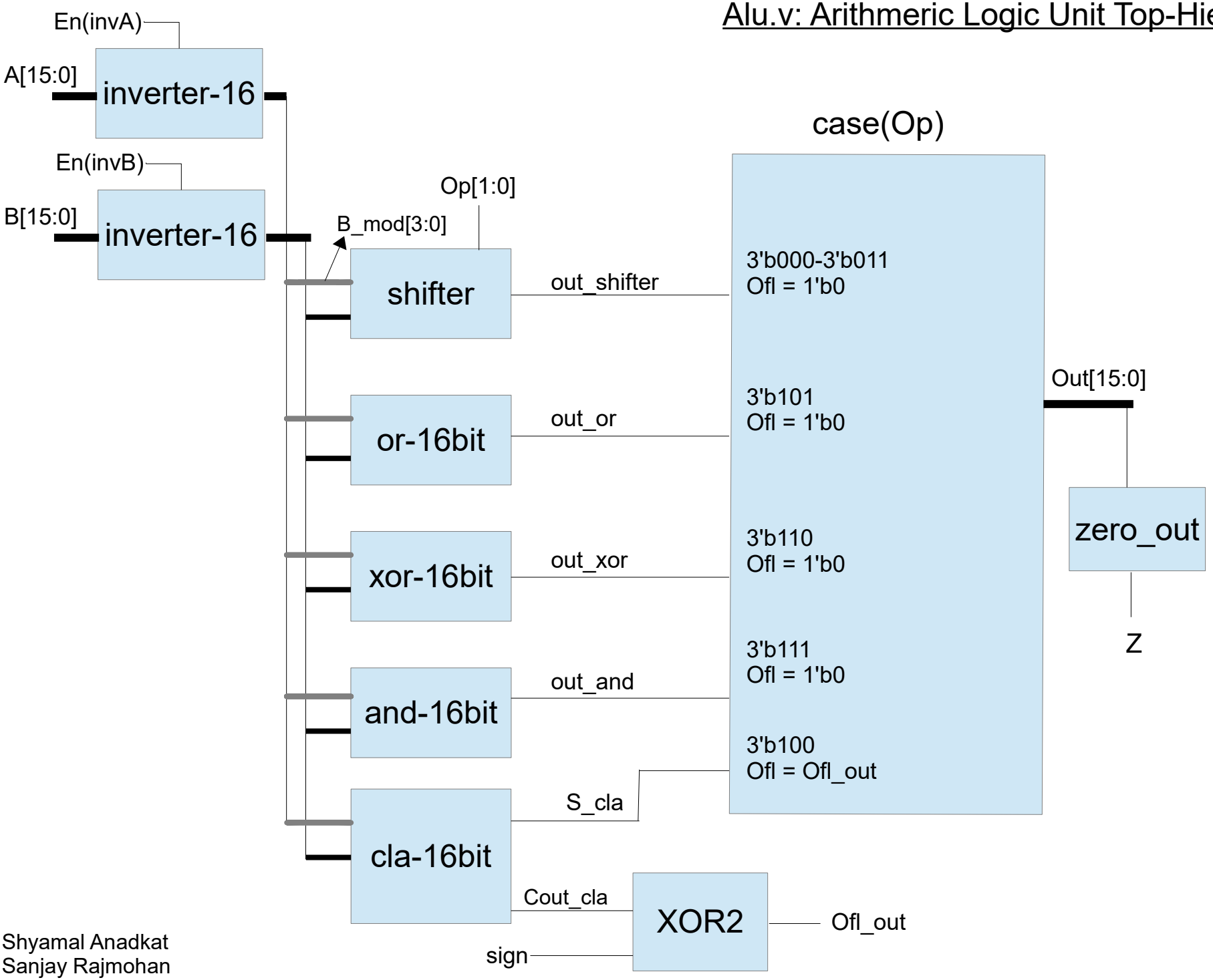
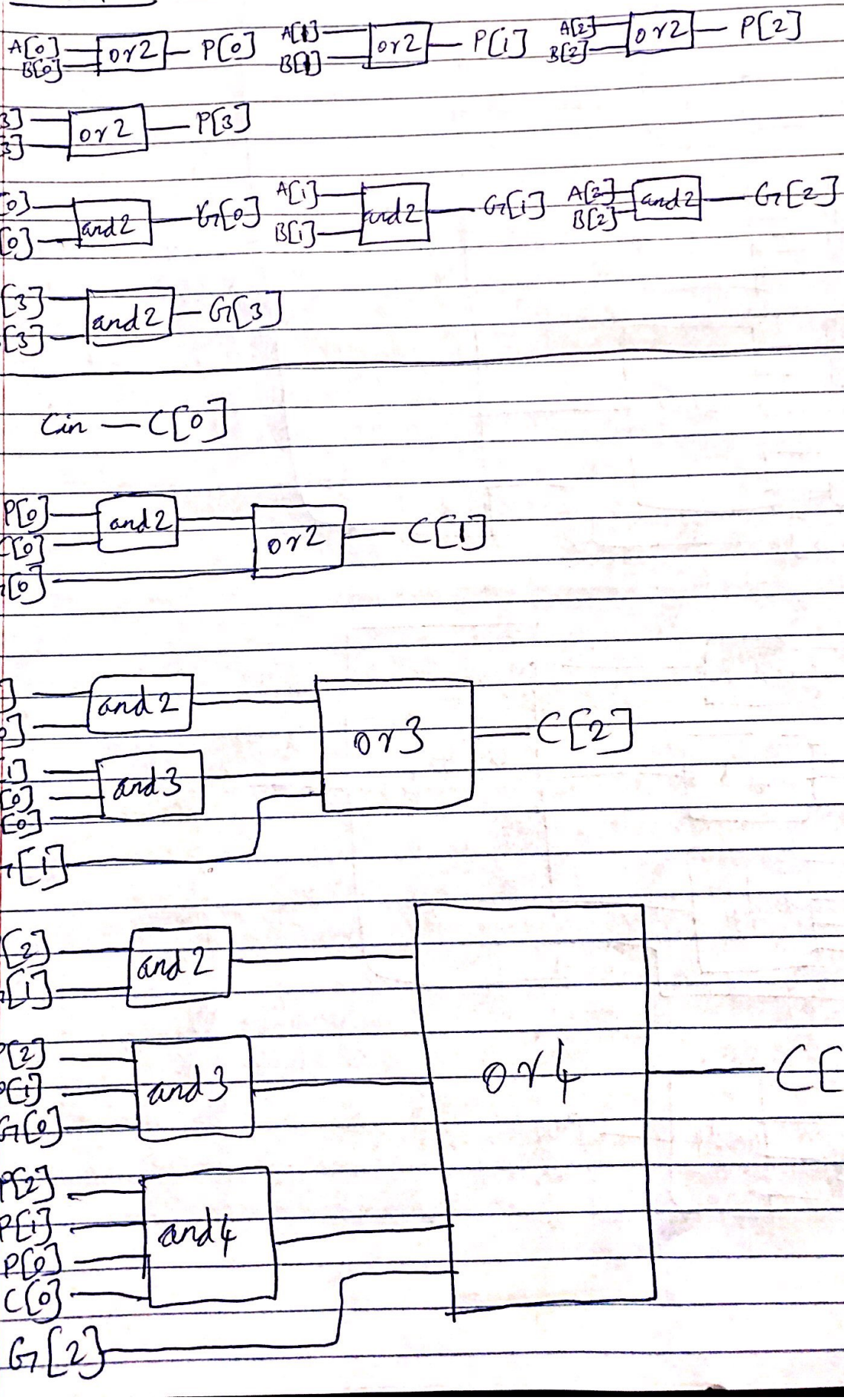
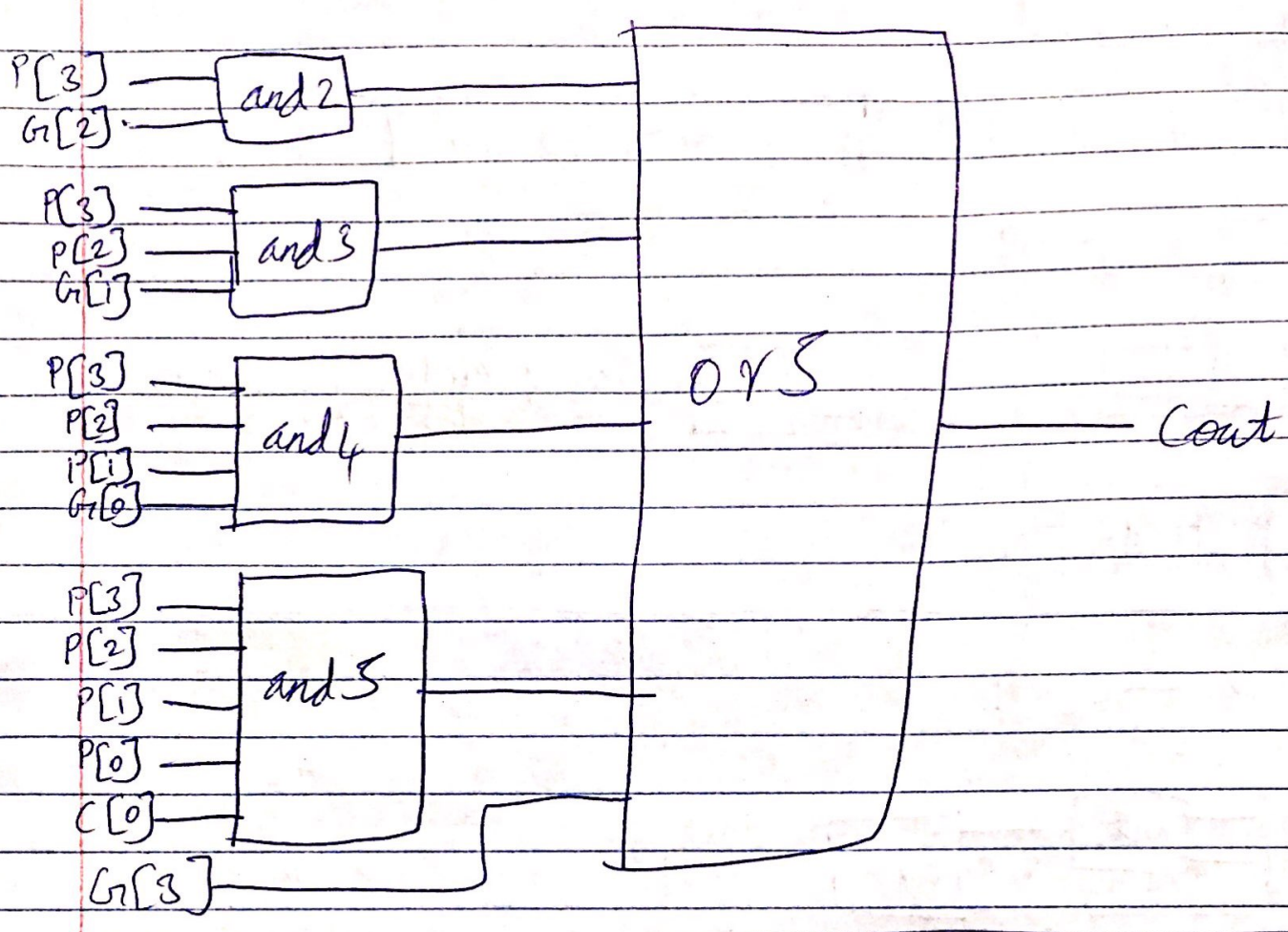
Alu.v: Arithmeric Logic Unit Top-Hier

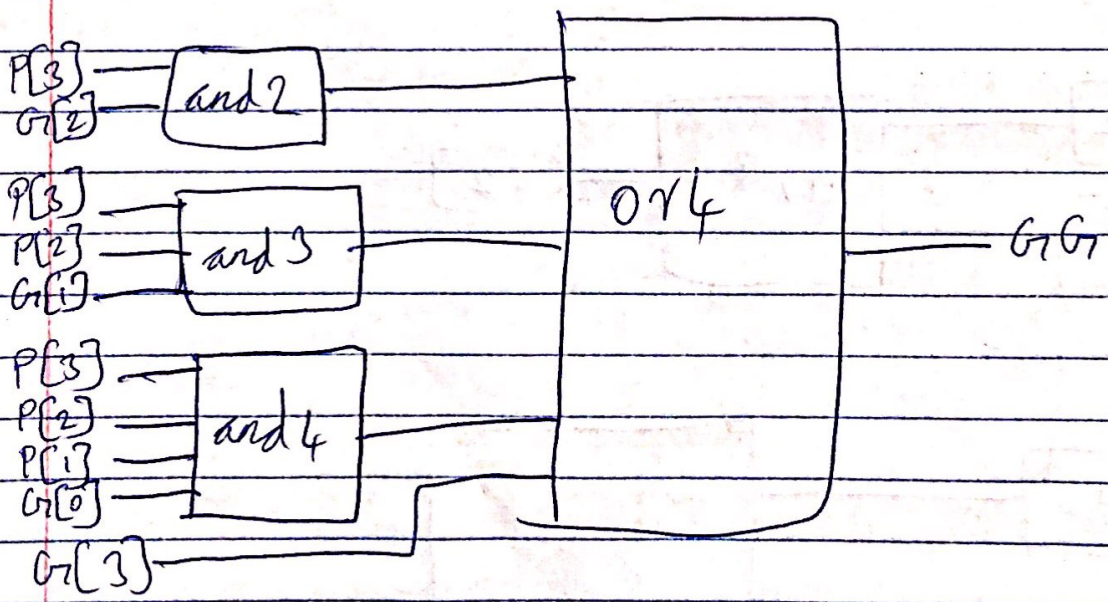


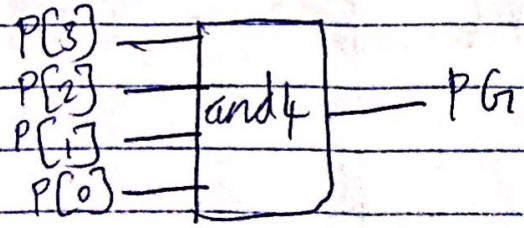
Shyamal Anadkat
Sanjay Rajmohan

CLA4: P[3:0] → Propagate, G[3:0] → Generate C[3:0] → Cinss

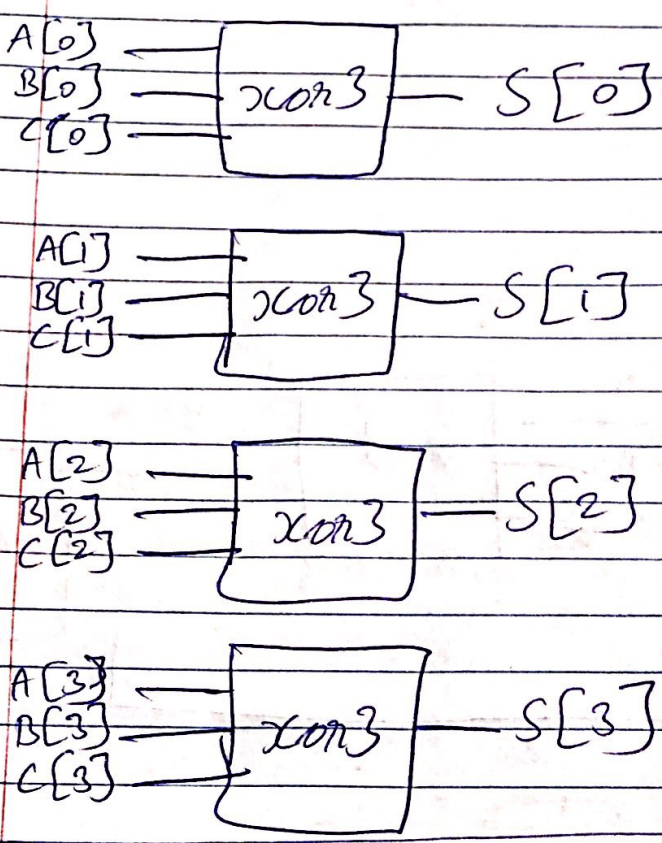






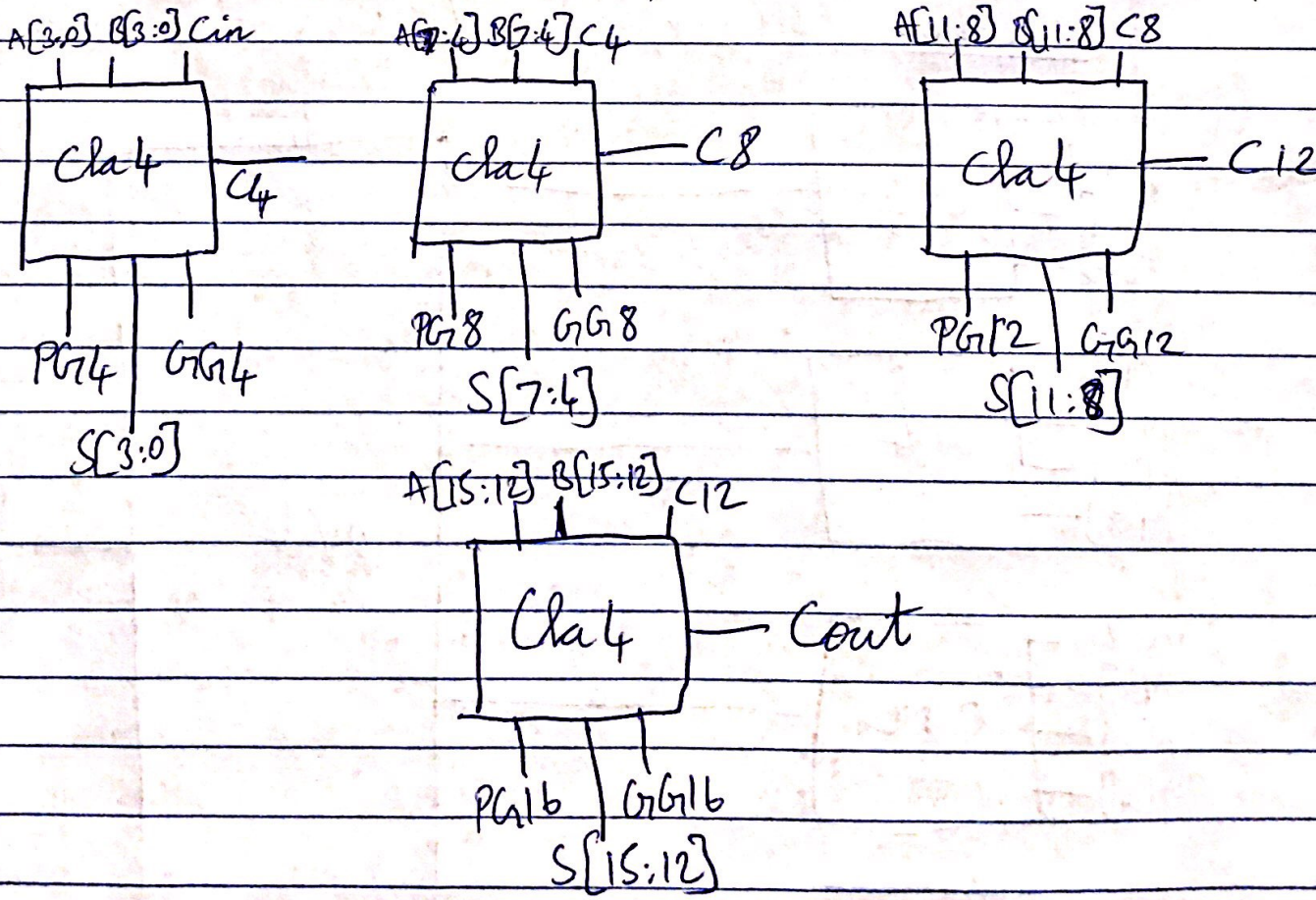


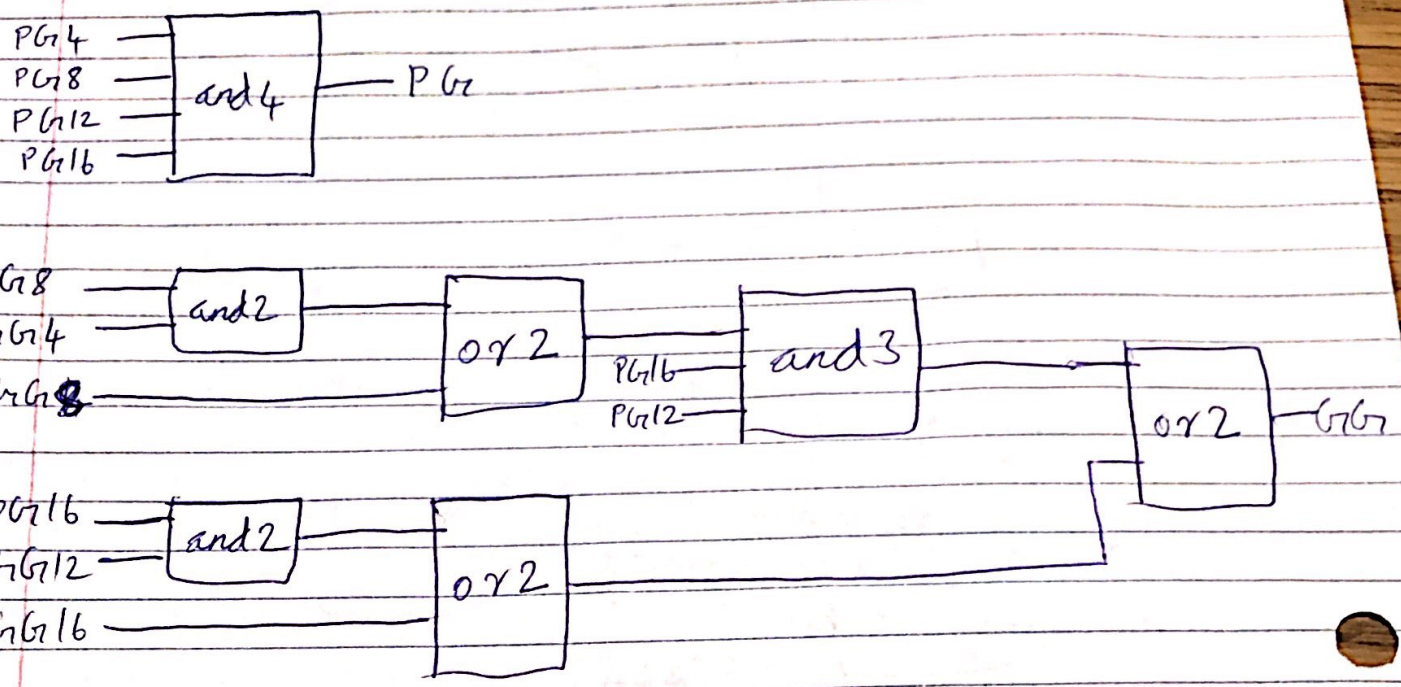
S[3:0] → Sum



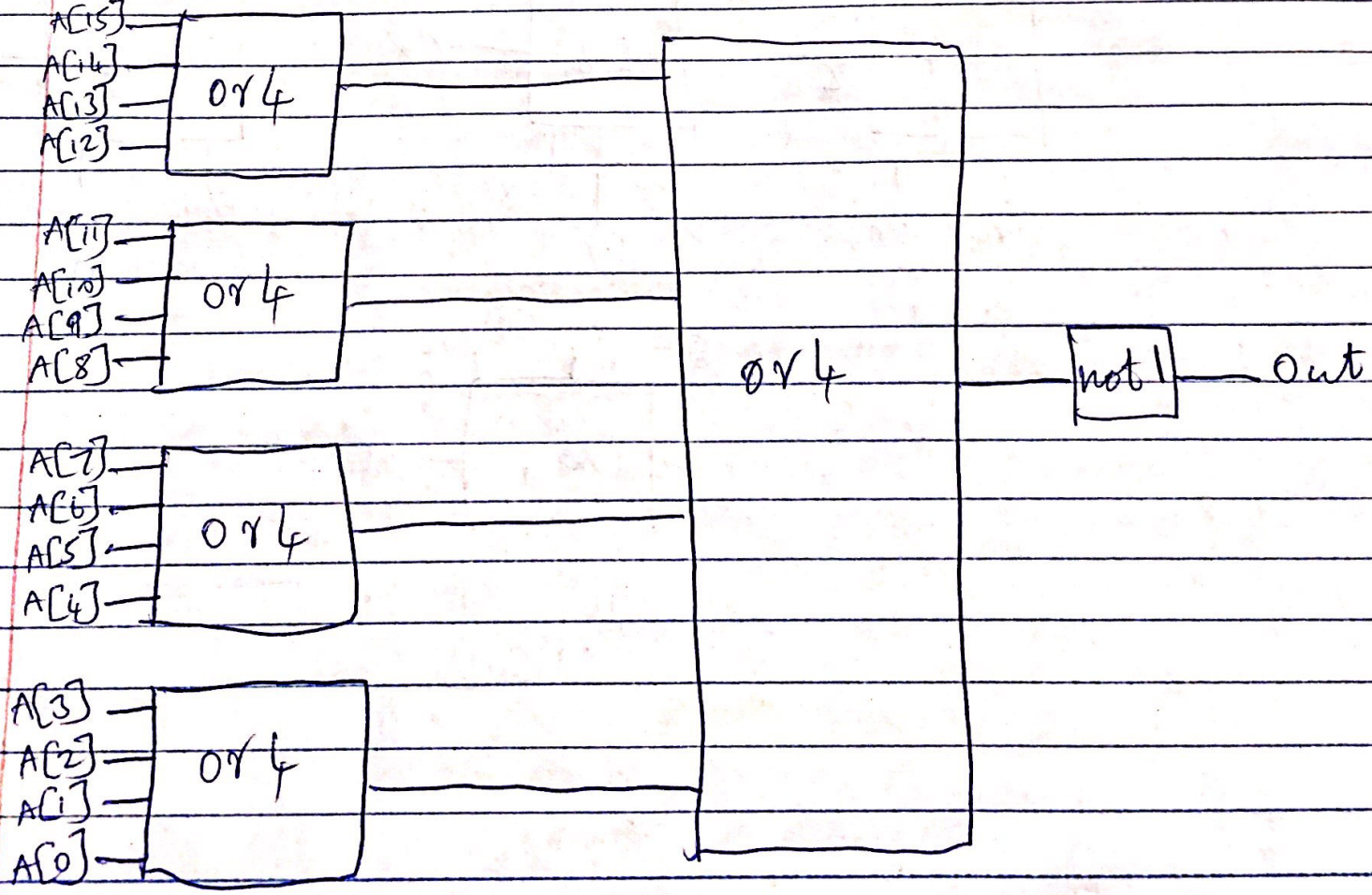
cla 16 :

C4, C8, C12 ⇒ Cout

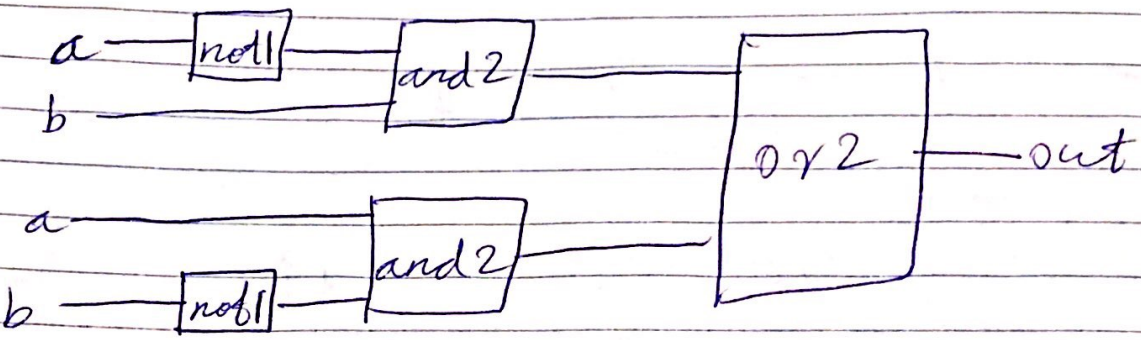




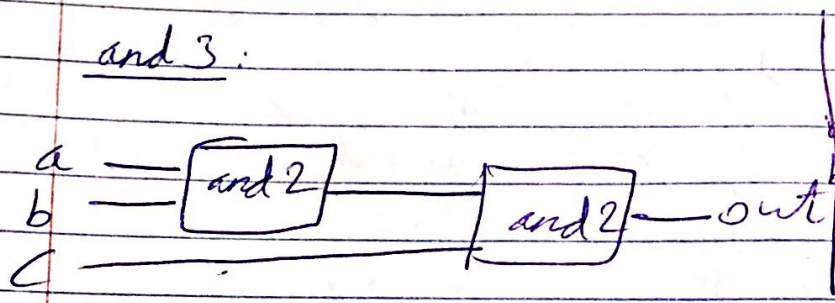
zero_out: Check if output is zero.



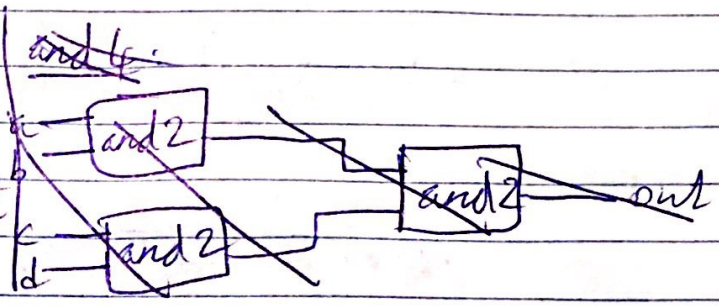
Xor2 (xor16 uses this)



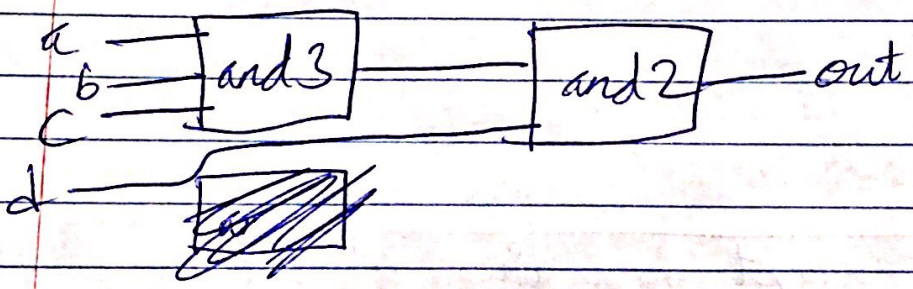
and3:



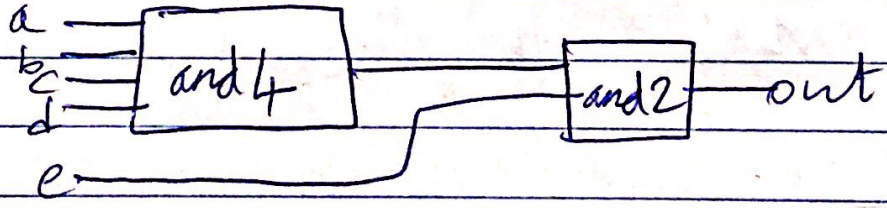
~~and4:~~



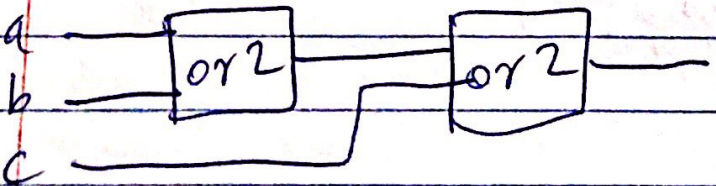
and4:



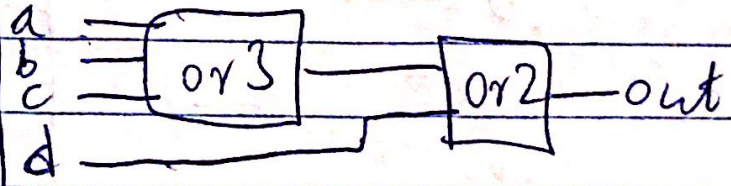
and5:



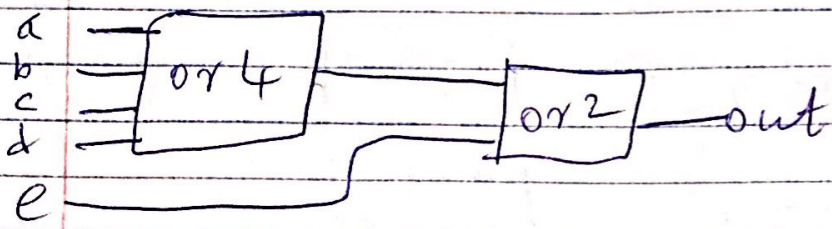
or3:



or4:



or5:



(or16 uses or2, and 16 uses and2).

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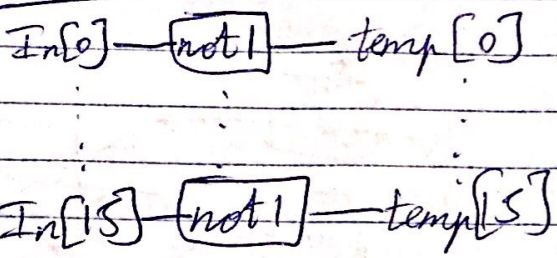
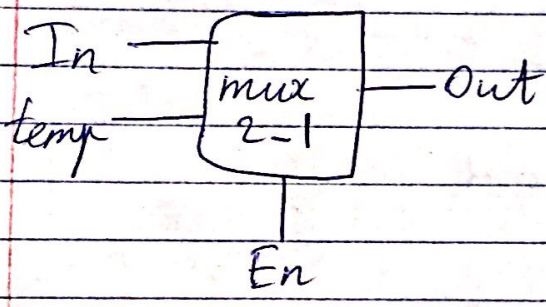
inv16:

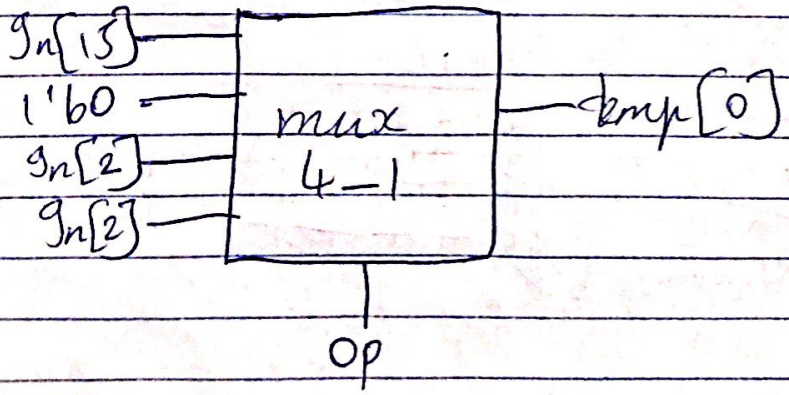




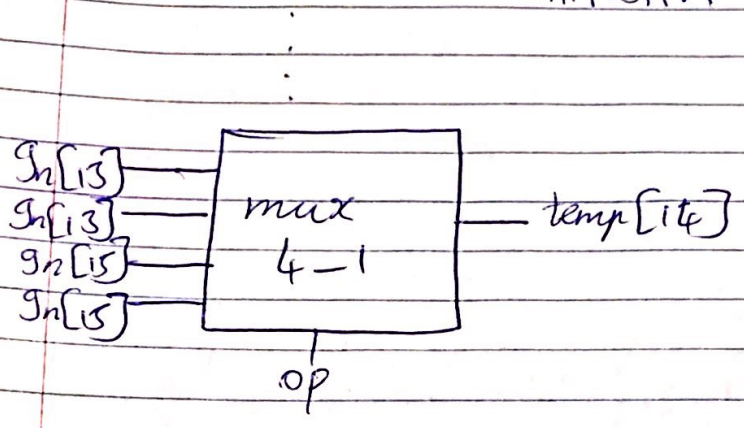
Shifters similar except how they start (Eg. shifter1 starts with In[15] and 1'b0).

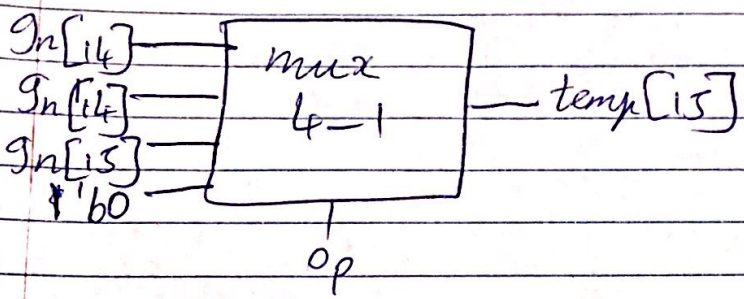
Shifter2 starts with In[14], 1'b0 and In[15], 1'b0

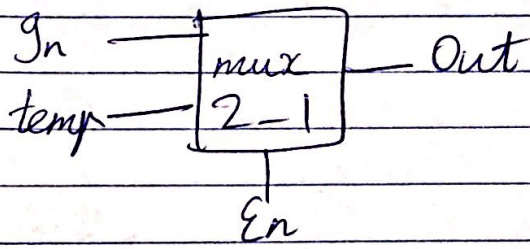
Shifter1:



shifter1.v







In shifter2, last 2 D inputs of mux4-1 are zeros.
In shifter4, last 4 D inputs of mux4-1 are zeros.
Similarly, for shifter8, last 8 are zeros.