CalSci – Open Source IoT Hardware Platform

Introduction

CalSci is an open-source IoT platform powered by theESP32-S3, combining a physical keyboard, display, and external GPIO access into a single modular device. Designed for developers, students, and makers, it functions as both astandalone embedded computer and an extendable tool forIoT experimentation. With wireless connectivity (Wi-Fi + BLE),onboard processing, and a developer-friendly SDK, CalSci bridges the gap between prototyping boards and fully interactive smart devices.

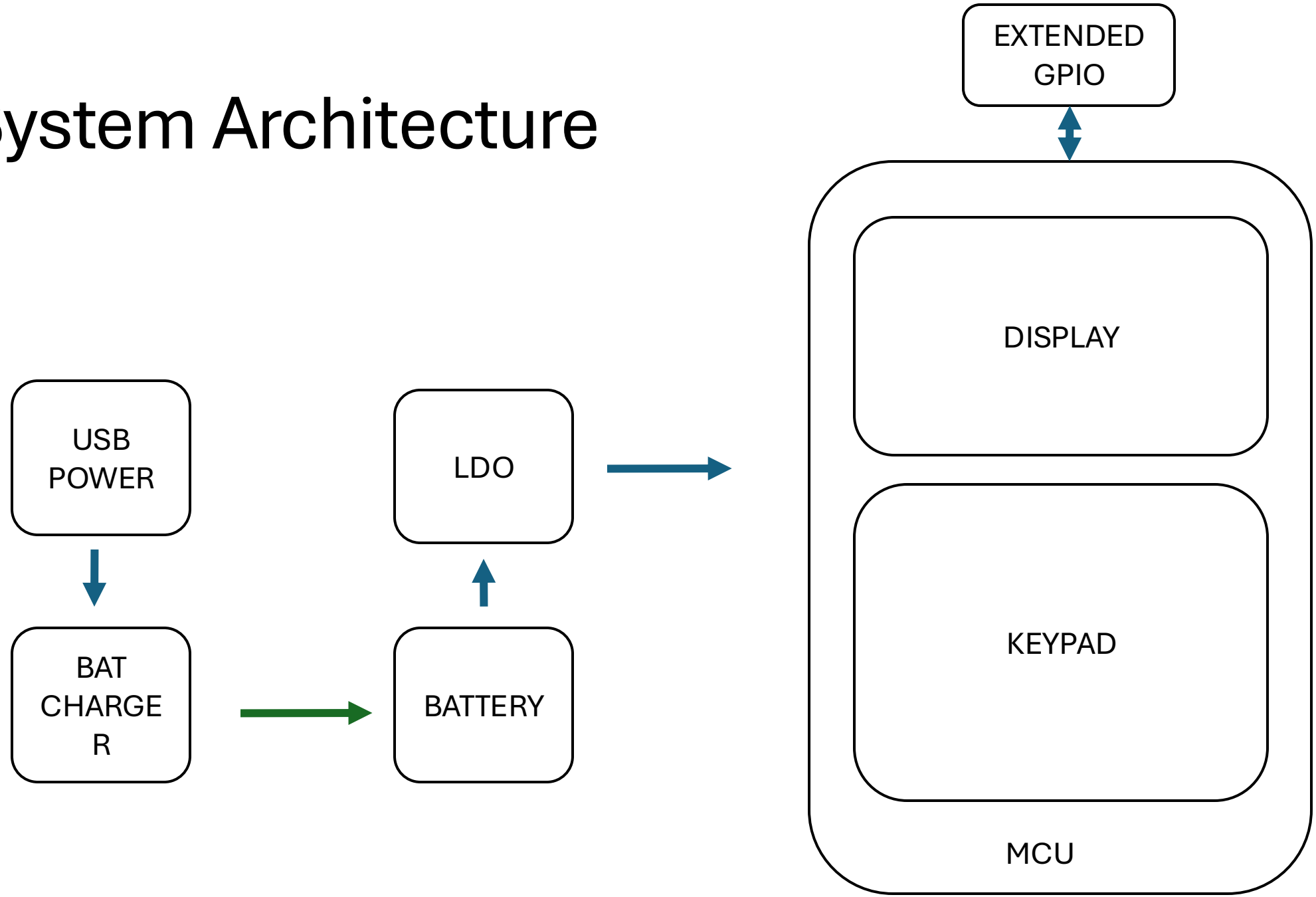
Main Features

- **ESP32-S3 Core:** Dual-core processor with Wi-Fi and Bluetooth for IoT applications.
- **Integrated Interface:** Built-in display and tactile keyboard for local interaction.
- **External GPIO Access:** Easily connect sensors, actuators, or expansion modules.
- **Developer Tools:** VS Code extension, SDK, and WebREPL for fast programming and debugging.
- **Open-Source Design:** Hardware and firmware are fully customizable and community-driven.

Objective

- CalSci was created to simplify the process of developing and experimenting with embedded systems by integrating both hardware and software into a single, ready-to-use platform. Traditional development boards require multiple external components—keyboards, displays, and interface modules—just to test simple ideas. CalSci solves this by providing everything on one board, allowing developers to code, test, and interact with their projects instantly.
- Unlike typical IoT boards, CalSci is designed as a **complete embedded computing device**, not just a controller. It demonstrates seamless hardware–software integration while remaining open-source and modular. This makes it ideal for learning, prototyping, and rapid deployment—bridging the gap between **educational tools, developer kits, and real-world IoT devices.**

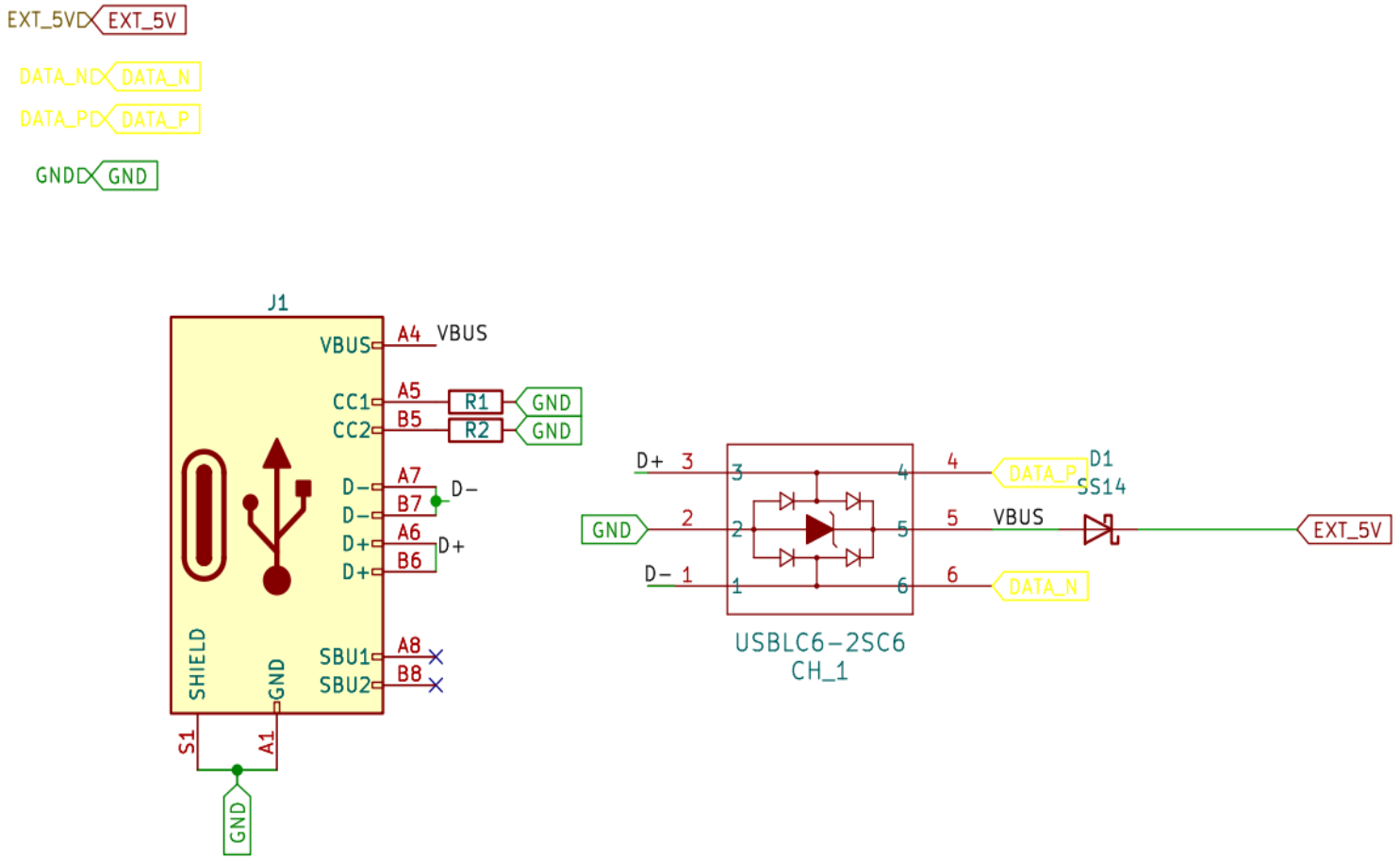
System Architecture



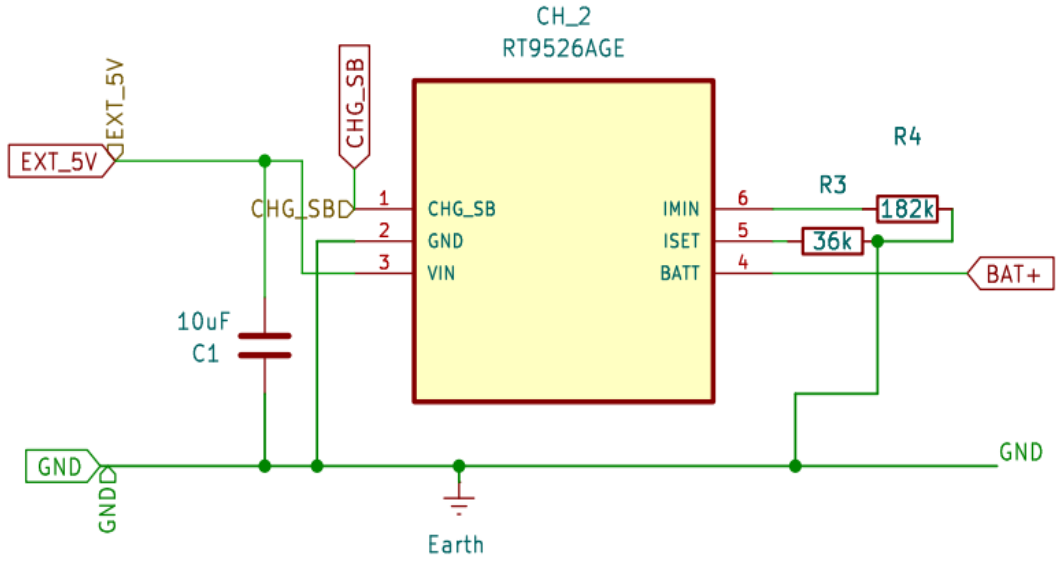
Circuit Design

USB

The USB Type-C input stage consists of connector **J1**, which provides **VBUS (5 V)**, **D+**, **D–**, and **CC1/CC2** lines, each terminated with pull-down resistors **R1** and **R2** for proper Type-C device configuration. The **USBLC6-2SC6** ESD protection array safeguards the differential data lines from voltage transients, ensuring signal integrity and compliance with USB standards. A **SS14 Schottky diode (D1)** isolates and protects the external **EXT_5V** rail from reverse current while maintaining a low forward voltage drop. The resulting outputs — **DATA_P**, **DATA_N**, **EXT_5V**, and **GND** — provide protected, stable USB power and data connectivity to the ESP32-S3 subsystem for programming, communication, and power input.



BATTERY CHARGER



The **RT9526AGE** is a linear single-cell Li-ion battery charger IC that manages the entire charging process from the **EXT_5V** input. The **VIN** pin receives the 5 V input, filtered by a **10 µF capacitor (C1)**, while the **BATT** pin provides regulated charging to the battery. The **ISET** pin sets the fast-charge current using an external resistor **R3 (36 kΩ)** connected between ISET and GND, calculated by the formula

$$I_{CHG\_FAST} = K_{ISET} \times \frac{V_{ISET}}{R_{ISET}}$$

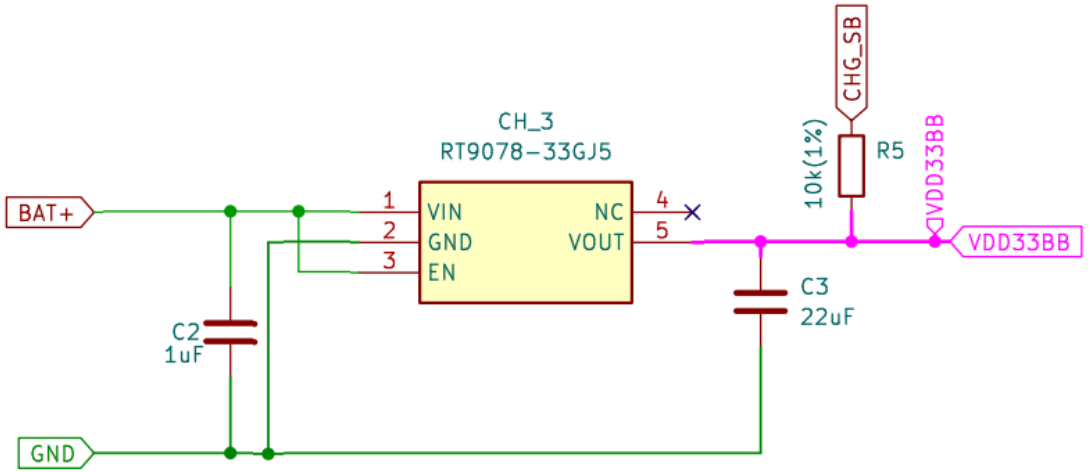
where $K_{ISET} = 9959$ and $V_{ISET} = 1.22V\,(typ.)$, resulting in a **fast-charge current of ≈ 337 mA**. The **IMIN** pin programs the **End-of-Charge (EOC)** current through resistor **R4 (182 kΩ)**, following

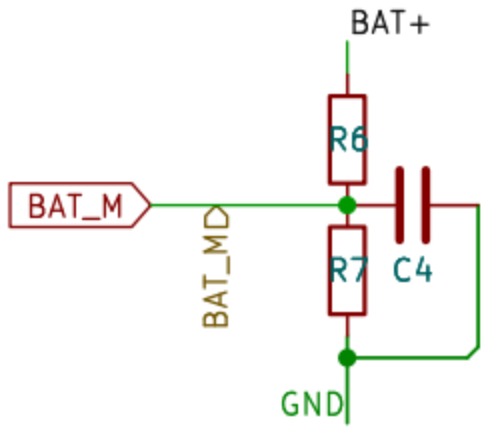
$$I_{IMIN} = \frac{10935}{R_{IMIN}}\,(mA)$$

which yields an **EOC current of ≈ 60 mA**. Upon reaching EOC, the charger maintains a constant **4.2 V** output while signaling charge completion via the **CHG_SB** pin, which transitions **high** from its initial **low** state during trickle charging. The **CHG_SB** signal resets automatically if the charge current rises above **75% of the programmed fast-charge level**, enabling intelligent recharge control. This configuration ensures stable, safe, and efficient Li-ion charging with built-in current regulation, voltage control, and charge-status indication for the CalSci system.

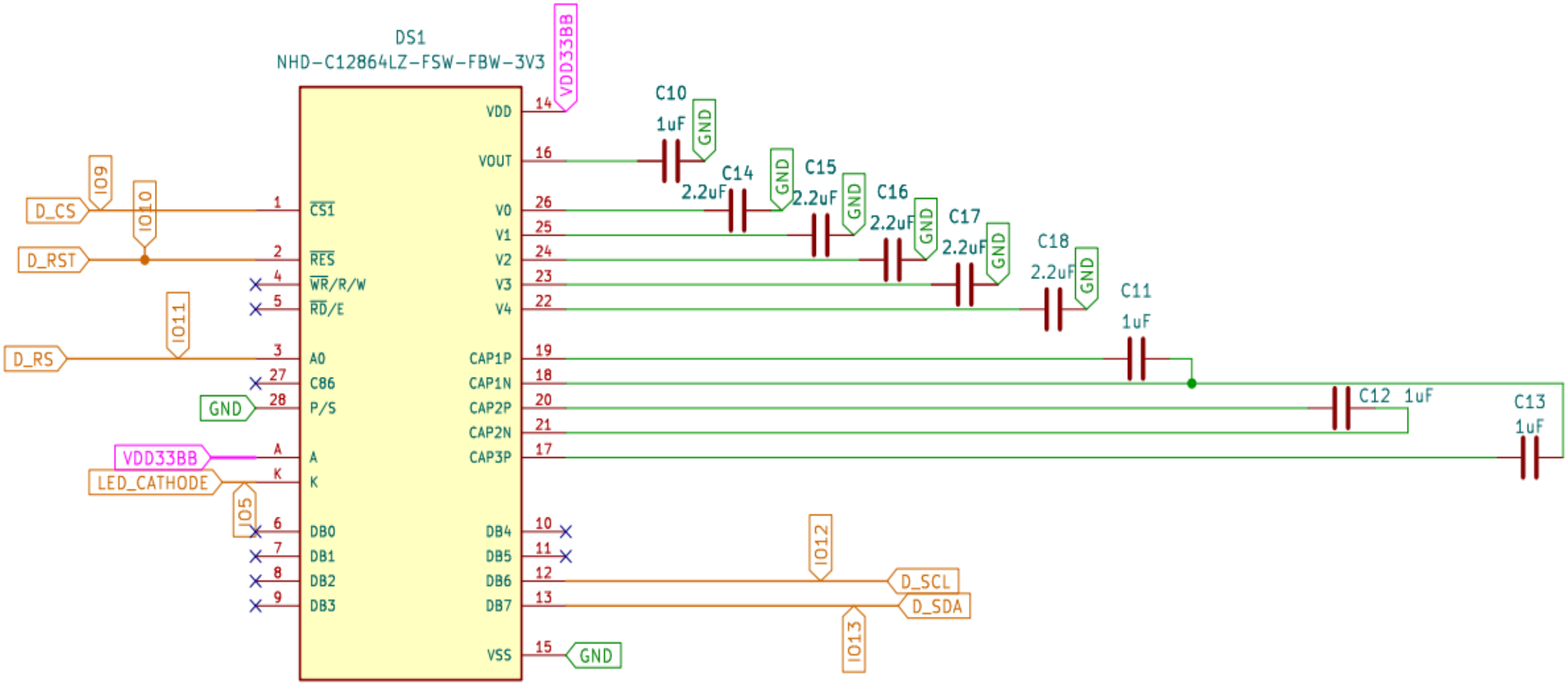
BATTERY AND LDO

The **BAT+** node is the single-cell battery output, decoupled to ground with **C2 (1 µF)** for input stability. Battery voltage is monitored via a resistor divider (**R6 / R7**) and filtered by **C4** on the **BAT_M** net to provide a smooth battery measurement input to the microcontroller/ADC. The low-dropout regulator **RT9078-33GJ5** (CH_3) is used as the 3.3 V power rail generator: its **VIN** is tied to **BAT+**, **EN** is enabled when battery power is present, and the regulator's output **VOUT** is decoupled by **C3 (22 µF)** to produce **VDD33BB**. The charger status pin **CHG_SB** is pulled up to **VDD33BB** through **R5 (10 kΩ)** so the system can read charge-state (active low during charge, high at EOC). This arrangement provides stable battery sensing, a battery-powered 3.3 V rail, and a simple charge-status interface for the CalSci power subsystem.



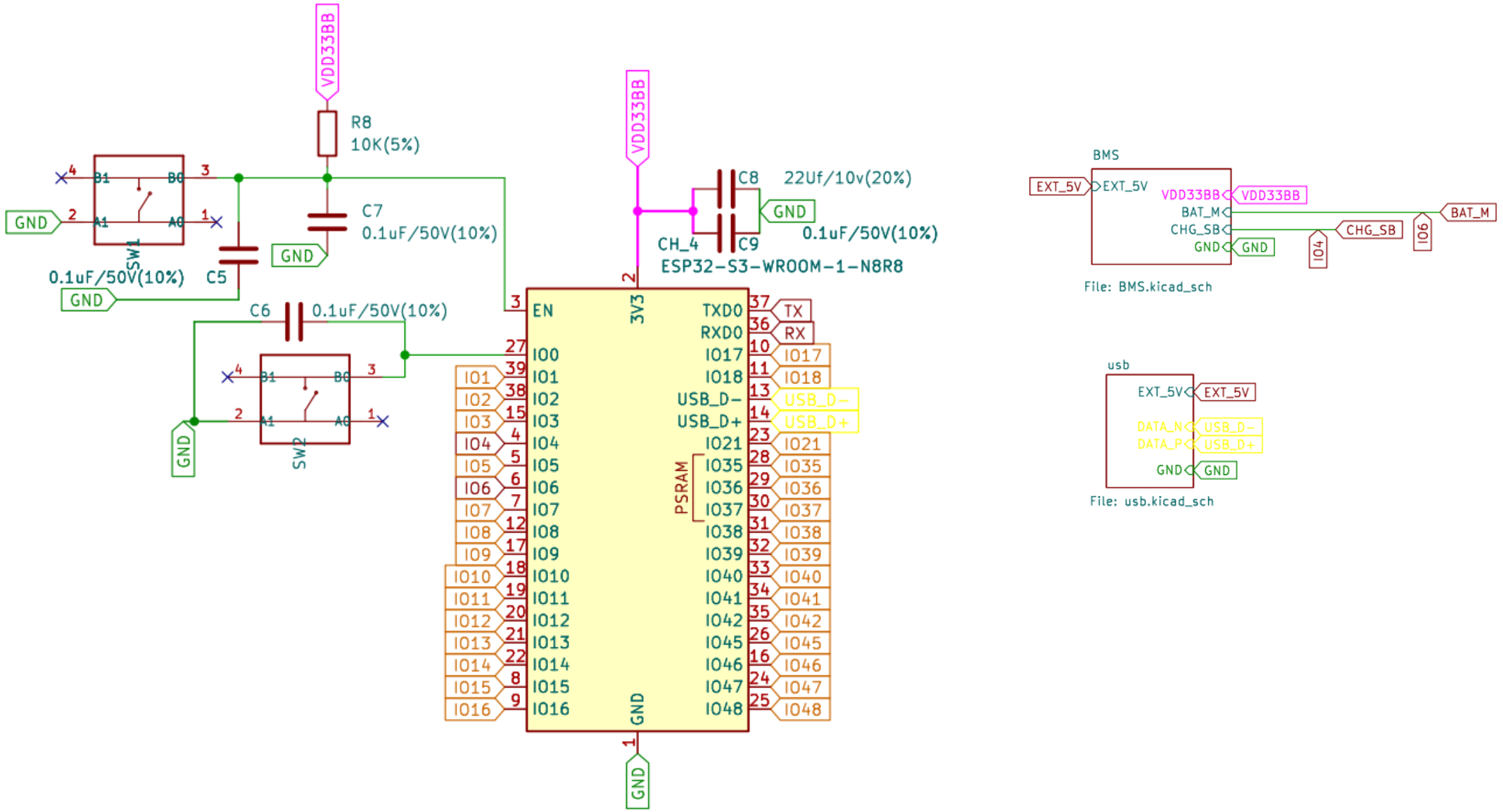


DISPLAY


DS1
NHD-C12864LZ-FSW-FBW-3V3
VDD33BB
VDD
VOUT
VSS
CS1
RES
WR/R/W
RD/E
A0
C86
P/S
A
K
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
V0
V1
V2
V3
V4
CAP1P
CAP1N
CAP2P
CAP2N
CAP3P
D_CS
D_RST
D_RS
GND
VDD33BB
LED_CATHODE
IO9
IO10
IO11
IO5
IO12
IO13
D_SCL
D_SDA
C10
1uF
C14
2.2uF
C15
2.2uF
C16
2.2uF
C17
2.2uF
C18
2.2uF
C11
1uF
C12
1uF
C13
1uF

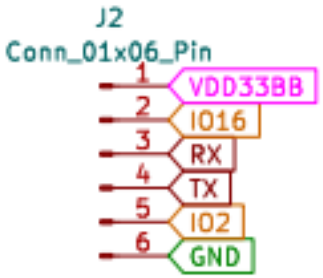
The external capacitors are essential for the $\mathrm{ST7565}$'s integrated power supply. The $1\mu\mathrm{F}$ **capacitor (**$\mathrm{C10}$**)** connected to the VDD pin provides necessary **power supply decoupling** for the digital logic. The three $1\mu\mathrm{F}$ **capacitors (**$\mathrm{C11}$**,** $\mathrm{C12}$**,** $\mathrm{C13}$**)** are mandatory for the operation of the **charge pump (voltage booster)**, generating the high-voltage potential required for LCD driving (VOUT). Finally, the five $2.2\mu\mathrm{F}$ **capacitors (**$\mathrm{C14}$**–**$\mathrm{C18}$**)** are placed on the VOUT and regulator outputs ($\mathrm{V1}$ to $\mathrm{V5}$) to function as **decoupling components**, ensuring ripple suppression and the stability of the LCD bias voltages for proper display contrast.

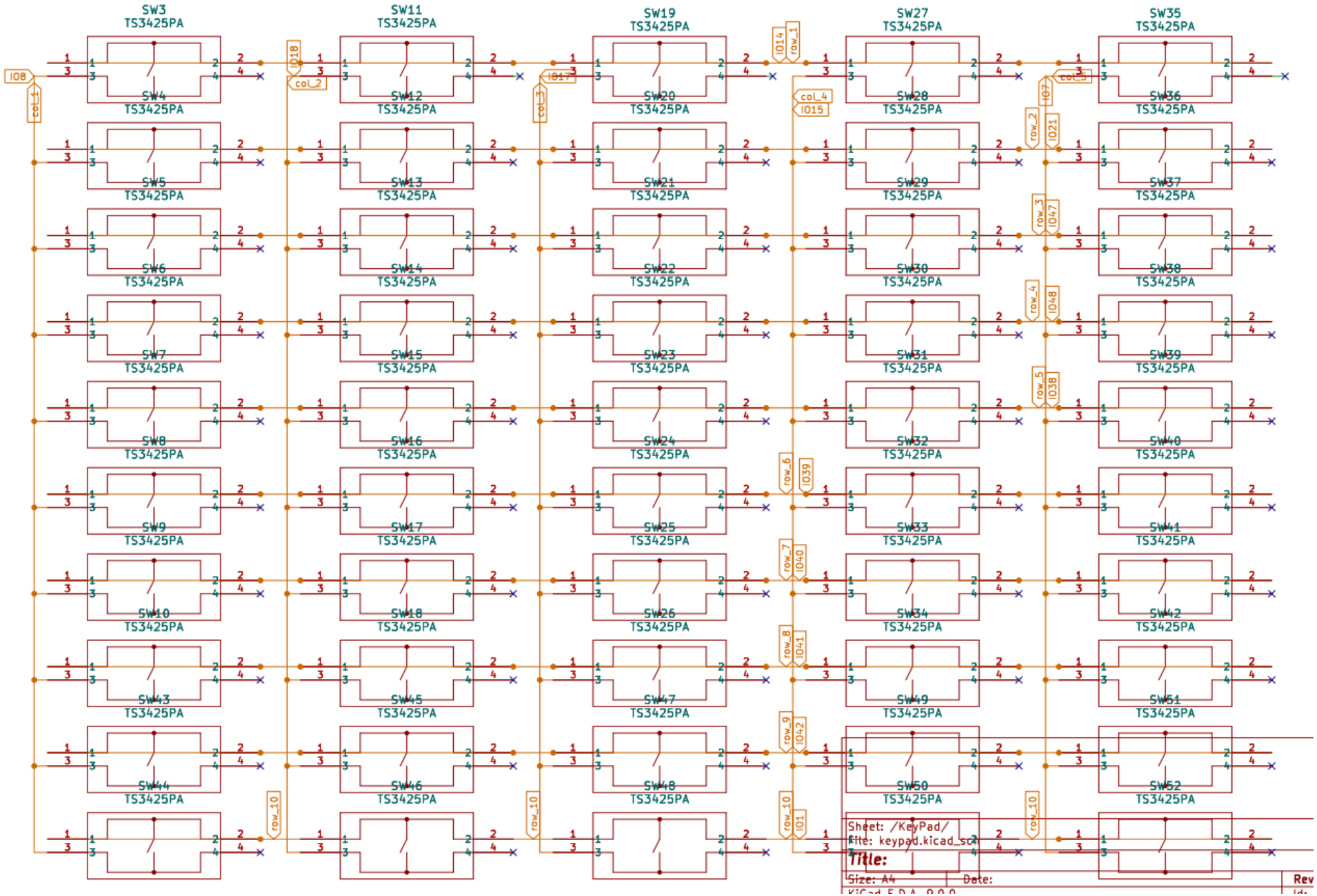
MCU


VDD33BB
R8
10K(5%)
GND
C7
0.1uF/50V(10%)
SW1
0.1uF/50V(10%)
C5
C6
0.1uF/50V(10%)
SW2
C8
22Uf/10v(20%)
CH_4
C9
0.1uF/50V(10%)
ESP32-S3-WROOM-1-N8R8
EN
3V3
GND
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
IO8
IO9
IO10
IO11
IO12
IO13
IO14
IO15
IO16
TXD0
RXD0
IO17
IO18
USB_D-
USB_D+
IO21
IO35
IO36
IO37
IO38
IO39
IO40
IO41
IO42
IO45
IO46
IO47
IO48
PSRAM
TX
RX
BMS
EXT_5V
VDD33BB
BAT_M
CHG_SB
GND
104
106
File: BMS.kicad_sch
usb
DATA_N
DATA_P
File: usb.kicad_sch

The capacitors in this circuit are primarily for **power stabilization and signal conditioning**. The main power rail ($\mathrm{VDD33BB}$) stabilization is handled by a combination of the $22\mu\mathrm{F}$ **capacitor (** $\mathrm{C8}$**)**, which provides **bulk decoupling** to supply instantaneous current demands, and the $0.1\mu\mathrm{F}$ **capacitor (**$\mathrm{C9}$**)**, which acts as a **high-frequency bypass filter** to suppress noise close to the $\mathrm{ESP32\text{-}S3}$ chip. Additionally, the $0.1\mu\mathrm{F}$ capacitors $\mathrm{C5}$ **and** $\mathrm{C6}$ are critical for **switch debouncing**. When paired with a resistor (like $\mathrm{R8}$ in the EN circuit), they form an RC network that filters the mechanical noise (bouncing) from the push-buttons ($\mathrm{SW1}$ on the EN pin and $\mathrm{SW2}$ on $\mathrm{IO9}$), ensuring a single, clean transition for reliable reset and digital input signals.

KEYPAD AND EXTENDED GPIO





LAYOUT AND PHYSICAL BOARD