ES8374

Low Power Mono Audio CODEC

FEATURES

System

- High performance and low power multi-bit delta-sigma audio ADC and DAC
- I^2S/PCM master or slave serial data port
- Two pairs of analog input with differential input option
- Mono analog output
- 256/384Fs, USB 12/24 MHz, fractional PLL for wide range of system clocks
- Standard audio clock output
- Sophisticated analog input and output routing, mixing and gain
- GPIO
- I^2C interface

ADC

- 24-bit, 8 to 96 kHz sampling frequency
- 95 dB signal to noise ratio, -85 dB THD+N
- Low noise pre-amplifier
- Noise reduction filters
- Auto level control (ALC) and noise gate
- Support analog and digital microphone
- Microphone bias

DAC

- 24-bit, 8 to 96 kHz sampling frequency
- 95 dB signal to noise ratio, -85 dB THD+N
- 1.25W@8Ω/5V or 1.8W@4Ω/4.2V mono class D speaker driver
- Dynamic range compression
- Headphone and external mic detection
- Pop and click noise suppression

Low Power

- 3.3V to 5V operation
- 32 mW playback; 42 mW playback and record
- Low standby current

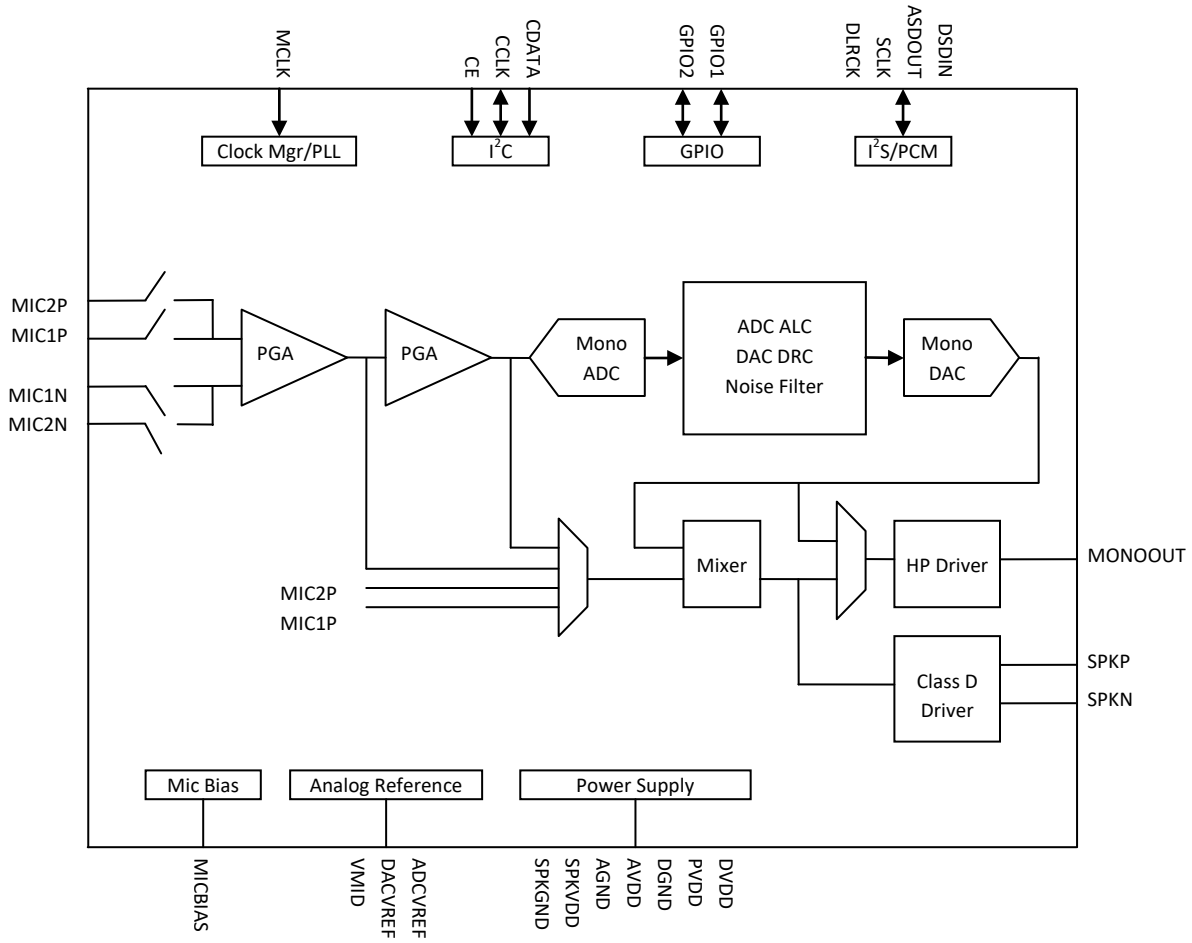
APPLICATIONS

- Car DV
- IP Camera
- DVR, NVR
- Surveillance

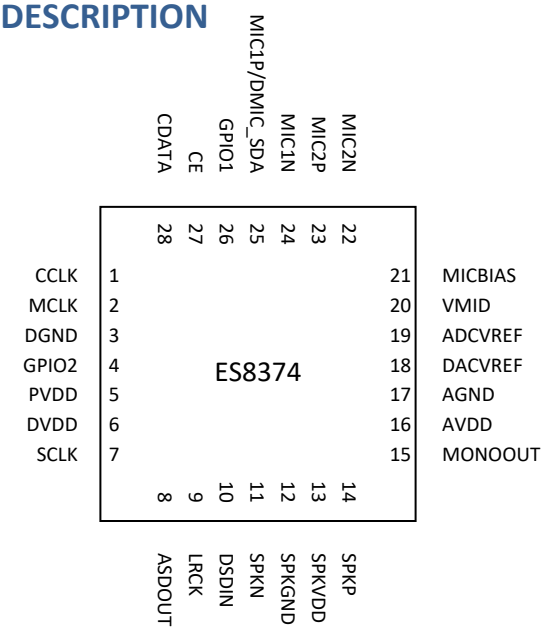
ORDERING INFORMATION

ES8374 -40°C ~ +85°C
QFN-28

1. BLOCK DIAGRAM

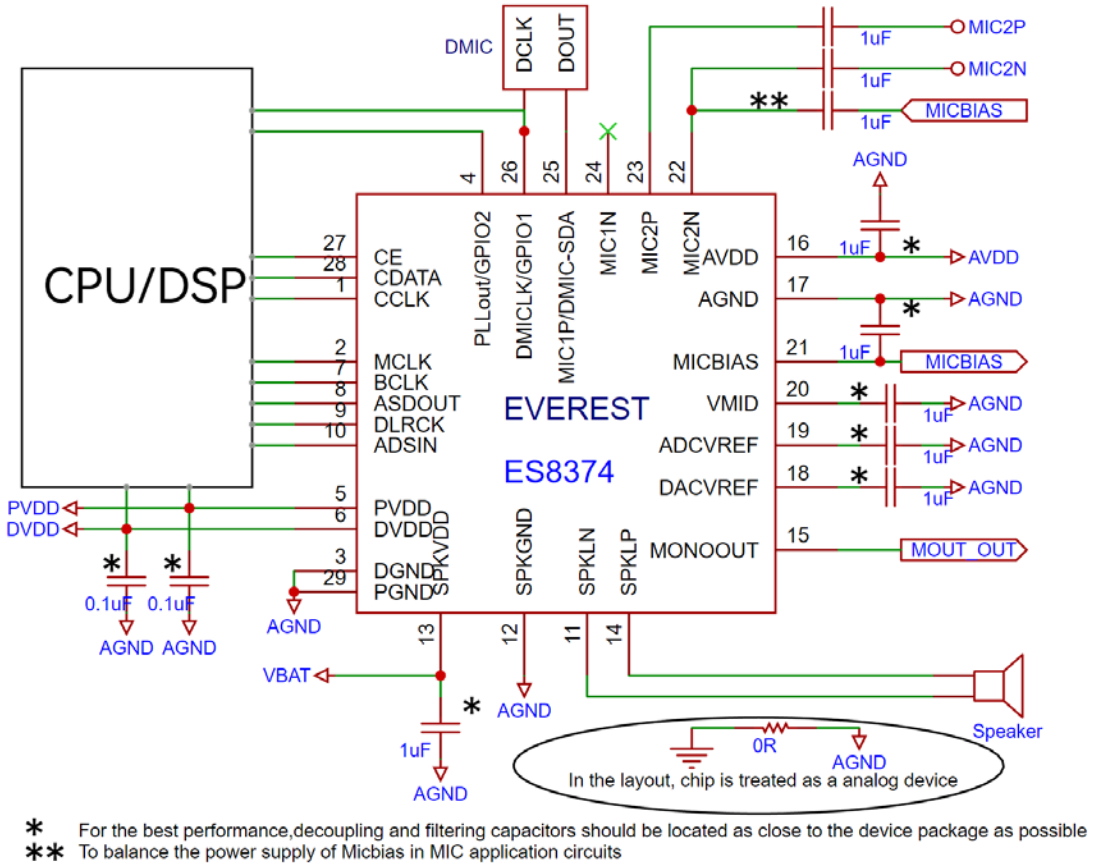


2. PIN OUT AND DESCRIPTION



NAME	I/O	DESCRIPTION
MCLK	DI	Master clock
CDATA	DIO	I^2C data
CCLK	DI	I^2C clock
CE	DI	I^2C address
GPIO1	DIO	GPIO (digital mic clock, jack detect, PLL out, interrupt)
GPIO2	DIO	GPIO (PLL out, interrupt)
ASDOUT	DO	I^2S/PCM serial data out
DSDIN	DI	I^2S/PCM serial data in
LRCK	DIO	I^2S/PCM left and right clock
SCLK	DIO	I^2S/PCM bit clock
MIC1P/DMIC_SDA	AI	P analog input or digital mic data
MIC1N	AI	N analog input
MIC2P	AI	P analog input
MIC2N	AI	N analog input
MONOOUT	AO	Mono output
SPKP	AO	Positive speaker out
SPKN	AO	Negative speaker out
MICBIAS		Mic bias
ADCVRP		ADC reference filtering
DACVRP		DAC reference filtering
VMID		Common mode filtering
DVDD		Digital core power supply
PVDD		Digital IO power supply
DGND		Digital ground
AVDD		Analog power supply
AGND		Analog ground
SPKVDD		Speaker driver power supply
SPKGND		Speaker driver ground

3. TYPICAL APPLICATION CIRCUIT



* For the best performance,decoupling and filtering capacitors should be located as close to the device package as possible
** To balance the power supply of Micbias in MIC application circuits

4. CLOCK MODES AND SAMPLING FREQUENCIES

The device supports three types of clocking: standard audio clocks (256Fs, 384Fs, 512Fs, etc), USB clocks (12/24 MHz), and an on-chip 22-bit fractional PLL clock (minimal PLL input is 2 MHz).

According to the serial audio data sampling frequency (Fs), the device can work in two speed modes: single speed mode or double speed mode. In single speed mode, Fs normally ranges from 8 kHz to 48 kHz, and in double speed mode, Fs normally range from 64 kHz to 96 kHz.

The device can work either in master clock mode or slave clock mode. In slave mode, LRCK and SCLK are supplied externally, and LRCK and SCLK must be synchronously derived from the system clock with specific rates. In master mode, LRCK and SCLK are derived internally from device master clock.

5. MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard I^2C micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

I²C interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 1. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 400 kbps.

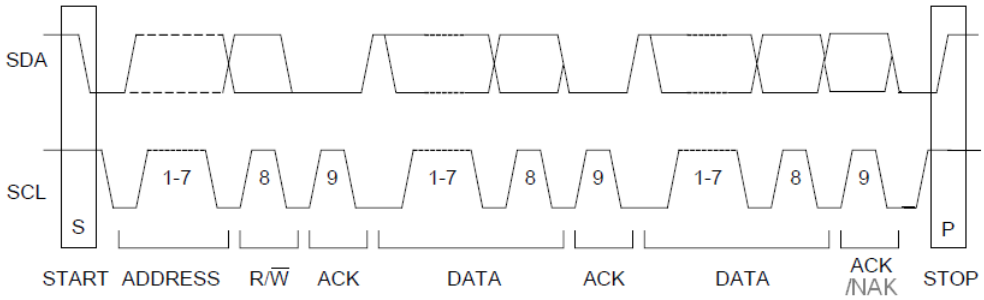


Figure 1 Data Transfer for I²C Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0. The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In I²C interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 1 and Table 2. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register.

Table 1 Write Data to Register in I²C Interface Mode

Chip Address		R/W		Register Address		Data to be written
001000	AD0	0	ACK	RAM	ACK	DATA

Table 2 Read Data from Register in I²C Interface Mode

Chip Address		R/W		Register Address
001000	AD0	0	ACK	RAM
Chip Address		R/W		Data to be read
001000	AD0	1	ACK	Data

6. DIGITAL AUDIO INTERFACE

The device provides many formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, BCLK (SCLK) and DACDAT/ADCDAT pins. These formats are I^2S, left justified, right justified, DSP/PCM and TDM mode. DAC input DACDAT is sampled by the device on the rising edge of SCLK. ADC data is out at ADCDAT on the falling edge of SCLK. The relationship of SDATA (DACDAT/ADCDAT), SCLK and LRCK with these formats are shown through Figure 2 to Figure 6.

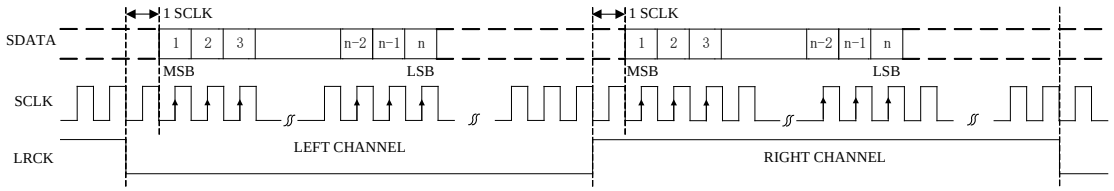


Figure 2 I^2S Serial Audio Data Format Up To 24-bit

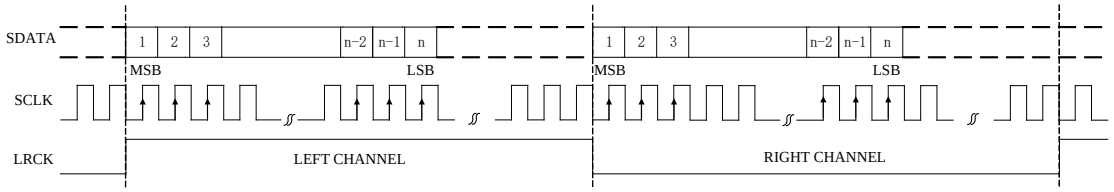


Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

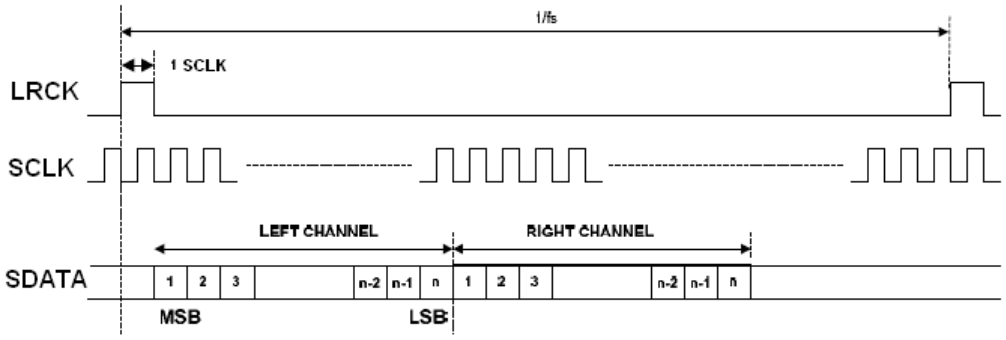


Figure 4 DSP/PCM Mode A

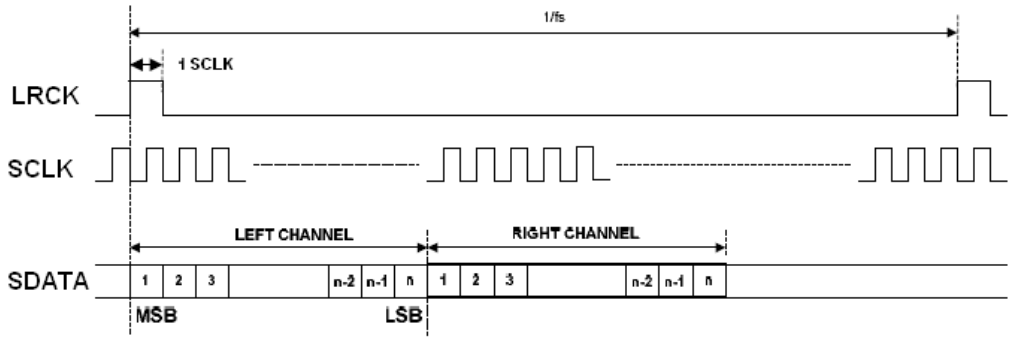


Figure 5 DSP/PCM Mode B

7. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Continuous operation at or beyond these conditions may permanently damage the device.

PARAMETER	MIN	MAX
Analog Supply Voltage Level	-0.3V	+5.5V
Digital Supply Voltage Level	-0.3V	+5.5V
Analog Input Voltage Range	AGND-0.3V	AVDD+0.3V
Digital Input Voltage Range	DGND-0.3V	PVDD+0.3V
Operating Temperature Range	-40°C	+85°C
Storage Temperature	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
AVDD	3	3.3/5	5.5	V
SPKVDD (Note 1, 2) 4Ω Speaker 8Ω Speaker	 3 3	 3.3/4.2 3.3/5	 5 5.5	V
DVDD	3	3.3/5	5.5	V
PVDD (DVDD - input high level < 2V)	1.6	1.8/3.3/5	5.5	V

Note 1: package thermal pad must be connected to ground as much as possible to provide class D speaker driver heat dissipation.

Note 2: when standby class D speaker driver, with all power supply on, entering low power through control register setting, then stopping MCLK.

ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz or 96 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
ADC Performance				
Signal to Noise ratio (A-weigh)	85	95	98	dB
THD+N	-88	-85	-75	dB
Gain Error			±5	%
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	50			dB
Filter Frequency Response – Double Speed				
Passband	0		0.2268	Fs
Stopband	0.4535			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	50			dB
Analog Input				
Full Scale Input (differential P and N)		AVDD/3.3		Vrms
Input Impedance		10		KΩ

DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify: AVDD=3.3V, DVDD=3.3V, AGND=0V, DGND=0V, Ambient temperature=25°C, Fs=48 KHz or 96 KHz, MCLK/LRCK=256.

PARAMETER	MIN	TYP	MAX	UNIT
DAC Performance				
Signal to Noise ratio (A-weigh)	83	95	98	dB
THD+N	-88	-85	-75	dB
Filter Frequency Response – Single Speed				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	53			dB
Filter Frequency Response – Double Speed				
Passband	0		0.4167	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	56			dB
Analog Output				
Full Scale Output Level		AVDD/3.3		Vrms

DC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT
Normal Operation Mode				
DVDD=3.3V, PVDD=3.3V, AVDD=3.3V: Play back Play back and record		 32 42		mW
Power Down Mode				
DVDD=3.3V, PVDD=3.3V, AVDD=3.3V		50		uA
Digital Voltage Level				
Input High-level Voltage	0.7*PVDD			V
Input Low-level Voltage			0.5	V
Output High-level Voltage		PVDD		V
Output Low-level Voltage		0		V

SERIAL AUDIO PORT SWITCHING SPECIFICATIONS

PARAMETER	Symbol	MIN	MAX	UNIT
MCLK frequency			51.2	MHz
MCLK duty cycle		40	60	%
LRCK frequency			200	KHz
LRCK duty cycle		40	60	%
SCLK frequency			26	MHz
SCLK pulse width low	TSCLKL	15		ns
SCLK Pulse width high	TSCLKH	15		ns
SCLK falling to LRCK edge	TSLR	–10	10	ns
SCLK falling to SDOUT valid	TSDO	0		ns
SDIN valid to SCLK rising setup time	TSDIS	10		ns
SCLK rising to SDIN hold time	TSDIH	10		ns

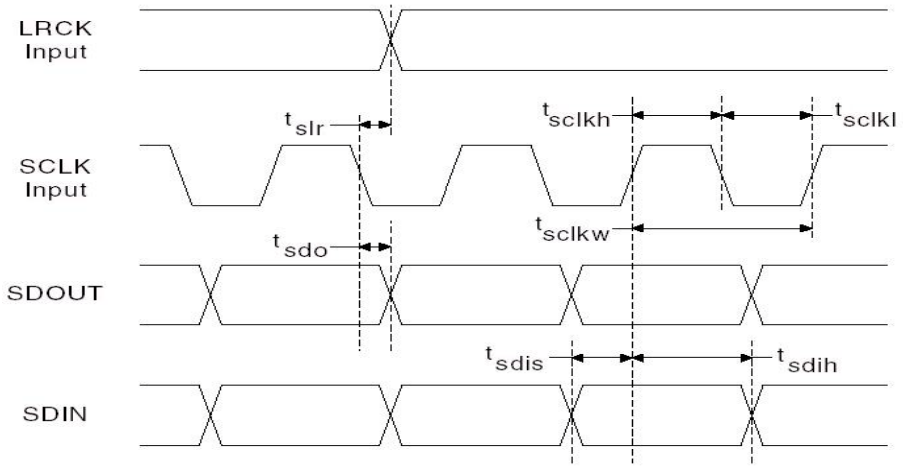


Figure 6 Serial Audio Port Timing

I²C SWITCHING SPECIFICATIONS (SLOW SPEED MODE/HIGH SPEED MODE)

PARAMETER	Symbol	MIN	MAX	UNIT
CCLK Clock Frequency	F_{CCLK}		100/400	KHz
Bus Free Time Between Transmissions	T_{TWID}	4.7/1.3		us
Start Condition Hold Time	T_{TWSTH}	4.0/0.6		us
Clock Low time	T_{TWCL}	4.7/1.3		us
Clock High Time	T_{TWCH}	4.0/0.6		us
Setup Time for Repeated Start Condition	T_{TWSTS}	4.7/0.6		us
CDATA Hold Time from CCLK Falling	T_{TWDH}		3.45/0.9	us
CDATA Setup time to CCLK Rising	T_{TWDS}	0.25/0.1		us
Rise Time of CCLK	T_{TWR}		1.0/0.3	us
Fall Time CCLK	T_{TWF}		1.0/0.3	us

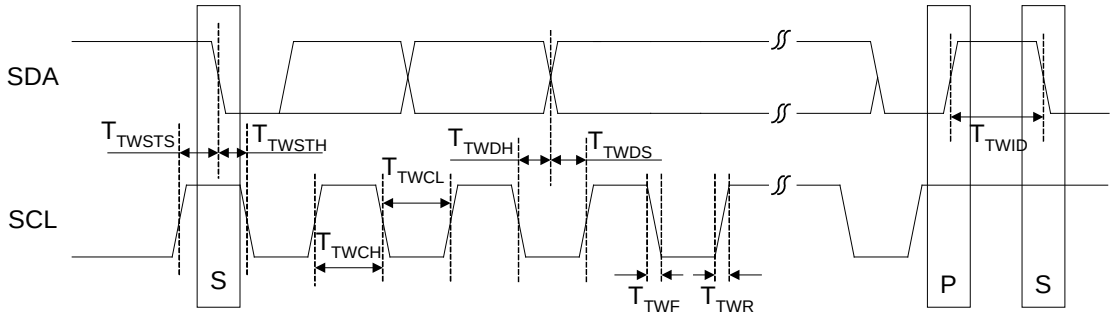


Figure 7 I²C Timing

8. CONFIGURATION REGISTER DEFINITION

REGISTER 0X00 –RESET, DEFAULT 0000 0011

Bit Name	Bit	Description
CSM_ON	7	Chip current state machine control 0 – csm power down(default) 1 – csm power on
SEQ_DIS	6	Power up sequence control 0 – power up sequence enable(default) 1 – power up sequence disabled
RST_DIG	5	Digital reset 0 – normal(default) 1 – reset digital except control port block
RST_REGS	4	registers reset 0 – normal(default) 1 – reset all registers to default value except “rst_regs”
RST_CLKMGR	3	clock manager block reset 0 – normal(default) 1 – reset clock manager block
RST_MASTER	2	master block reset 0 – normal(default) 1 – reset master block
RST_ADC_DIG	1	ADC digital block reset 0 – normal 1 – reset ADC digital block (default)
RST_DAC_DIG	0	DAC digital block reset 0 – normal 1 – reset DAC digital block (default)

REGISTER 0X01 – CLOCK MANAGER, DEFAULT 0000 0011

Bit Name	Bit	Description
MCLK_DIV2	7	MCLK divide by 2 control 0 – normal (default) 1 – MCLK divide by 2
MCLK_ON	6	MCLK in control 0 – MCLK off(default) 1 – MCLK on
BCLK_ON	5	SDP bit clock control 0 – BCLK off(default) 1 – BCLK on
CLKD_ON	4	Class D clock control 0 – clk_spk off (default) 1 – clk_spk on
CLK_ADC_ON	3	ADC digital clock control 0 – adc_mclk off(default) 1 – adc_mclk on
CLK_DAC_ON	2	DAC digital clock control 0 – dac_mclk off(default) 1 – dac_mclk on
ANACLK_ADC_ON	1	ADC analog clock control

		0 – anaclk_adc off 1 – anaclk_adc on(default)
ANACLK_DAC_ON	0	DAC analog clock control 0 – anaclk dac off 1 – anaclk_dac on(default)

REGISTER 0X02 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
CLK_ADC_CONT	6	ANA_CLK_ADC control 0: CLK_ADC flex (default) 1: CLK_ADC continue
CLK_ADC_DOUBLE	5	clk_adc divide by 2 control 0 – normal(default) 1 – clk_adc divide by 2
CLK_DAC_DOUBLE	4	clk_dac divide by 2 control 0 – normal(default) 1 – clk_dac divide by 2
PLL_SEL	3	PLL selection 0 – PLL disable (default) 1 – PLL enable (minimal PLL input is 2 MHz)
SYNCMODE	0	sync mode 0 – normal(default) 1 – sync mode

REGISTER 0X03 – CLOCK MANAGER, DEFAULT 0010 0000

Bit Name	Bit	Description
ADC_OSR	5:0	ADC delta sigma over sample rate when SS: ADC_OSR <=f(adc_mclk) / fs / 8 when DS: ADC_OSR<=f(adc_mclk) /fs /4 f(adc_mclk) refer to CLK_ADC_DIV and CLK_ADC_DOUBLE when clk_adc_double=0: f(adc_mclk) = f(MCLK) /CLK_ADC_DIV when clk_adc_double=1: f(adc_mclk) = f(MCLK) /CLK_ADC_DIV/2

REGISTER 0X04 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
FLTCNT_EX	5:0	DAC filter counter waiting cycles control 6'h3F: -1 0~6'h3E: 0~6'h3E FLTCNT_EX >= (f(dac_mclk)/fs) % 256 (when SS)，FLTCNT_EX >= (f(dac_mclk)/fs) % 128 (when DS) f(dac_mclk) refer to CLK_DAC_DIV and CLK_DAC_DOUBLE when clk_dac_double=0: f(dac_mclk) = f(MCLK) /CLK_DAC_DIV when clk_dac_double=1: f(dac_mclk) = f(MCLK) /CLK_DAC_DIV/2

REGISTER 0X05 – CLOCK MANAGER, DEFAULT 0001 0001

Bit Name	Bit	Description
CLK_ADC_DIV	7:4	adc_mclk=MCLK/CLK_ADC_DIV
CLK_DAC_DIV	3:0	dac_mclk=MCLK/CLK_DAC_DIV

REGISTER 0X06 – CLOCK MANAGER, DEFAULT 0000 0001

Bit Name	Bit	Description

DACLRCK_DIV[11:8]	3:0	Internal daclrck divider bit 11 to bit 8 LRCK=MCLK/DACLRCK_DIV

REGISTER 0X07 – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
DACLRCK_DIV[7:0]	7:0	Internal daclrck divider bit 7 to bit 0 LRCK=MCLK/DACLRCK_DIV

REGISTER 0X08 – CLOCK MANAGER, DEFAULT 0010 0000

Bit Name	Bit	Description
DIV_CLKD	5:0	class D speaker clock divider 0 – divide by 32 (default) 61 – divide by 64 62 – divide by 96 63 – divide by 127 other – divide by DIV_CLKD

REGISTER 0X09 – CLOCK MANAGER, DEFAULT 1000 0000

Bit Name	Bit	Description
PLL_PDN	7	power down PLL analog block 0 – enable PLL analog 1 – power down PLL analog
PLL_RB	6	reset PLL digital block 0 – reset PLL digital 1 – PLL digital on
PLLDITH_MAG	4:2	PLL DSM divider dither 0 – dither off 1 – minimum dither … 7 – maximum dither
PLLOUT_SEL	1:0	PLL output select 0 – PLL clock in (PLL bypass) 1 – vcoout divide by 8 2 – vcoout divide by 4 3 – vcoout divide by 2

REGISTER 0X0A – CLOCK MANAGER, DEFAULT 0100 1010

Bit Name	Bit	Description
PLL_LP	7	PLL analog low power mode 0 – normal 1 – PLL low power mode
PLL_CP	6:4	PLL cp gain setting 000 – cp gain0 001 – cp gain1 010 – cp gain2 011 – cp gain3 100 – cp gain4 101 – cp gain5 110 – cp gain6 111 – cp gain7

PLL_SUPSEL	3:2	00 for vddd=1.8v 01 for vddd=2.5v 1x for vddd=3.3v
PLL_KVCO	1:0	Vco gain setting 00 – vco gain0 01 – vco gain1 10 – vco gain2 11 – vco gain3

REGISTER 0X0B – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
PLL_CAL_SHORT	7	0 – PLL calibration 64 data 1 – PLL calibration 32 data
PLL_VCO_WAIT	6:5	0 – wait 2 MCLK for vcoout stable when calibration 1 – wait 4 MCLK for vcoout stable when calibration 2 – wait 8 MCLK for vcoout stable when calibration 3 – wait 16 MCLK for vcoout stable when calibration
PLL_N	3:0	Integer part of PLL input/output frequency ratio; Use value greater than 5 and less than 13

REGISTER 0X0C – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
PLL_K[21:16]	5:0	Fractional part of PLL input/output frequency ratio (treat as one 22-digital binary number) fraction= PLL_K/0.65735982222960 F(vcoout)=F(PLLOUT)*8 (8or 4, 2, through PLLOUT_SEL) R=F(vcoout) / F(MCLK) PLL_N=int(R) PLL_K=int(2^22*(R-R(int))* 0.65735982222960)

for example: F(MCLK)=12MHz, F(PLLOUT)=12.288MHz:
F(vcoout) = 12.288MHz * 8 = 98.304MHz.
R = F(vcoout) / F(CLK_IN) = 98.304 / 12.0 = 8.192
PLL_N = int(R) = 8
PLL_K = int(2^22 * (8.192-8) * 0.65735982222960) = 529376 = 0x813E0

REGISTER 0X0D – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
PLL_K[15:8]	7:0	Fractional part of PLL input/output frequency ratio (treat as one 22-digital binary number)

REGISTER 0X0E – CLOCK MANAGER, DEFAULT 0000 0000

Bit Name	Bit	Description
PLL_K[7:0]	7:0	Fractional part of PLL input/output frequency ratio (treat as one 22-digital binary number)

REGISTER 0X0F – SDP, DEFAULT 0000 0001

Bit Name	Bit	Description
MSC	7	0 – slave serial port mode (default) 1 – master serial port mode
TRI	6	Tri-state output 0 – normal

		1 – ADCDAT, LRCK, BCLK tri-state output
BCLK_INV	5	0 – normal (default) 1 – BCLK inverted
BCLKDIV	4:0	0 – no master BCLK 1~18 – MCLK/BCLKDIV 19 – MCLK/20 20 – MCLK/22 21 – MCLK/24 22 – MCLK/25 23 – MCLK/30 24 – MCLK/32 25 – MCLK/33 26 – MCLK/34 27 – MCLK/36 28 – MCLK/44 29 – MCLK/48 30 – MCLK/66 31 – MCLK/72

REGISTER 0X10 – SDP, DEFAULT 0000 0000

Bit Name	Bit	Description
ADC_SDP_MUTE	7:6	ADC SDP MUTE 00: ADC SDP unmute(default) 01: ADC SDP mute R 10: ADC SDP mute L 11: ADC SDP mute L+R
ADCLRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity 1 – left and right inverted polarity DSP/PCM mode: 0 – MSB is available on 2nd BCLK rising edge after ALRCK rising edge 1 – MSB is available on 1st BCLK rising edge after ALRCK rising edge
ADCWL	4:2	000 – 24-bit serial audio data word length(default) 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
ADCFORMAT	1:0	00 – I2S serial audio data format(default) 01 – left justify serial audio data format 10 – reserve 11 – DSP/PCM mode serial audio data format

REGISTER 0X11 – SDP, DEFAULT 0000 0000

Bit Name	Bit	Description
DAC_SDP_MUTE	6	DAC SDP mute control 0 – DAC SDP unmute(default) 1 – DAC SDP mute
DACLRP	5	I2S, left justified or right justified mode: 0 – left and right normal polarity 1 – left and right inverted polarity DSP/PCM mode:

		0 – MSB is available on 2nd BCLK rising edge after DLRCK rising edge 1 – MSB is available on 1st BCLK rising edge after DLRCK rising edge
DACWL	4:2	000 – 24-bit serial audio data word length(default) 001 – 20-bit serial audio data word length 010 – 18-bit serial audio data word length 011 – 16-bit serial audio data word length 100 – 32-bit serial audio data word length
DACFORMAT	1:0	00 – I2S serial audio data format(default) 01 – left justify serial audio data format 10 – reserve 11 – DSP/PCM mode serial audio data format

REGISTER 0X12 –SYSTEM, DEFAULT 0100 0000

Bit Name	Bit	Description
CHIPINI_CON	7:0	ChipIni state period control period=CHIPINI_CON*16/LRCK

REGISTER 0X13 –SYSTEM, DEFAULT 0100 0000

Bit Name	Bit	Description
POWERUP_CON	7:0	PowerUp state period control period=POWERUP_CON*16/LRCK

REGISTER 0X14 –ANALOG REFERENCE, DEFAULT 1001 1100

Bit Name	Bit	Description
LPVREFBUF	7	0 – normal mode of internal reference voltage 1 – low power mode of internal reference voltage
VREF_LO	6	VREF control
RST_A	5	Reset ADC
PDN_MIC	4	Power down internal mic bias reference 0 – enable mic bias 1 –power down mic bias
VROI_LN	3	Select impedance internal reference voltage 0 – normal impedance 1 – low impedance
PDN_VREFBUF	2	Power down internal reference voltage 0 – enable reference 1 – power down reference
VMIDSEL	1:0	00 – vmid off 01 – xx 10 – normal vmid operation 11 – start up vmid speed charge

REGISTER 0X15 –ANALOG POWER DOWN, DEFAULT 10111110

Bit Name	Bit	Description
PDN_ANA	7	0 – enable analog circuits 1 – power down analog circuits
ENREFR	6	0 – disable internal reference circuits 1 – enable reference circuits
PDN_DACL	5	0 – enable analog DAC circuits 1 – power down analog DAC circuits

PDN_IBIASGEN	4	0 – enable analog bias circuits 1 – power down analog bias circuits
PDN_ADCBIASGEN	3	0 – enable analog ADC bias circuits 1 – power down analog ADC bias circuits
PDN_ADCVERFGEN	2	0 – enable analog ADC reference circuits 1 – power down analog ADC reference circuits
PDN_DACVREFGEN	1	0 – enable analog DAC reference circuits 1 – power down analog DAC reference circuits

REGISTER 0X16 –ANALOG LOW POWER MODE, DEFAULT 00000000

Bit Name	Bit	Description
LPMCDF	6	0 – normal mode 1 – low power mode for input diff
LPPGA	5	0 – normal mode 1 – low power mode for PGA
LPVCMMOD	4	0 – normal mode 1 – low power mode for ADC
LPADCVRP	3	0 – normal mode 1 – low power mode for ADC
LPDACVRP	2	0 – normal mode 1 – low power mode for DAC
LPFLASH	1	0 – normal mode 1 – low power mode for ADC
LPINT1	0	0 – normal mode 1 – low power mode for ADC

REGISTER 0X17 –REFERENCE AND POWER MODE, DEFAULT 10000000

Bit Name	Bit	Description
VX1SEL	7	0 – vx1=1.45v 1 – vx1=1.65v
VX2OFF	6	0 – enable internal reference voltage doubler 1 – disable internal reference voltage doubler
DAC_IBIAS_SW	5	0 – normal DAC bias setting 1 – higher DAC bias setting
VMIDLOW	4:3	00- vmid='vdda/2' 01- vmid='vdda/2-50mv' 10- vmid='vdda/2-100mv' 11- vmid='vdda/2-150mv'
LPDACL	1	0 – normal mode 1 – low power mode for DAC
LPLOUT1	0	0 – normal mode 1 – low power mode for mono output

REGISTER 0X18 –BIAS SELECTION, DEFAULT 11111100

Bit Name	Bit	Description
VSEL	7:0	Select bias Bit2 1 0 001 -2.5u 010 -5u 011 -7.5u

		100 -10u 101 -12.5u 110 -15u 111 -17.5u Bit7—bias for input diff, 0=10u 1=bit[2:0] bias setting Bit6—bias for momo output, 0=10u 1=bit[2:0] bias setting Bit5—bias for miserSPK, 0=10u 1=bit[2:0] bias setting Bit4—bias for DAC, 0=10u 1=bit[2:0] bias setting Bit3—bias for ADC, 0=10u 1=bit[2:0] bias setting

REGISTER 0X1A –MONO OUT SELECTION, DEFAULT 00011000

Bit Name	Bit	Description
LD2LOUT	7	0 – disable 1 – select DAC to mono output
LLN2LOUT	6	0 – disable 1 – select mixer output to mono output
ENLOUT1	5	0 – disable 1 – enable mono output
LINE1_REF2	4	0 – normal mono output bias 1 – low level mono output bias
LOUT_MUTE	3	0 – normal mono output level 1 –mute mono output level
LMIXSEL	2:0	Select analog input to mixer input
		000 – MIC1P 001 – MIC2P 010 – diff out1 011 – diff out2 100 – PGA out1 111 – PGA out2

REGISTER 0X1B –MONO OUT GAIN, DEFAULT 00000000

Bit Name	Bit	Description
LOUT_HI	7	1 – mono output level high
LOUT_LO1	6	1 – mono output low level1
LOUT_LO0	5	1 – mono output low level0
LINE1_REF1	4	0 – normal mono output bias 1 – high driving level mono output bias
LOUT_VOL	3:0	Gain setting for mono output
		Bit 765 3210: gain when LD2LOUT=1/gain when LLN2LOUT=1 000 0000：-8dB/-9.5dB 000 0001：-6.5dB/-8dB 000 0010：-5dB/-6.5dB 000 0011：-3.5dB/-5dB 000 0100：-2dB/-3.5dB 000 1000：-0.5dB/-2dB 000 1001：+1dB/-0.5dB 000 1010：+2.5dB/+1dB 000 1011：+4dB/+2.5dB

		001 0000：-21.5dB/-23dB 001 0001：-20dB/-21.5dB 001 0010：-18.5dB/-20dB 001 0011：-17dB/-18.5dB 001 0100：-15.5dB/-17dB 001 1000：-14dB/-15.5dB 001 1001：-12.5dB/-14dB 001 1010：-11dB/-12.5dB 001 1011：-9.5dB/-11dB 010 0000：-8dB/-21.5dB 010 0001：-6.5dB/-20dB 010 0010：-5dB/-18.5dB 010 0011：-3.5dB/-17dB 010 0100：-2dB/-15.5dB 010 1000：-0.5dB/-14dB 010 1001：+1dB/-12.5dB 010 1010：+2.5dB/-11dB 010 1011：+4dB/-9.5dB 011 0000：-21.5dB/-35dB 011 0001：-20dB/-33.5dB 011 0010：-18.5dB/-32dB 011 0011：-17dB/-30.5dB 011 0100：-15.5dB/-29dB 011 1000：-14dB/-27.5dB 011 1001：-12.5dB/-26dB 011 1010：-11dB/-24.5dB 011 1011：-9.5dB/-23dB 100 0000：-8dB/-3.5dB 100 0001：-6.5dB/-2dB 100 0010：-5dB/-0.5dB 100 0011：-3.5dB/+1dB 100 0100：-2dB/+2.5dB 100 1000：-0.5dB/+4dB 100 1001：+1dB/+5.5dB 100 1010：+2.5dB/+7dB 100 1011：+4dB/+8.5dB

REGISTER 0X1C –MIXER, DEFAULT 00010000

Bit Name	Bit	Description
LD2LSPKMX	7	0 – disable 1 – select DAC to mixer
LAX2LSPKMX	6	0 – disable 1 – select aux to mixer
LPSPKMX	5	0 – normal 1 – low power for mixer
SPKMIX_REF2	4	0 – normal mixer bias 1 – low power level mixer bias

SPKMIX_REF1	3	0 – normal mixer bias 1 – high driving level mixer bias

REGISTER 0X1D –MIXER GAIN, DEFAULT 00010000

Bit Name	Bit	Description
LSPKMX_HI	7	1 – mixer output level high
LSPKMX_LO1	6	1 – mixer output low level1
LSPKMX_LO0	5	1 – mixer output low level0
LSPKMX_MUTE	4	0 – normal mixer output level 1 –mute mixer output level
LSPKMXVOL	3:0	Gain setting for mixer output
		Bit 765 3210: gain when LD2LSPKMX=1/gain when LAX2LSPKMX=1 000 0000：-8dB/-9.5dB 000 0001：-6.5dB/-8dB 000 0010：-5dB/-6.5dB 000 0011：-3.5dB/-5dB 000 0100：-2dB/-3.5dB 000 1000：-0.5dB/-2dB 000 1001：+1dB/-0.5dB 000 1010：+2.5dB/+1dB 000 1011：+4dB/+2.5dB 001 0000：-21.5dB/-23dB 001 0001：-20dB/-21.5dB 001 0010：-18.5dB/-20dB 001 0011：-17dB/-18.5dB 001 0100：-15.5dB/-17dB 001 1000：-14dB/-15.5dB 001 1001：-12.5dB/-14dB 001 1010：-11dB/-12.5dB 001 1011：-9.5dB/-11dB 010 0000：-8dB/-21.5dB 010 0001：-6.5dB/-20dB 010 0010：-5dB/-18.5dB 010 0011：-3.5dB/-17dB 010 0100：-2dB/-15.5dB 010 1000：-0.5dB/-14dB 010 1001：+1dB/-12.5dB 010 1010：+2.5dB/-11dB 010 1011：+4dB/-9.5dB 011 0000：-21.5dB/-35dB 011 0001：-20dB/-33.5dB 011 0010：-18.5dB/-32dB 011 0011：-17dB/-30.5dB 011 0100：-15.5dB/-29dB 011 1000：-14dB/-27.5dB 011 1001：-12.5dB/-26dB

		011 1010：-11dB/-24.5dB 011 1011：-9.5dB/-23dB 100 0000：-8dB/-3.5dB 100 0001：-6.5dB/-2dB 100 0010：-5dB/-0.5dB 100 0011：-3.5dB/+1dB 100 0100：-2dB/+2.5dB 100 1000：-0.5dB/+4dB 100 1001：+1dB/+5.5dB 100 1010：+2.5dB/+7dB 100 1011：+4dB/+8.5dB

REGISTER 0X1E – SPEAKER, DEFAULT 00000000

Bit Name	Bit	Description	
EN_SPKL	7	1 – enable classD speaker output	
PDN_SPKLBIASGEN	6	0 – enable speaker bias 1 – power down speaker bias	
LM2SPKLOUT	5	0 – disable input to speaker output 1 – select mixer output to speaker output	
LSPKVOL	2:0	SPK volume	
		000 – 0dB 001 – 1.5dB 010 – 3dB 011 – 4dB	100 – 5dB 101 – 6dB 110 – 6.75dB 111 – 7.5dB

REGISTER 0X1F –SPEAKER, DEFAULT 00001000

Bit Name	Bit	Description
SPK_TRI_TSEL0	7	SPK internal PWM FREQ selection
SPK_TRI_TSEL1	6	SPK internal PWM FREQ selection
		TSEL1 TSEL0 00-384KHZ 01-352KHZ 10-341KHZ 11-256KHZ
SPK_TRI_TSEL2	5	SPK internal PWM TRIM selection
SPK_TRI_TSEL3	4	SPK internal PWM TRIM selection
EN_OTP	3	1 – enable over temperature protection
EN_SPKLSCP	2	SPKL short circuit protection 0-disable 1-enable
SPK_LPBUF	1	0 – normal mode 1 – low power mode for speaker D internal reference
SPKL_DT	0	SPKL dead time selection 0-normal 1-add delay

REGISTER 0X20 –SPEAKER, DEFAULT 00001000

Bit Name	Bit	Description

EN_OC	3	Over current control 0 –system OC/OTP protection disable 1 –system OC/OTP protection enable
SPKL_ILOSEL1	2	SPKL short circuit current detection selection 0-normal 1 -lower current
SPKL_ILOSEL0	1	SPKL short circuit current detection selection 0-normal 1 -lower current
OTP_SEL	0	Over temperature protection 0 – protection level0 0 – protection level1

REGISTER 0X21 –PGA, DEFAULT 11010100

Bit Name	Bit	Description
PDN_ALINL	7	0 – enable analog PGA circuits 1 – power down analog PGA circuits
PDN_MODE	6	0 – enable analog ADC modulator 1 – power down analog ADC modulator
LINSEL	5:4	00 – no in 01 – MIC1P-MIC1N 10 – MIC2P-MIC2N 11 – MIC1P-MIC1N and MIC2P-MIC2N
LDCM	3	1 – enable DC measurement
DF2SE_15DB	2	0 – 0dB gain for input diff circuits 1 – 15dB gain for input diff circuits

REGISTER 0X22 –PGA GAIN, DEFAULT 00001111

Bit Name	Bit	Description
LPGAGAIN (write to 3:0, but read back from 7:4)	3:0	PGA gain 15 – -3.5 dB (default) 0 – 0 dB 1 – 3 dB 2 – 6 dB 3 – 9 dB 4 – 12 dB 5 – 15 dB 6 – 18 dB 7 – 21 dB Others – 0 dB

REGISTER 0X24 –ADC CONTROL, DEFAULT 00011000

Bit Name	Bit	Description
DMIC_SCALE	7	DMIC gain scale up 0 – normal 1 – 6dB scale up
ADCFSMODE	6	adc fs mode 0 – single speed 1 – double speed
ADCMUTE	5	ADC mute 0 – normal

		1 – mute ADC volume to -96dB
ADCSOFTRAMP	4	adc soft ramp 0 – normal 1 – adc soft ramp enable
ADCHPF	3	0 – disable ADC left channel high pass filter 1 – enable ADC left channel high pass filter (default)
ADCINV	2	0 – normal (default) 1 – left channel polarity inverted
DMIC_SRC	1:0	digital mic control 0x – dmic disable 10 – DMIC high 11 – DMIC low

REGISTER 0X25 –ADC CONTROL, DEFAULT 1100 0000

Bit Name	Bit	Description
ADCVOLUME	7:0	00000000 — 0dB 00000001 — -0.5dB 00000010 — -1dB … 11000000 — -96dB(default)

REGISTER 0X26 –ALC CONTROL, DEFAULT 0001 1100

Bit Name	Bit	Description	
ALCSEL	7:6	00 — alc off 01 —ADC alc on 1x —DAC alc on	
ALCMODE	5	Determines the ALC mode of operation: 0 – ALC mode (Normal Operation) 1 – Limiter mode.	
MAXGAIN[4:0]	4:0	ALC MAXGAIN[1:0] for PGA max gain	
		00000 – -6.5dB 00001 – -5 dB 00010 – -3.5dB 00011 – -2dB 00100 – -0.5dB 00101 – +1dB 00100 – +2.5dB 00111 – +4dB 01000 – +5.5dB 01001 – +7dB 01010 – +8.5dB 01011 – +10dB 01100 – +11.5dB 01101 – +13dB	01110 – +14.5dB 01111– +16dB 10000 – +17.5dB 10001 – +19dB 10010 – +20.5dB 10011 – +22dB 10100 – +23.5dB 10101 – +25dB 10110 – +26.5dB 10111 – +28dB 11000 – +29.5dB 11001 – +31dB 11010 – +32.5dB 11011 – +34dB others – +35.5dB

REGISTER 0X27 –ALC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
MINGAIN[4:0]	4:0	ALC MINGAIN[1:0] for PGA min gain

		00000 – -12dB 00001 – -10.5 dB 00010 – -9dB 00011 – -7.5dB 00100 – -6dB 00101 – -4.5dB 00100 – -3dB 00111 – -1.5dB 01000 – 0dB 01001 – +1.5dB 01010 – +3dB 01011 – +4.5dB 01100 – +6dB 01101 – +7.5dB	01110 – +9dB 01111– +10.5dB 10000 – +12dB 10001 – +13.5dB 10010 – +15dB 10011 – +16.5dB 10100 – +18dB 10101 – +19.5dB 10110 – +21dB 10111 – +22.5dB 11000 – +24dB 11001 – +25.5dB 11010 – +27dB 11011 – +28.5dB others – +30dB

REGISTER 0X28 –ALC CONTROL, DEFAULT 1011 0000

Bit Name	Bit	Description
ALCLVL	7:4	ALC target 0000 – -16.5 dB 0001 – -15 dB 0010 – -13.5 dB …… 0111 – -6 dB 1000 – -4.5 dB 1001 – -3 dB 1010-1111 – -1.5 dB
ALCHLD	3:0	ALC hold time before gain is increased 0000 – 0ms 0001 – 2.67ms 0010 – 5.33ms …… (time doubles with every step) 1001 – 0.68s 1010 or higher – 1.36s

REGISTER 0X29 –ALC CONTROL, DEFAULT 0011 0010

Bit Name	Bit	Description
ALCDCY	7:4	ALC decay (gain ramp up) time at ALC mode/limiter mode: 0000 – 410 us/90.8 us 0001 – 820 us/182us 0010 – 1.64 ms/363us …… (time doubles with every step) 1001 – 210 ms/46.5 ms 1010 or higher – 420 ms/93 ms
ALCATK	3:0	ALC attack (gain ramp down) time at ALC mode/limiter mode: 0000 – 104 us/22.7 us 0001 – 208 us/45.4 us 0010 – 416 us/90.8 us …… (time doubles with very step) 1001 – 53.2 ms/11.6 ms

		1010 or higher – 106 ms/23.2 ms

REGISTER 0X2A –ALC CONTROL, DEFAULT 0000 0011

Bit Name	Bit	Description
WIN_SIZE	4:0	Windows size for peak detector， set the window size to N*16 samples 00110 – 96 samples (default) 00111 – 102 samples ….. 11111 – 496 samples

REGISTER 0X2B –ALC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
ALC_NGG	6	noise gate type 0 – original gain(default) 1 – mute
ALC_NGAT	5	noise gate enable 0 – disable(default) 1 – enable
ALC_NGTH	4:0	Noise gate threshold 00000 – -76.5 dBFS 00001 – -75 dBFS …… 11110 – -31.5 dBFS 11111 – -30 dBFS

REGISTER 0X2C –ADC CONTROL, DEFAULT 0000 1101

Bit Name	Bit	Description
JD_SRC	7	Jack detection pin select 0 – Jack detect from GPIO 1 – Jack detect from RMIC1P
JDSW_POL	6	Jack detection level polarity 0 – low active, low JD input means HP inserted, mute speakers 1 – high active, high JD input means HP inserted, mute speakers
JDSW_EN	5	Jack detection control 0 – Jack detection disable 1 – jack detection enable
HPF_COEFF_S	4:0	HPF slow settling coeff

REGISTER 0X2D –ADC CONTROL, DEFAULT 0000 0110

Bit Name	Bit	Description
ADC_SDP_SRC	7	0 – from adc_cf 1 – from eq_2nd
DAC_DSM_SRC	6	0 – from int 1 – from eq_2nd
EQ_SRC	5	0 – from adc_cf 1 – from int
HPF_COEFF_F	4:0	HPF fast settling coeff

REGISTER 0X2E –ADC CONTROL , DEFAULT 0X1F

Bit Name	Bit	Description
ADC_SHELVING_A[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X2F –ADC CONTROL , DEFAULT 0XF7

Bit Name	Bit	Description
ADC_SHELVING_A[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X30 – ADC CONTROL, DEFAULT 0XFD

Bit Name	Bit	Description
ADC_SHELVING_A[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X31 –ADC CONTROL , DEFAULT 0XFF

Bit Name	Bit	Description
ADC_SHELVING_A[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X32 –ADC CONTROL, DEFAULT 0X1F

Bit Name	Bit	Description
ADC_SHELVING_B[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X33 –ADC CONTROL, DEFAULT 0XF7

Bit Name	Bit	Description
ADC_SHELVING_B[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X34 –ADC CONTROL, DEFAULT 0XFD

Bit Name	Bit	Description
ADC_SHELVING_B[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X35 –ADC CONTROL, DEFAULT 0XFF

Bit Name	Bit	Description
ADC_SHELVING_B[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X36 –DAC CONTROL, DEFAULT 0X00000100

Bit Name	Bit	Description
DACDATSEL	6	0 – SDP Left to out 1 – SDP Right to out
DACMUTE	5	dac mute 0 – normal 1 – mute dac volume to -96dB
DACSOFTRAMP	4:2	dac soft ramp

		000 – off 001 – 0.5 dB per 4 LRCKs (default) 010 – 0.5 dB per 16 LRCKs 011 – 0.5 dB per 32 LRCKs 100 – 0.5 dB per 64 LRCKs 101 – 0.5 dB per 128 LRCKs 110 – 0.5 dB per 256 LRCKs 111 – 0.5 dB per 512 LRCKs
DACINVL	1	0 – normal DAC left channel analog output no phase inversion (default) 1 – normal DAC left channel analog output 180 degree phase inversion

REGISTER 0X37 –DAC CONTROL, DEFAULT 0X00000001

Bit Name	Bit	Description
DACFSMODE	7	DAC fs mode 0 – single speed 1 – double speed
DACAUTOMUTE	5:4	auto mute control 0 – auto mute dis (default) 1 – LOUT auto mute en 2 – SPK auto mute en 3 – LOUT/SPK auto mute en
VPP_SCALE	3:2	00 – Vpp set at 3.5V (0.7 modulation index) (default) 01 – Vpp set at 4.0V 10 – Vpp set at 3.0V 11 – Vpp set at 2.5V
DSM_MUTE	0	DSM mute 0 – DAC DSM unmute 1 – DAC DSM mute

REGISTER 0X38 –DAC CONTROL, DEFAULT 1100 0000

Bit Name	Bit	Description
DACVOLUME	7:0	00000000 — 0dB 00000001 — -0.5dB 00000010 — -1dB … 11000000 — -96dB(default)

REGISTER 0X39 –DAC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
DACOFFSET	7:0	DAC offset

REGISTER 0X3A –DAC CONTROL, DEFAULT 0000 0010

Bit Name	Bit	Description
SHELVING_B1[29:24]	5:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X3B –DAC CONTROL, DEFAULT 0X17

Bit Name	Bit	Description
SHELVING_B1[23:16]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X3C –DAC CONTROL, DEFAULT 0XFD

Bit Name	Bit	Description
SHELVING_B1[15:8]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X3D – DAC CONTROL, DEFAULT 0XFF

Bit Name	Bit	Description
SHELVING_B1[7:0]	7:0	30-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X3E –DAC CONTROL, DEFAULT 0X07

Bit Name	Bit	Description
SHELVING_B2[19:16]	3:0	20-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X3F –DAC CONTROL, DEFAULT 0XFD

Bit Name	Bit	Description
SHELVING_B2[15:8]	7:0	20-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X40 – DAC CONTROL, DEFAULT 0XFF

Bit Name	Bit	Description
SHELVING_B2[7:0]	7:0	20-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X41 –DAC CONTROL, DEFAULT 0000 0000

Bit Name	Bit	Description
SHELVING_A2[24]	0	25-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X42 –DAC CONTROL , DEFAULT 0XFF

Bit Name	Bit	Description
SHELVING_A2[23:16]	7:0	25-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X43 –DAC CONTROL, DEFAULT 0XBB

Bit Name	Bit	Description
SHELVING_A2[15:8]	7:0	25-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X44 – DAC CONTROL, DEFAULT 0XFF

Bit Name	Bit	Description
SHELVING_A2[7:0]	7:0	25-bit a coefficient for shelving filter Default value is {5'h0f, 5'h1f, 5'h0f, 5'h1f, 5'h0f, 5'h1f}

REGISTER 0X45 – 2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B0[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X46 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B0[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X47 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B0[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X48 – 2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B0[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X49 – 2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B1[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X4A –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B1[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X4B –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B1[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X4C –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B1[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X4D –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B2[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X4E –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B2[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X4F –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B2[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X50 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_B2[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X51 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description

EQ1_A1[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X52 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_A1[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X53 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_A1[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X54 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_A1[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X55 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_A2[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X56 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_A2[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X57 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_A2[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X58 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ1_A2[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X59 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B0[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X5A –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B0[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X5B –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B0[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X5C –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B0[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X5D –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B1[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X5E –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B1[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X5F –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B1[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X60 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B1[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X61 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B2[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X62 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B2[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X63 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B2[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X64 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_B2[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X65 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_A1[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X66 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_A1[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X67 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_A1[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X68 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description

EQ2_A1[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X69 –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_A2[29:24]	5:0	30-bit a coefficient for shelving filter

REGISTER 0X6A –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_A2[23:16]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X6B –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_A2[15:8]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X6C –2-BAND EQ, DEFAULT 00000000

Bit Name	Bit	Description
EQ2_A2[7:0]	7:0	30-bit a coefficient for shelving filter

REGISTER 0X6D –GPIO AND INTERRUPT CONTROL, DEFAULT 00000000

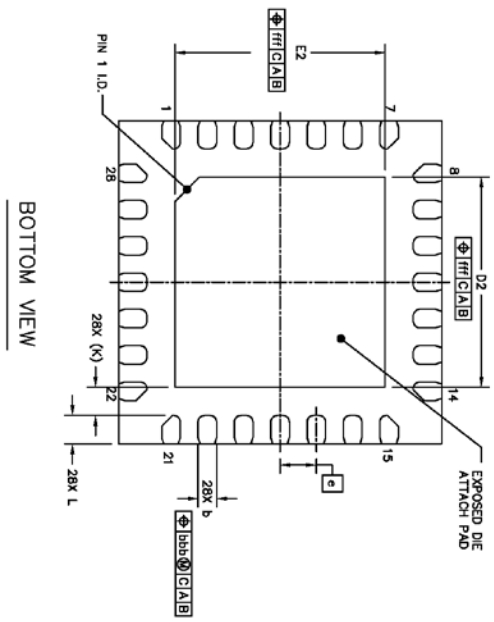
Bit Name	Bit	Description
GPIO1_SEL	7:6	GPIO1 select 0 – HPInserted in 1 – DMIC_SCL out 2 – PLL_OUT out 3 – INT_OUT out
GPIO2_SEL	5	GPIO2 select 0 – Interrupt out 1 – PLL out
INSERT_DEBOUNCE	4:2	Headset Detection debounce 0 – 512fs - 10.6ms 1 – 1024fs - 21ms 2 – 2048fs - 42ms 3 – 4096fs - 84ms 4 – 8192fs - 168ms 5 – 16384fs - 341ms 6 – 32768fs - 682ms 7 – 65536fs - 1364ms
INT_EN	1	Interrupt enable 0 – Interrupt disable 1 – Interrupt enable
INT_POL	0	Interrupt polarity 0 – high active 1 – low active

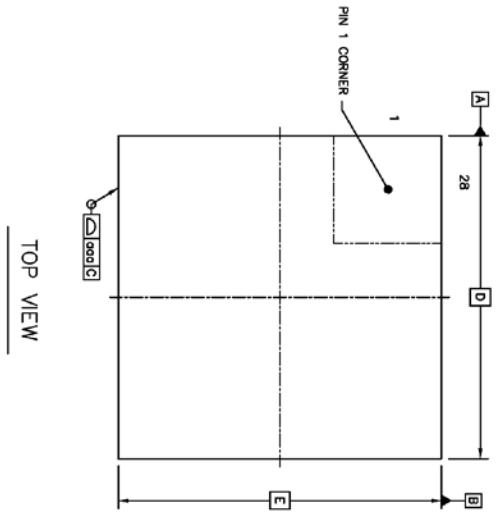
REGISTER 0X6E –FLAGS, DEFAULT 00000000

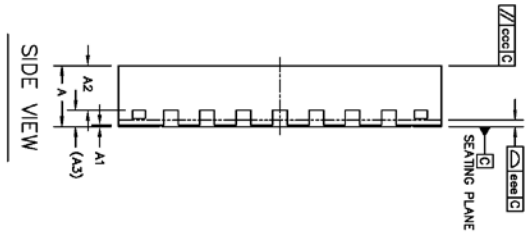
Bit Name	Bit	Description
FLAG_MUTE	7	Mute flag
FLAG_OC	6	Over current flag
CSM_CHIP	5:4	Chip current state machine flag

		00 – PowDown 01 – ChipIni 11 – PowerUp 10 – Normal
FLAG_OTP	3	Over thermal flag
PLL_CAL_ERR	2	PLL calibration error flag
PLLDSM_OVFL	1	PLL DSM overflow flag
FLAGHPINSERTED	0	HP Inserted flag

9. PACKAGE (UNIT: MM)







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.18	0.23	0.28
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.45 BSC	
EP SIZE	X	D2	2.5	2.6	2.7
	Y	E2	2.5	2.6	2.7
LEAD LENGTH		L	0.25	0.35	0.45
LEAD TIP TO EXPOSED PAD EDGE		K		0.35 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

10.CORPORATE INFORMATION

Everest Semiconductor Co., Ltd.

苏州工业园区金鸡湖大道 1355 号国际科技园, 邮编 215021

Email: info@everest-semi.com

11.IMPORTANT NOTICE AND DISCLAIMER

Everest Semiconductor publishes reliable technical information about its products. Information contained herein is subject to change without notice. It may be used by a party at their own discretion and risk. Everest Semiconductor disclaims responsibility for any claims, damages, costs, losses, and liabilities arising out of your use of the information. This publication is not to be taken as a license to operate under any existing patents and intellectual properties.