STAMFORD UNIVERSITY BANGLADESH

Department of Computer Science and Engineering
Final Examination, Spring2023 Semester
CSE 219: Digital Logic & Computer Design
CT: Tamanna Haque Nipa
Date and Time: 10/03/23 & 4:30PM-6:30PM

Batch: MCA-S-Mixed
Duration: 2 hours **Full Marks: 20**

(There are **Two** questions. Answer all of them. Figures in the right margin indicate Marks. Writing anything on the question paper is strictly prohibited.)

1. a) Express the given floating numbers -111.302 in IEEE standard format. [3]
   b) Consider the following page address traces: [5]

      5, 1, 1, 2, 1, 4, 6, 7, 4, 1, 3, 1, 1, 6, 4, 4, 3, 2,

      4 frames are available. Find out the action generated for LRU and OPT replacement policies.
   c) Explain the toggle condition of the JK flip-flop with a proper diagram. [2]

2. a) Design a MOD-13 Synchronous Down Counter. Mention the uses of this counter. [3]
   b) Differences between the followings: [4]
      a. Latch and Flipflops
      b. Combinational and Sequential Circuit.
   c) Draw the logic diagram for 4-bit PISO and 5-bit Ring Counter. [3]

==== GOOD LUCK ====