1. The primary functions of the CPU (Central Processing Unit) are:

a) Fetching: Retrieving commands from reminiscence.
B) Decoding: Interpreting the fetched instructions to decide what operation desires to be performed.
C) Executing: Carrying out the operation or preparation indicated through the decoded practise.
D) Controlling: Managing the waft of data and commands within the CPU and among the CPU and different hardware additives.
E) Arithmetic/Logic Operations: Performing mathematics calculations and logical operations necessary for processing facts.

2. The ALU (Arithmetic Logic Unit) is part within the CPU responsible for appearing mathematics and logical operations. It is closely associated with the CPU as it's far considered one of its primary useful units. The foremost functions of the ALU encompass:

a) Arithmetic Operations: Addition, subtraction, multiplication, and department of numerical facts.
B) Logical Operations: AND, OR, NOT, and other bitwise operations used for records manipulation and decision making.
C) Comparison Operations: Comparing two pieces of statistics to decide equality, inequality, or different relationships.

3. When an interrupt occurs, the CPU wishes to quickly droop its current execution to deal with the interrupt. Here's what occurs:

a) Detection: The CPU constantly monitors for interrupt signals from diverse sources.
B) Handling: When an interrupt is detected, the CPU saves the present day nation of execution (together with application counter and sign in contents) and jumps to an interrupt handler routine.
C) Servicing: The interrupt handler routine executes to cope with the interrupt. Once the interrupt is serviced, the CPU restores the saved state and resumes everyday execution.

Four. For a reminiscence of 2M × 32:

a) Byte-addressable: (2M instances 32 = 2^1 times 2^20 instances 2^5 = 2^26) bits. So, 26 bits are wished.
B) Word-addressable: Since each word is 32 bits, (2M instances 32 = 2^1 instances 2^20 = 2^21) phrases. So, 21 bits are wanted.

Five. Advantages:

a) Memory-mapped I/O permits gadgets to talk directly with reminiscence, simplifying I/O operations and decreasing overhead.
B) Instruction-based totally I/O permits for greater flexibility and control over I/O operations, allowing complicated operations and protocols to be applied efficiently.

6. To provide 4 Kilobytes of memory:

(4 textual content Kilobytes = four instances 1024 text bytes = 4 instances 1024 instances 8 textual content bits)

Each 512 × 8 RAM chip affords (512 instances 8) bits of reminiscence. So, the quantity of chips needed is:

(frac4 times 1024 instances 8512 times eight = 8) chips.

7. For a byte-addressable memory of 20 bytes the usage of 4 modules:

a) High-order interleaving:

```
Module zero: 0, four, 8, 12, 16
Module 1: 1, five, nine, 13, 17
Module 2: 2, 6, 10, 14, 18
Module three: three, 7, eleven, 15, 19
```

b) Low-order interleaving:

```
Module 0: 0, 1, 2, three, 4
Module 1: five, 6, 7, 8, 9
Module 2: 10, 11, 12, 13, 14
Module 3: 15, 16, 17, 18, 19
```

8. For a 4M × 32 main reminiscence:

a) Number of RAM chips needed: (4M instances 32 / (128K instances 8) = 32) chips.
B) When having access to a complete word, all 32 chips may be involved.
C) Number of banks: (32) banks.
D) Number of cope with bits wished: (log_2(4M) = 22) bits.
E) For excessive-order interleaving, the address 7060016 would be placed in bank 0.
F) For low-order interleaving, the cope with 2C77D516 might be positioned in bank 29.

9. The fetch-decode-execute cycle includes the following steps:

a) Fetch: The CPU retrieves the following training from reminiscence, placing its cope with into the MAR (Memory Address Register) and transferring the preparation into the MBR (Memory Buffer Register).
B) Decode: The CPU translates the fetched instruction, figuring out the operation to be accomplished and the operands concerned.
C) Execute: The CPU incorporates out the operation indicated by means of the decoded guidance, the use of the ALU and other relevant components.

D) Update: Any necessary updates to the CPU registers or reminiscence are finished based totally on the finished practise.

10. In MARIE, the MAR (Memory Address Register) is most effective 12 bits huge whilst the AC (Accumulator) is 16 bits huge due to the fact:

a) MAR is used to cope with reminiscence locations, and in MARIE, the memory length is confined to (2^12) locations, which may be addressed the usage of 12 bits.
B) AC is used to save records and computation results, and a much wider width (sixteen bits) allows for large numerical values and extra precise calculations.