2018 Second International Conference on Advances in Electronics, Computer and Communications (ICAECC-2018)

# Data Rate Based Performance Analysis and Optimization of Bulk OUT Transactions in USB 3.0 SuperSpeed Protocol

Adithya Rangan C.K.*, Aravinda Holla K.†, Vikas Kulkarni‡, Anurag Kumar§, Akshay Patil¶
*Innovative Logic Design Services Pvt. Ltd.,Bangalore Email: aditya@inno-logic.com
†Innovative Logic Design Services Pvt. Ltd.,Bangalore Email: aravinda@inno-logic.com
‡Innovative Logic Design Services Pvt. Ltd.,Bangalore Email: vikas@inno-logic.com
§Innovative Logic Design Services Pvt. Ltd.,Bangalore Email: anurag@inno-logic.com
¶Innovative Logic Design Services Pvt. Ltd.,Bangalore Email: Akshay@inno-logic.com

***Abstract*—USB 3.0 SuperSpeed is one of the most widely used serial communication protocols that interface various electronic devices. It provides a signaling rate as high as 5 Giga Bits Per Second and raw data rate of 400-500 Mega Bytes Per Second with functional overheads. With transfers such as Bulk, Isochronous, Interrupt, Control types; Bulk transactions are highly acclaimed due to their efficient utilization of bandwidth and guaranteed delivery of integral data between host and device. Hence, data rate based performance becomes an inherent criterion to verify that the design and implementation conforms to the protocol standards and system requirements. The analysis and characterization of performance based on data rate provides the necessary information so as to improve the robustness and accuracy of the design. Different parameters that may be tun-able act as causative factors in enhancing or degrading the data rate. This paper presents an elaborate description of various facets through which data rate based performance analysis is achieved for USB 3.0 SuperSpeed Bulk OUT transactions. This paper also deals with the characterization and statistical variation of causative factors for different scenarios to obtain minimum, maximum and ideal data rate thus leading to optimum performance.**

***Keywords*—USB 3.0 SuperSpeed Bulk OUT transaction, Performance analysis, Data rate characterization, Data rate optimization**

## I. Introduction

Data rate analysis and optimization form a major field of verification with respect to accuracy and precision of design and implementation of USB 3.0 SuperSpeed protocol. The point of view is to obtain a value that is closer to the raw data rate of around 400-500 Mega Bytes per Second (MBps) without violating protocol specifications and satisfying system requirements. USB 3.0 SuperSpeed Bulk transaction supports reliable data transfer with integrity between host and device thus posing a new challenge to ascertain optimum data rate. Bulk transactions can be either Bulk IN, where data flow is from device to host, or Bulk OUT where data flow is from host to device. All transactions are always initiated by the host through a request acknowledgement in case of Bulk IN, and a data packet in case of Bulk OUT, which depict the readiness of the host to accept data or transmit data respectively.[1][2] Bulk IN and Bulk OUT transfers are carried out through one or more endpoints with a maximum of 15 endpoints for data flow and one control endpoint for control flow. Bulk OUT transaction has a vital role in analyzing the device's capability to accept data packets from the host.[3][4] The host initiates Bulk OUT transaction by sending a data packet (DP OUT) to the device. The device responds with a response acknowledgement (ACK) transaction packet (TP) which also acts a request ACK TP for the next packet to be received from the host. The device sends ACK TP if it is able to receive and accept DP OUT from the host. The device may also respond with a Not Ready (NRDY) TP depicting its inability to accept DP OUT. An Endpoint Ready (ERDY) TP is consequent to NRDY depicting the readiness of device to accept DP OUT. ACK TPs and DP OUTs are identified through the sequence number which varies from 0 to 31 and has a 1:1 relationship between DP OUT and ACK TP. ACK TPs may be sent asynchronously by the device to host at any instant of time after the reception of corresponding DP OUT with the boundary that all ACK TPs are to be sent before the completion of transaction.[5][6] Burst transfers allow data to be transferred in terms of bursts where data packets are delimited based on burst size. DP OUT with error injected are responded with Retry acknowledgement (ACK with Rty=1) TP from the device for which the host may resend the same DP OUT without error. Normal data flow may be interrupted by flow control mechanism which may occur due to generation of NRDY TP or Terminating Acknowledgment (ACK with NumP=0) TP due to which data transfer stagnates for a measurable interval of time. Both NRDY TP and ACK with NumP=0 TP are always followed by ERDY TP to resume the transfer. While NRDY TP refers to inability of device to receive data, ACK with NumP=0 TP refers to non-availability of space for the device to accept the data. Hence, the host waits for ERDY TP from device till it can send any pending DP OUTs or initiate another transaction.[7][8][9] Thus, with the background of data and control flow of USB 3.0 Bulk OUT transaction, this paper presents the performance analysis with respect to data rate for which various scenario based test cases are run on Linux Fedora 2.24.0 platform with ncsim tool of Cadence software and Simvision 14.10 tool for waveform observation. Algorithms and computation formulae for data rate are shown to arrive at data rate characterization.

978-1-5386-3785-2/18/$31.00 

## II. Various Facets of Performance Analysis

Bulk OUT transactions of USB 3.0 SuperSpeed protocol are mainly analyzed based on the capability of device to receive and accept data packets from the host for a given transaction time interval. Thus, efficiency of the transfer has primary dependency on the packets such as NRDY, ERDY and ACK with NumP=0. The PISTON model helps in providing broader input on the inter-dependency of these packets as well as their effect on the data rate as shown in the Equations 1 to 6.[10] However, some preliminary conditions are taken into account for achieving data rate as much optimized as possible.

$$No.of ACKTPs \propto No.of DPOUTs \tag{1}$$

$$No.of ERDYTPs \propto No.of NRDYTPs \tag{2}$$

$$No.of ERDYTPs \propto No.of ACKTPswithNumP = 0 \tag{3}$$

$$DataRate \propto Inverse[No.of NRDYTPs] \tag{4}$$

$$DataRate \propto Inverse[No.of ERDYTPs] \tag{5}$$

$$DataRate \propto Inverse[No.of ACKTPswithNumP = 0] \tag{6}$$

Associated with the proportionality equations, is the data rate calculation which forms the base for performance analysis. Equation 7 depicts the data rate calculation $DataRate_{Bulk-OUT}$ based on the generic algorithm for Bulk OUT transaction.[11]

$$DataRate_{Bulk-OUT} = (dl * np)/(t_{Bulk-OUT}) \tag{7}$$

where $np$ represents the number of packets corresponding to data length $dl$ and $t_{Bulk-OUT}$ is the total time for transaction completion.

Various facets of performance analysis involve the proposition and realization of scenarios that inherently result in optimum data rate. These scenarios are transfer of non-erroneous packets, full length data packets and avoidance of zero length data packets, usage of one Bulk OUT endpoint at a time exclusively without Bulk IN endpoints, uniformity of all data packets with transfer completion.[12][13][14] In terms with the above factors, the methodology of inter tun-able design constraints is applied in order to analyze and characterize performance and obtain optimum data rate.[15] The variation of parameters is as explained below -

- ***Processor Clock Frequency*** – Processor clock frequency plays a vital role in deciding how fast the host can send data packets to the device adhering to synchronization. [16][17] Processor clock frequency is varied from a maximum of 500 MHz, a mediocre of 250 MHz and a minimum of 125MHz.
- ***Data Length of each packet and Number of packets*** -For transferring data of around 1 MB, two combinations of data length and number of packets are realized i.e. 1024 packets with a data length of 1024 bytes or 64 repetitions with data length of 16384 bytes.
- ***Burst Size*** - Burst size depicts the number of packets that could be sent in a single burst. The value is varied between two ends i.e. burst size of 2 where each burst can incorporate a maximum of only 2 packets and burst size of 16 where 16 packets can be transferred in a single burst.
- ***Bus Configuration*** - Different system bus configurations contribute to data rate variation and AXI/AHB bus configurations are interchangeably used for various design constraint combinations.
- ***Direct Memory Access (DMA)*** -DMA feature helps to increase data rate and scenarios are implemented with and without DMA enabled for performance characterization.

## III. Data Rate Characterization and Analysis of Different Parameters

The characterization of data rate for USB 3.0 SuperSpeed Bulk OUT transaction is based on analysis of different parameters of concern that lead to either increase or decrease of throughput or the performance. Various test cases corresponding to the scenarios are run using ncsim 14.10 tool of Cadence on Linux Fedora 2.24.0 platform with Simvision version 14.10 for monitoring the wave forms as observed in Figure 1 inorder to identify the begin and end points as well as number of packets and data length as specified in the data rate computation formula.

The efficiency is decided by various combinations of such parameters; however an analytic understanding of statistical changes with respect to different scenarios provides a better platform to arrive at the extreme case results. The description is as follows -

- ***Data Rate*** - Data rate is obtained to have the highest value for a scenario that involves a transaction of 1 MB of data i.e. 64 repetitions of data length of 16384 bytes each for DMA transfer with a burst size of 16 and AHB bus configuration at a processor clock frequency of 500MHz. Additionally, some observations on data rate variation are as follows -
  - Data rate always stands at a higher value for a higher burst size of 16 as compared to a lower burst size of 2 due to reduced number of ACKs with NumP=0 generated by device for every burst as well as reduced number of NRDYs generated at every burst initiation.
  - Data rate remains same for Non DMA transfer with both AHB and AXI bus configurations at lower processor clock frequencies of 125 MHz and 250 MHz.
  - Data rate for DMA transfer with AHB bus configuration is greater than that with AXI bus

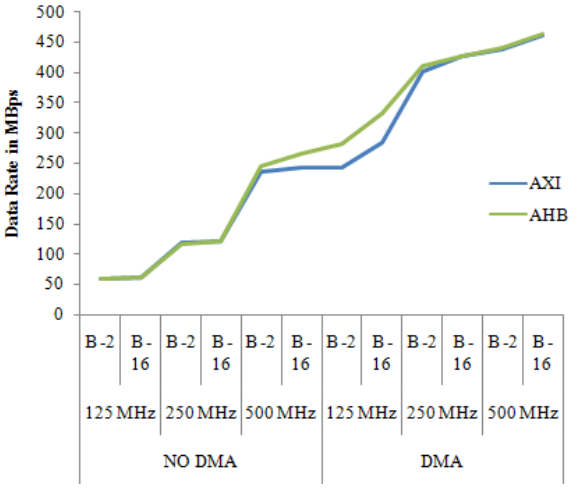


Fig. 1: Data Rate Variation

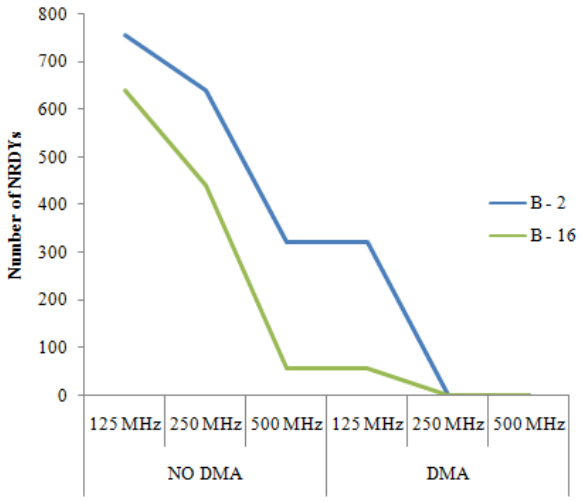


Fig. 2: NRDY Variation

configuration at lower processor clock frequencies of 125 MHz and 250 MHz.

- Data rate for transactions with AHB/AXI bus configurations are same at a processor clock frequency of 500MHz.
- Generally, data rate increases with increasing clock frequency i.e. from 125MHz to 500MHz.
- Data rate is almost same for transferring 16384 bytes with a repetition of 64 or 1024 packets with data length of 1024 bytes except at 500 MHz, where the former data rate is higher.

Figure 1 depicts the variation of data rate at different clock frequencies with AXI and AHB bus configuration for both DMA and Non DMA transfers for burst size of 2 and 16.

- ***NRDY*** - NRDY inherently reduces data rate to a greater extent, given its inverse effect on throughput by introducing flow control mechanism thus stagnating regular data flow. The observations based on scenarios are as follows -
  - No NRDYs are generated for a scenario of transferring 1024 packets of data length 1024 bytes each, thus constituting a total of 1 MB data.
  - The number of NRDYs is initially constant for both DMA and Non DMA transfers at 125MHz processor clock frequency for transferring 64 repetitions of 16384 bytes and eventually decreases to zero with increasing processor clock frequency up to 500MHz for both AXI and AHB bus configurations.
  - The number of NRDYs gets reduced more steeply for burst size of 16 compared to 2 with increasing clock frequency.

  Figure 2 shows variation of number of NRDYs at different processor clock frequencies with DMA and Non DMA transfers for burst 2 and 16.

- ***ACK with NumP=0*** - ACK with NumP=0 is also one of the parameters that induces flow control mechanism

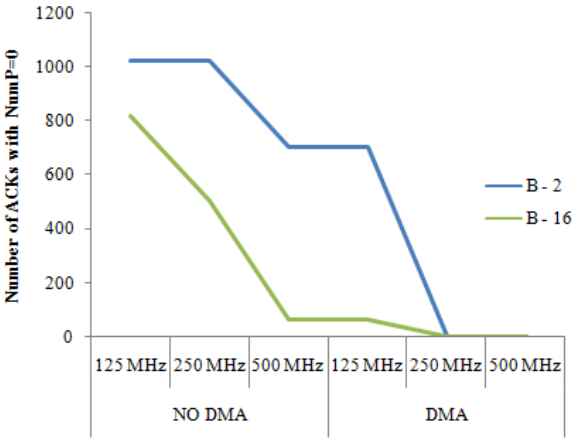


Fig. 3: ACK with NumP=0 Variation

thus interrupting normal data flow. With respect to the scenarios, following are the observations-

- The number of ACKs with NumP=0 shows similar variation as that of the NRDYs for a transaction involving 64 repetitions of 16384 bytes of data packets for burst size of 2 and 16.
- The number of ACKs with NumP=0 is constant for Non DMA transfer and decreases gradually to zero for DMA transfer with increasing processor clock frequency till 500MHz for transferring 1024 packets of 1024 bytes for either AXI or AHB bus configurations with burst size 2 or 16.
- The number of ACKs with NumP=0 for burst size of 16 reduces more steeply with increasing clock frequency when compared to burst size of 2.

Figure 3 depicts variation of number of ACK TPs with NumP=0 in terms of burst size and processor clock frequency for DMA and Non DMA transfers.

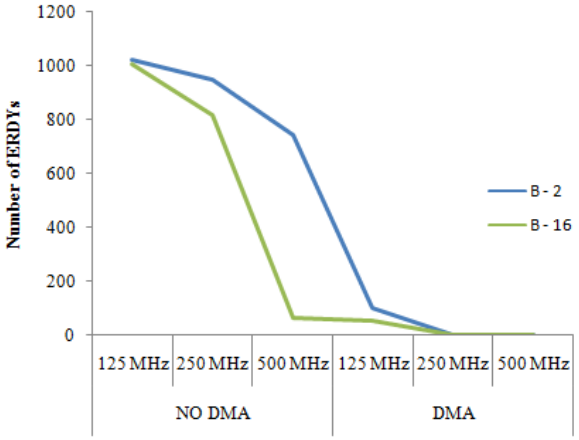


Fig. 4: ERDY Variation

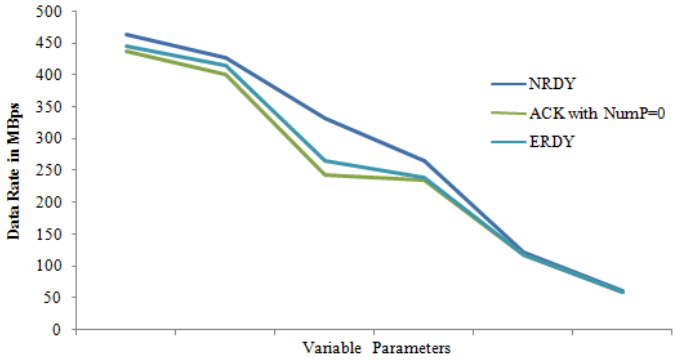


Fig. 5: Data Rate Variation in terms of Causative Parameters

- ***ERDY*** - The generation of ERDY is in response to NRDY and hence is directly proportional to the number of NRDY packets generated. Additionally, ACK with NumP=0 is also followed by an ERDY.[18][19][20] Hence, it could be inferred that more number of ERDYs generally reduce data rate with their necessity to come out of flow control mechanism and get back to data transfer. ERDY only acts as a tertiary reference in data rate analysis and may not be the primary source of data rate deterioration. The variation of ERDY is observed as follows -
    - The number of ERDYs decreases with increasing processor clock frequency from 125 MHz to 500 MHz. While the reduction is less steep for burst size of 2 than 16 for Non DMA transfer, the number of ERDYs drastically reduces and becomes zero at 500MHz for DMA transfer for burst size of both 2 and 16.
    - The number of ERDYs generated is less for a transaction involving 64 repetitions of 16384 bytes as compared to 1024 packets of 1024 bytes each. This appears sharper at higher processor clock frequencies.

  Figure 4 depicts variation of number of ERDYs for different processor clock frequencies with respect to burst size for DMA and Non DMA transfers.

## IV. Data Rate Optimization through Statistical Analysis of Causative Parameters

The performance of USB 3.0 SuperSpeed Bulk OUT transaction is decided by the data rate or throughput which needs to be optimized to arrive at the best case results with the consideration of supporting scenarios.[21][22][23] As discussed in the previous sections, data rate of Bulk OUT transaction is inversely proportional to number of NRDYs, ACKs with NumP=0 and consequently ERDYs. Thus, over a range of different scenarios, the statistical variation of causative parameters acts as a platform to enhance the data rate as much as possible. The analysis shows that the best data rate that is in terms with the maximum achievable value can be obtained generally at higher processor clock frequencies for AHB bus configuration while transferring 1 Mega Bytes of data in a combination of 64 repetitions of 16384 bytes using DMA. Minimum number of NRDYs is obtained for the same scenario with the exception that transfer involves 1024 packets of 1024 bytes each. Bus configuration i.e. either AXI or AHB does not affect the variable generation of NRDY and hence choice may be done with respect to obtaining best data rate. The same scenario holds good for variation of ACKs with NumP=0 and ERDYs as well. Overall, the causative parameters are quantitatively lesser and show steeper reduction tending to zero in DMA transfer as compared to Non DMA transfer with increasing processor clock frequency for burst size of both 2 and 16. Hence, in totality, the above scenarios help to obtain the maximum data rate with optimizations that are user-dependent. Additionally, ideal case scenarios are those where-in data rate may not be maximum but optimum enough to ensure that there are no NRDYs, ERDYs or ACKs with NumP=0 generated. This includes a scenario of data transfer with DMA enabled with a processor clock frequency of 500MHz for a burst size of 2 or 16 with AXI bus configuration. Minimum data rate may be obtained as a worst case result with a scenario involving data transfer without DMA at 125MHz and burst size of 2 with AXI bus configuration.

Data Rate based performance characterization and optimization can also be inferred through inter dependency of causative parameters as well as combined effect of the same on the data rate. The statistical analysis of these parameters from various scenarios helps in arriving at an optimum data rate that could be realized in real time. Figure 5 depicts variation of data rate with respect to other causative parameters such as NRDY, ACK with NumP=0 and ERDY. As depicted in the figure, data rate increases with decrease in the number of ACKs with NumP=0, which is steeper than the number of NRDYs and ERDYs. Hence, selection of the scenarios must be such that minimum number of ACKs with NumP=0 might be generated and at the same time, a fine line should demarcate the threshold to NRDY generation.

## V. Merits and Challenges

Data Rate based Performance Analysis and Optimization of USB 3.0 SuperSpeed Bulk OUT transaction has an underlying merit of characterizing data rate through variation of parameters for different scenarios that are deemed essential to obtain the best possible data rate that is closer to the value defined by the protocol specification. At the same time, it also paves the

way to verify that the protocol design and implementation is within the boundary of the specification and equally satisfy the system requirements. While adhering to expected output forms a major part, assurance that the implementation gets validated without overlooking functionality bugs gives an additional merit of interest.[24][25][26] The advantage of performance analysis and optimization, thereof, is to probe into every possibility to improve the design and arrive at accurate and precise values of data rate. This also provides the validation that the design conforms to the specifications at the intellectual property (IP) level. A probable challenge that might be faced during the process is the wrong identification of packets or synchronization issues in detecting and deciphering packet information that leads to misleading results. Time-stamps corresponding to wrongly identified packets further result in inefficient calculations which should be avoided through proper utilization of algorithms for data rate calculation. The prime challenge is to obtain best possible results sans protocol violation.

## VI. Related Works and Future Scope

The process of optimizing and characterizing the data rate based performance of USB 3.0 SuperSpeed Bulk OUT transaction nurtures the path towards data rate enhancement that could be channelized through hot spots in the design which could make it more reliable and bug-free. The extension of this process may be suited to implement a data rate engine specifically that would suffice for all the parameters that may be included to arrive at the results for every scenario. Automation of such a computation could also be implemented with different types of data transfers for similar protocols on a large scale.

## VII. Conclusion

This paper discusses the data rate based performance characterization and optimization of USB 3.0 SuperSpeed Bulk OUT transaction. Different causative parameters that contribute towards enhancement or deterioration of data rate are noted, and their effect on data rate is inferred through observations based on scenarios built upon by various facets of performance analysis. Data rate variation is analyzed statistically through tuning of causative parameters between extreme ends. The inter dependency of parameters is explained and the best case results and associated scenarios is observed for obtaining optimum data rate. Minimum and maximum data rate scenarios as well as ideal cases are shown. Thus, the importance of performance analysis and optimization based on data rate is portrayed for design implementation and verification.

## Acknowledgment

The authors would like to acknowledge their thanks to Mr. Dinesh Tyagi, President and CEO, Innovative Logic Inc. and all other team members of Innovative Logic Design Services Pvt. Ltd. for their valuable technical and non technical support.

## References

[1] USB-Implementers-Forum. *Universal Serial Bus 3.0 Specification. including errata and ECNs through May 1, 2011*. English. 1.0. Hewlett-Packard Company, Intel Corporation, Microsoft Corporation, NEC Corporation, STEricsson, Texas Instruments. USB Implementers Forum, 1. Chap. 1–8, pp. 1–340. 631 pp. URL: http://www.usb.org.

[2] *USB 3.0 Technology*. HP Technologies. 2. URL: http://h20195.www2.hp.com/V2/GetPDF.aspx/4AA4-2724ENW.pdf.

[3] *USB 3.0 IP SuperSpeed Device Controller IP*. Inno Logic Inc. URL: http://inno-logic.com/usb-3-otg/.

[4] *USB 3.0 FAQ Sheet*. Targus. URL: http://targus.com/hk/downloads/usb-3_faq_sheet.pdf.

[5] "USB 3.0 SuperSpeeds". In: (2011). URL: http://www.usr.com/en/education/usb-30-peripherals/.

[6] *USB Overview*. Silicon Labs. 2011. URL: http://www.silabs.com/Support%20Documents/Software/USB_Overview.pdf.

[7] *Intel Universal Serial Bus (USB) Frequently Asked Questions (FAQ)*. Intel Corporation. 2014. URL: http://www.intel.in/content/www/in/en/io/universal-serial-bus/universal-serial-bus-faq.html.

[8] Terry Moore. "USB 3.0 Technical Overview". In: (8). URL: http://www.mcci.com/mcci-v5/pdf/972156a_%28MCCI-USB3-TechnicalOverview%29.pdf.

[9] Francis Chao. "USB 3.0 vs USB 2.0 ys eSATA". In: (2011). URL: http://aztcs.org/meeting_notes/winhardsig/USB3/USB3versus.pdf.

[10] Adithya Rangan CK, Vikas Kulkarni, and HR Shashidhara. "A Theoretical Proposition to Characterize Speed Based Performance of Bulk Transaction in Universal Serial Bus 3.0 SuperSpeed Protocol". In: ISBN - 978-1-5090-2399-8. 2016, pp. 49–54.

[11] Adithya Rangan CK, Aravinda Holla K, and Vikas Kulkarni. "A Generic Algorithm for Speed Based Performance Estimation and Computation for Universal Serial Bus 3.0 SuperSpeed Bulk Transaction". In: *ICRAECT 2017 International Conference on Recent Advances in Electronics and Communication Technology*. ISBN - 978-1-5090-6701-5/17. IEEE. IEEE Bangalore Section, pp. 90–95.

[12] *USB 3.0 – Background Factors, New Features, and Applicability as a Camera Interface*. IDS Imaging Development Systems GmbH. 2012. URL: www.ids-imaging.com.

[13] Ankur Tomar and Edmund Linn. "Introduction to SuperSpeed USB 3.0 Protocol". English. In: 1 (2011). Ed. by Farnell, pp. 1–20. URL: https://www.element14.com/community/servlet/JiveServlet/previewBody/36206-102-2-218482/Introduction%20to%20USB%203.0%20Protocol.pdf.

[14] *USB 3.0 Internal Connector and Cable Specification. Revision 1.0*. Intel Corporation. 20. Chap. 1–3, pp. 10–22. URL: http://www.intel.in/content/dam/doc/technical-specification/usb3-internal-connector-cable-specification.pdf.

[15] Adithya Rangan CK, Aravinda Holla K, and Vikas Kulkarni. "Modeling of Inter-Tunable Design Constraints for Performance Optimization Through Data

Rate Enhancement of USB 3.0 Superspeed Bulk Transactions". In: *DVCON - INDIA 2017*. Accellera.

[16] LC Wu. "Motherboard with universal series bus connector". GEN US20120033369. Google Patents. 9. URL: https://www.google.com/patents/US20120033369.

[17] W Szeremeta and MN Trinh. "Universal test connector for connecting a SATA or USB data storage device to a data storage device tester". GEN US8753146. Google Patents. 17. URL: https://www.google.com/patents/US8753146.

[18] *Data Manual - TUSB1310 USB 3.0 Transciever*. Texas Instruments. 2009, pp. 10–21. 37 pp. ISBN: SLLSE16E. URL: http://www.ti.com/cn/lit/pdf/sllse16.

[19] Robert A. Dunstan, Gary A. Solomon, and Joseph A. Schaefer. "Universal Serial Bus Host to host communications". GEN US20100169511. Google Patents. 1. URL: https://www.google.com/patents/US20100169511.

[20] D. Luke. "Simplified universal serial bus (USB) hub architecture". GEN US7657691. Google Patents. 2. URL: https://www.google.com/patents/US7657691.

[21] A.and KADOI R. Yamamoto and M. Tone. "Wireless communication system". GEN US20110064023. Google Patents. 17. URL: https://www.google.com/patents/US20110064023.

[22] P Hung, T Sakurai, and PWW Fung. "Method and Apparatus of USB 3.0 Based Computer, Console and Peripheral Sharing". GEN US20110113166. Google Patents. 2011. URL: https://www.google.com/patents/US20110113166.

[23] NC Chang. "USB female connector". GEN US7927145. Google Patents. 19. URL: https://www.google.com/patents/US7927145.

[24] H Van Antwerpen and H. Letourneur. "USB port connected to multiple USB compliant devices". GEN US8364870. Google Patents. 29. URL: https://www.google.com/patents/US8364870.

[25] PS Hung and T Sakurai. "Translation USB Intermediate Device and Data Rate Apportionment USB Intermediate Device". GEN US20110022769. Google Patents. Jan. 27. URL: https://www.google.com/patents/US20110022769.

[26] MI Kakish. "Motherboard Compatible with Multiple Versions of Universal Serial Bus (USB) and Related Method". GEN US20110191503. Google Patents. 4. URL: https://www.google.com/patents/US20110191503.