Simultaneous Switching Noise Impact to Signal Eye Diagram on High-Speed I/O

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Abstract
Simultaneous Switching Noise (SSN) is increasing with higher I/O data rate, resulting into more challenges in regulating supply voltage noise. SSN increases jitter in high-speed interface circuit and limits the performance of I/O. In order to reduce SSN effect to supply voltage droop, Power Distribution Network (PDN) has to be designed optimally. PDN design goal is to reduce the power supply noise going into I/O circuit. Engineering efforts are focused on packaging and board routing in order to control the impedance profile and supply voltage droop within the design specification. This paper discusses the next level of investigation, quantifying the effect of supply noise to the I/O transistor level circuit performance, specifically on Universal Serial Bus (USB) transmitter circuit. Output of the USB's transmitted signal is shown in eye diagram with the existence of supply noise throughout PDN. Results show that the USB transmitter circuit can sustain with higher supply noise drop than the targeted PDN design.

Keywords
Simultaneous Switching Noise (SSN), Universal Serial Bus (USB), Transmitter, Eye Diagram, Power Supply Noise.

1. Introduction
Transistor size is shrinking to get higher clock speed, higher data rate, and lower power consumption. Operating voltage is also scaled down to achieve low power consumption in line with reduction in transistor's size. Additionally, design target of supply voltage droop is tightening because of lower supply noise margin, together with the scaling down of the operating voltage.

While technology demand is scaling down the operating voltage to fulfil low power consumption, it also has to meet with high data rate as market demands. Switching activities occur in transistor level during data transfer through the I/O channels. These switching activities in high-speed I/O produce significant voltage droop throughout PDN and this is transferred into on die's power supply. Increase in switching activities and number of I/O ports will lead to bigger voltage drop across PDN and will cause to fluctuation of the supply voltage noise. When many switching activities happen at the same time, it induces SSN in power supply.

SSN is a main concern in transistor level circuit. Previous research has shown some ways to simulate the SSN using tool such as SIGRITY [1] and also throughout measurement [2]. Study of SSN impact to high-speed I/O design is necessary due to noise impact in PDN which will influence both signal quality and timing impacts. This can be seen from previous study which correlated both crosstalk and simultaneous switching into lateral pull in and push out of timing diagram [3]. In some extreme cases of simultaneous switching, they can cause to I/O failure. SSN does not produce a timing impact at all the circumstances. SSN is harmful especially when there is a relative movement between the signal and its sampling signal.

In order to handle SSN, PDN is designed specifically to meet its peak-to-peak voltage droop target. Different approaches are evaluated in order to optimize the power delivery path. Options can be for example, via designing with a different chip packaging technology to meet required electrical needs [4] or using more advanced substrate technologies [5] for better power delivery. Essentially, these methods are trying to reduce the inductive and resistive elements on the PDN path and so to minimize the effect of IR drop and $L*di/dt$ droops.

Additionally, the right decoupling capacitor value and its placement plays an important part in reducing noise induced in power supply [6-7]. Via these decoupling capacitors, the total impedance in the power delivery path is reduced by reducing the current return path. By this method, it reduces the inductance path of the PDN. Furthermore, the capacitors store and supply charge to transistors when there are switching activities whereby current is drawn from voltage supplies. Although it can significantly reduce the supply voltage noise induced by SSN, it increases the cost of designing the PDN.

The goal of optimizing a PDN design is to reduce the effect of power supply noise to the transistors. However, the target peak-to-peak voltage droop is mainly set through previous product assumption and targets with little investigation into the actual effect to circuit performance. Single target impedance is set in a PDN design and is enforced across whole frequency range. This is not an effective way of designing PDN, giving rise to instances of overdesigned solutions. Hence, it is needed to study the effect of supply noise in transistor level circuit. In some cases, circuit may only be sensitive to a specific frequency range and less sensitive to another frequency range. This is shown in supply noise induced jitter in high-speed I/O from previous analysis [8].

Publications [4-7] have emphasized on effective way of suppressing noise and optimizing power delivery path. These papers have demonstrated the conventional way of designing a PDN with low supply noise. Different with previous publications, this paper aims to bring out the important of combining PDN and transistor circuits together

into single simulation. The effect of excessive voltage droop to transistor circuit is observed and can be used as reference for future design.

In this paper, the impact of simultaneous switching induced supply voltage noise is studied and simulated on a USB transmitter circuit performance. Its effect on the USB transmitter is quantified through eye diagrams. In brief, this paper goes as follow. Section 2 elaborates the methodology and the simulation setup of the process. The comprehensive simulation results are shown in Section 3. In section 4, discussion based on the results, analysis and findings is explained. Finally, Section 5 concludes the paper.

2. Methodology and Simulation Setup

In this research, USB transmitter simulation test bench is employed with actual transistors to represent the die excitation. Simulation is carried out using SPICE model with fixed temperature settings at 50°C in typical corner process. Pre-emphasis of the USB transmitter is turned off with pre-charge is enabled. The main parameters to study in this research are the USB core voltage (1.05 V), the differential signal pair (+) and the differential signal pair (-).

The PDN model is shown in Figure 1. PDN modelling starts from Voltage Regulator Module (VRM), including board power planes, vias and package structures. PDN is extracted into SPICE compatible netlist through a power delivery extraction tool for simulation in circuit transistor environment.

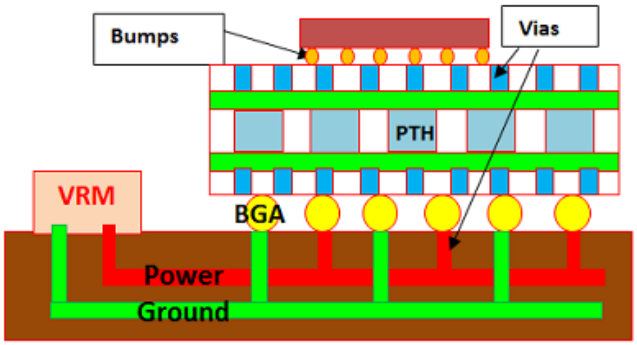

Figure 1: Power Distribution Network overview

Additionally, channel model is added into the transmitter output differential signal (+) and signal (-) to include the channel effect. It is important to include channel model in the simulation as this will add losses and delays to the signal. This is to ensure that the signal waveform matches as close as possible with the model on chip.

The channel modelling setup for USB transmitter is shown in Figure 2. It shows the overall channel modelling in a signal transmission through package and motherboard. In USB's transmitter, the signal will start to transfer from buffer into bump and breakout region of the package. Figure 3 shows an example of a breakout region in a package. From breakout region, signals are routed through package traces to the bottom of package through vias and go into the motherboard through BGAs.

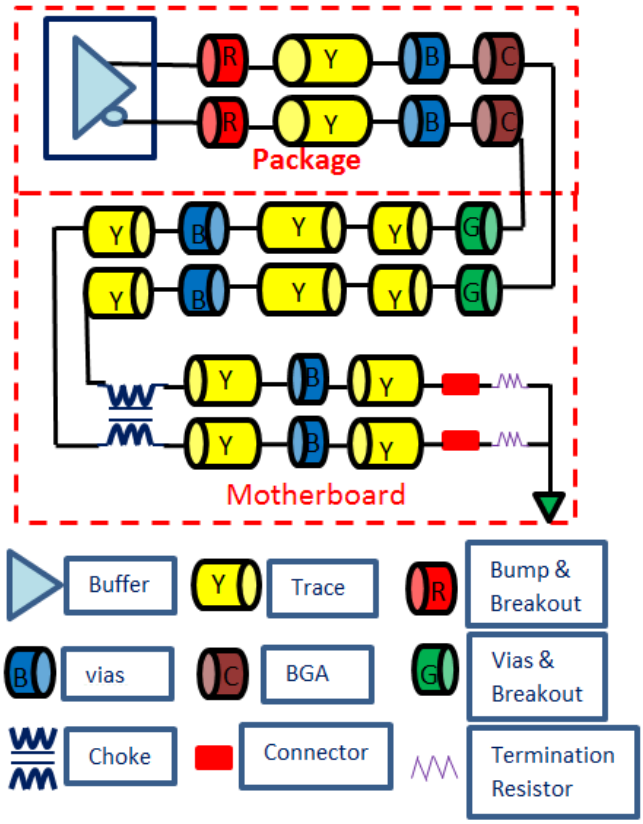

Figure 2: Signal channel modelling overview

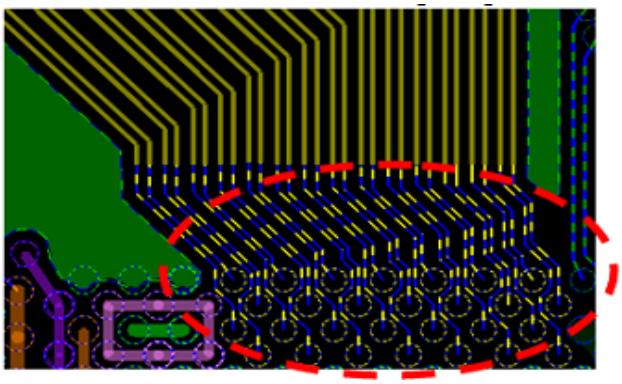

Figure 3: Breakout region in package

By connecting the PDN and channel model together, this will form a more realistic circuit as shown in Figure 4. With full PDN modelling, voltage drop can be observed on power supply rail when the transistor is switched. The output signal fluctuation cause by voltage drop from PDN can also be seen on the eye diagram. When simultaneous switching events happen in the transmitter, the voltage drop becomes bigger.

The worst case voltage droop is expected when 14 ports of USB transmitters are turned on at the same time or at the time that all of them are transmitting data. Simulation is done to carry out the worst case noise produced by 14 ports of USB transmitters that being turned on simultaneously. Supply noise having decoupling capacitor is compared with supply noise without decoupling capacitor. With the supply

voltage droop waveform, the output signal of USB transmitter is studied in eye diagram to check the effect of supply noise to the output signal waveform.

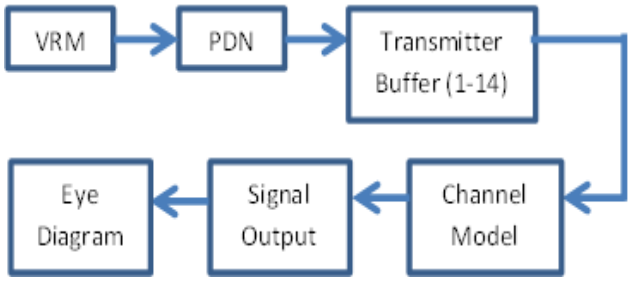

Figure 4: Full transmitter test bench overview

3. Simulation Results

On a channel modelling with 1.05 V input voltage setup, the result of eye diagram can be seen as in Figure 5. The distortion observed on the signals is due to channel losses and delays.

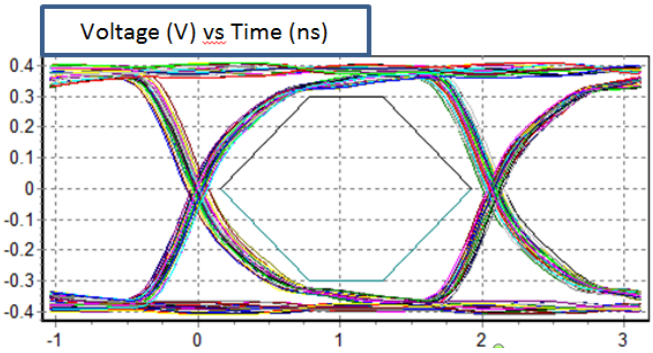

Figure 5: Eye diagram of transmitter's signal without PDN

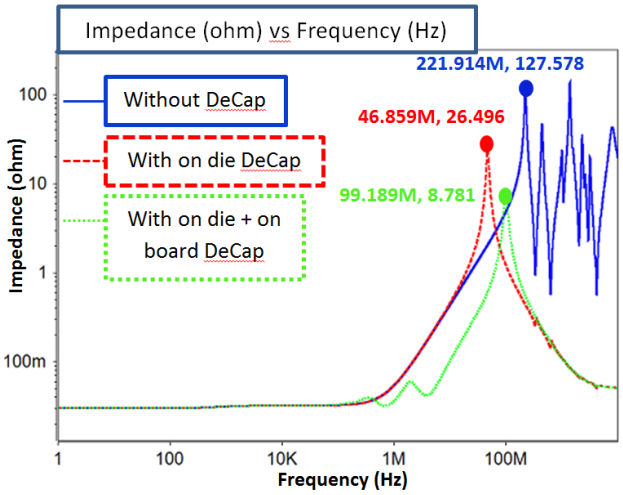

Figure 6: Impedance profile comparison between different PDN structures in decoupling capacitor connection

The impedance profile of the PDN is shown in Figure 6. The impedance profile shows comparison between a PDN without any decoupling capacitors, to PDN with 2 different stages of capacitors.

The following simulations are divided into 3 test cases; those are PDN with on die + on board decoupling capacitors, PDN with on die decoupling capacitors and PDN without any decoupling capacitor. By exciting 14 ports of the transmitter circuit at the same time, the supply voltage droop is maximized. From the supply voltage of each case, the eye diagram is captured.

Figure 7 shows the first test case, which is power supply voltage droop corresponding to PDN with on die + on board decoupling capacitors. The voltage waveform is probed on package's bump which directly connected to VCCCORE of the USB 1.05 V supply rail. The peak-to-peak supply voltage from the simulation is 37.04 mV, which is still within the target specification of the voltage droop. Figure 8 shows the eye diagram of test case 1. It is expected to pass the eye diagram since the voltage droop is still within the target specification.

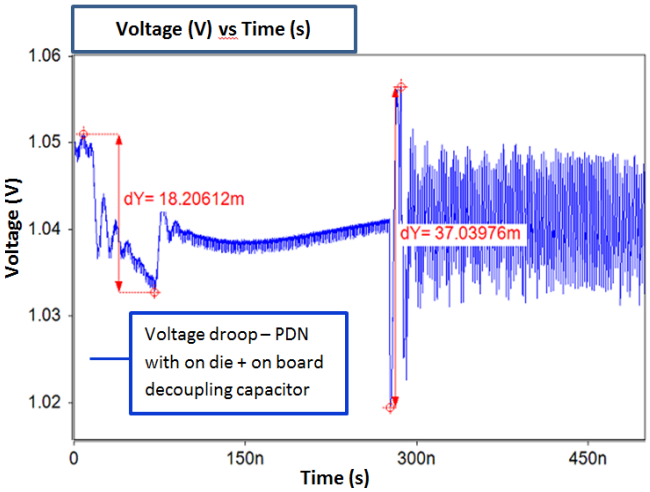

Figure 7: Supply voltage droop waveform for case 1 – PDN with on die + on board decoupling capacitors

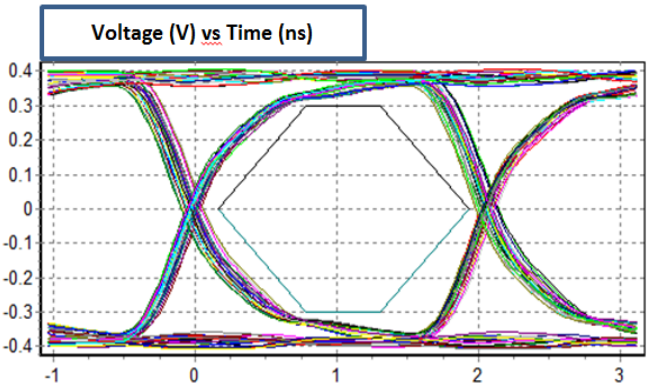

Figure 8: Eye diagram of transmitter's signal for case 1 – PDN with on die + on board decoupling capacitors

Figure 9 shows the second test case, whereby the PDN is connected with on die decoupling capacitor only without any on board decoupling capacitor. The supply voltage droop is still within the acceptable range which is 62.735

mV. The eye diagram result is passed as predicted with the passing of supply noise specification as shown in Figure 10.

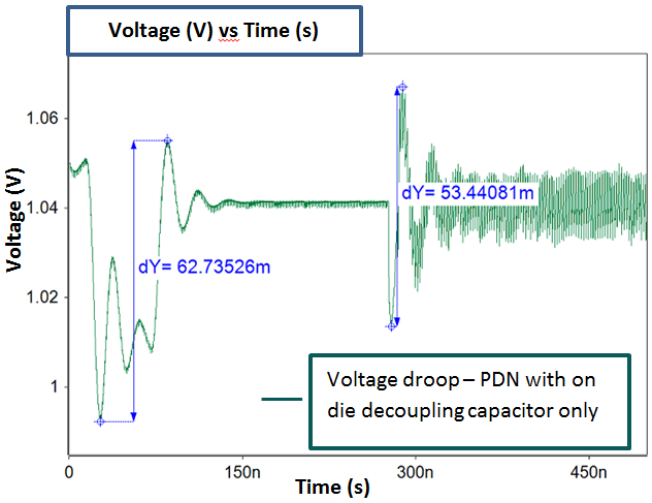

Figure 9: Supply voltage droop waveform for case 2 – PDN with on die decoupling capacitor only

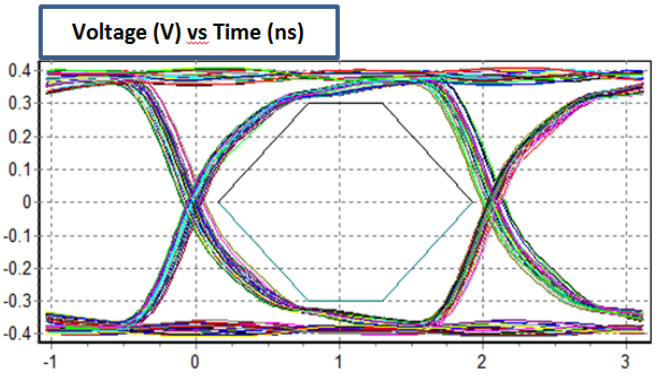

Figure 10: Eye diagram of transmitter's signal for case 2 – PDN with on die decoupling capacitor only

The interesting part of the investigation is apparent in the third case simulation result shown in Figure 11 and Figure 12. In this simulation, PDN is connected with the transmitter circuit without any decoupling capacitor. From the result, the peak-to-peak supply voltage droop (220.67 mV) is more than the allowable voltage droop in the design stages of the PDN. However, with this excessive voltage appear in VCCCORE of USB on die, the schematic eye diagram still passes the eye margin specification.

The summary of eye diagram is shown in Table 1. The transmitter connected to PDN without decoupling capacitor has the highest voltage margin (high) and voltage margin (low) on the eye mask. It also has the highest voltage opening (max) but with lowest voltage opening (min). From timing perspective, without decoupling capacitor in PDN, it will induce the highest jitter.

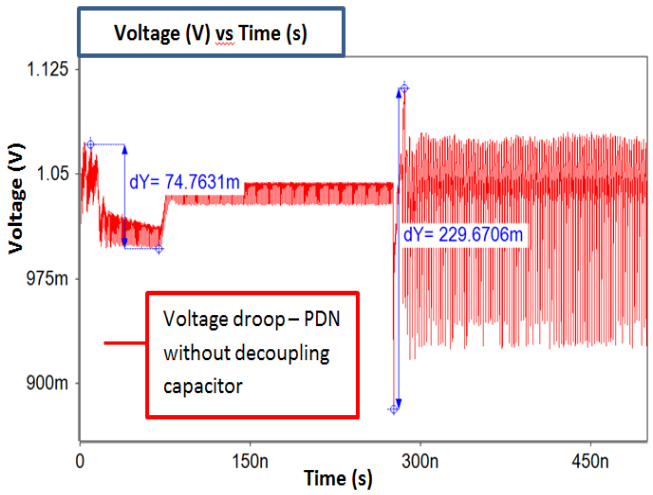

Figure 11: Supply voltage droop waveform for case 3 – PDN without any decoupling capacitor

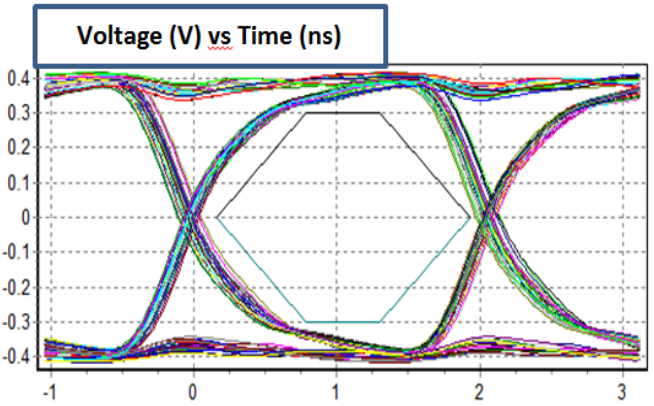

Figure 12: Eye diagram of transmitter's signal for case 3 – PDN without any decoupling capacitor

Table 1: Summary of voltage droop and eye diagram results by 3 different types of decoupling capacitor placement

Test Case	1	2	3
Decoupling Capacitor Placement	On Board + On Die	On Die	None
$V_{droop\ peak\text{-}to\text{-}peak}$ (mV)	37.040	62.735	229.670
V_{margin} (high) (mV)	16.885	17.002	23.158
V_{margin} (low) (mV)	19.548	19.407	23.432
V_{open} (min) (mV)	158.775	176.756	141.403
V_{open} (max) (mV)	719.023	718.194	750.208
Total Jitter (ps)	162.469	165.956	166.480

4. Discussions

Different I/O interfaces will have different peak-to-peak supply voltage droop design target. The target voltage droop may vary within a range of numbers depending on the transistor circuit design and its sensitivity. Additionally, the change in silicon process may also scale down the targeted voltage droops.

In order to reduce the power supply noise, effort is done towards package and motherboard routing, stacking and also vias, as to reduce the resistive and inductive elements on the PDN path. The noise induced in PDN is mainly because of total resistance (R_{total}) and total inductance (L_{total}) introduced by the formula:

$$V_{drop} = I_{total}R_{total} + L_{total}\,(dI_{total}/dt)$$

Where I_{total} = total current drawn by the circuit, t = time

Other than that, decoupling capacitors are one of the main components to be added to reduce the total impedance as shown in impedance profile at Figure 6. By adding decoupling capacitor into the PDN, the peak resonance frequency of impedance profile will change to different amplitude and different frequency. All these efforts serve the same purpose, which are trying to reduce the voltage drop happening in circuit because of the current going through the inductive and resistive elements.

From the simulation, it is clear that voltage droop design target is not the only indication, nor the absolute parameter to quantify a failure on a high speed I/O interface. Results also indicate that although the peak-to-peak voltage droop is much higher than the targeted PDN design, the transmitter eye diagram still passes the specification. From the result in Table 1, signal without decoupling capacitor has the highest voltage margin as compared to those signals with decoupling capacitors. Without decoupling capacitor, jitter numbers are higher and this should be addressed. In this scenario, it proves that the USB transmitter circuit can actually sustain higher supply noise drop, hence leading to the observation that power delivery noise design needs to include more than just the power delivery network simulation.

However, this paper studies on the self-noise created by all the 14 ports of USB transmitters at the same power rail only. The coupling-noise from other circuit such as receivers, PLL, and clock circuits are not included in the simulation. Thus, the voltage droop waveform can't represent the total voltage droop without the existing of decoupling capacitors. It is mainly to bring up the issue that even the supply voltage droop is more at certain level, it may not necessary to cause the circuit to fail (As shown in Figure 12).

In the other note, validation over real measurements is also not done due to hardware limitations. With stronger prove and further justification in future, a chip with modified structure in term of decoupling capacitors can be taped out as to prove the analysis observed from this simulation research.

5. Conclusion

It is important to know the correlation between PDN and circuit performance. Previous method in designing PDN is based on voltage droop design target without connecting both together. This paper has shown that when 14 ports of transmitters are switching at the same time, the PDN without decoupling capacitors will cause a large peak-to-peak voltage droop (229.67 mV). However, this large voltage droop is not causing the eye diagram to fail the eye mask's specification.

By this initial research, it is shown that supply voltage noise more than the target specification is not necessary to cause the failure to the I/O circuit. This is justified by the result of the eye diagram as shown in Figure 12. This circumstance might be due to USB sensitivity to noise at different frequency which requires further proves and researches in the future.

In addition, impact of PDN model to transistor circuits should be included in future design. Conventional way of designing PDN just by using target voltage droop should be improved by including the PDN impact to transistor circuit. Without connecting them during design stage, overdesign may easily happen. Further investigation especially on power delivery design with die capacitor impact to coupling noise and the coupling noise impact to transistor circuit is remained to be explored. This will be the next research study in the near future.

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