The Signal Integrity Analysis of Differential Signal Based on HyperLynx

Guanzhong Ren[1] Runjing Zhou[2]
College of Electronic Information Engineering
Inner Mongolia University
Hohhot, China
[1]e-mail: qrenlele@163.com
[2]e-mail: auzhourj@163.com

***Abstract*—In the design of high-speed digital circuit, the transmission of digital signal by the differential pair can solve signal integrity issues effectively. Making use of an actual PCB, its signal integrity and "eye diagram" performances were simulated by the HyperLynx software. The high-frequency performance of the PCB was improved, and the potential signal integrity problems were settled. It is proved that depending on the impedance controlling and matching, the differential pair can make the signal transmission more stable.**

Keywords-differential signal; signal integrity; simulation

I. INTRODUCTION

Technological progress makes the signal transmission rate continuously double. Relying on the advantages of strong anti-interference and easy to match, the differential signal transmission has been applied more and more in high-speed digital circuits. In the design of high-speed PCB, the differential transmission of digital signal can increase the speed of signal effectively, reduce the power consumption, and improve the signal integrity. However, the verification of signal integrity on the completed PCB is not only costly, but also extremely delays the progress of the entire project. Researching, finding out and getting rid of the potential signal integrity issues, or depressing their influence when the circuit is being designed, then the unnecessary time and money will be saved.

II. DIFFERENTIAL SIGNAL DIFFERENTIAL IMPEDANCE AND ROUTING RULES

A. Differential Signal

Differential signal is the method that uses two lines to transmit the digital data. Driving by two completely complementary signal lines, it can avoid the noise interference well and increase the Signal-to-Noise Ratio (SNR). When the signals are transmitted down, one line is positive, and the other is negative. Thus, at the receiver the signal can be extracted from the difference between the two lines. This method is considered to be superior to single-ended signal transmission——the reference voltage is ground, and it will change in the long distance transmission. Generally, differential transmission makes the external radiation affect the two lines at the same location, and the noisy can be detected more easily.

Differential signal transmission of data is of obvious advantages. (1)The reference voltage is under control, so weak signals can be identified easily. (2)The interference source makes an impact on each of the differential line almost at the same degree. Therefore, the differential lines are almost immune to external electromagnetic interference (EMI). (3)In the single power supply system, bipolar signal processing will be exactly and easily.

B. Differential Impedance

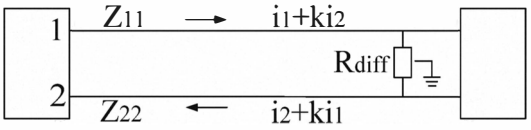

Figure 1. Differential impedance

The usual form of differential termination is shown in Fig. 1. The characteristic impedance of Line 1 is Z_{11}, current is i_1. Likewise, the characteristic impedance of Line 2 is Z_{22}, and current is i_2. The currents on the two lines are coupled to the other one respectively by the coupling constants k_1 and k_2. Then, the voltages on each line are:

$$\begin{cases} v_1 = Z_{11}i_1 + Z_{11}k_2i_2 \\ v_2 = Z_{22}i_2 + Z_{22}k_1i_1 \end{cases} \quad (1)$$

As the two lines are very close to each other, and their attributes are equal, so $k_1 = k_2 = k$, $Z_{11} = Z_{22} = Z_0$, and $i_2 = -i_1$. By Ohm's low, the differential impedance is:

$$Z_{diff} = 2\,v_1/i_1 = 2Z_0i_1(1-k) \quad (2)$$

It can be seen clearly that differential impedance is smaller than two times of the impedance of a single line.

C. Routing Rules of Differential Pair

When the circuit diagram is completed, the topology of the differential pair can be modeled in HyperLynx before routing. There are very strict requirements for the routing of the differential pair. The general rules for the routing of the differential pair are: (1) The two lines should be as close as possible. (2) The length of the two lines must be equal. The consistency of differential impedance requires that the width of each line and the separation between the lines are kept invariant. And to prevent the impedance discontinuities, vias and polygonal lines should be used as few as possible. In addition, a complete ground plane can be used to decrease the signal distortion.

III. SIMULATION

HyperLynx produced by the Mentor Graphics Corporation supports the simulation before and after the layout and routing. Calculating the differential impedance

978-1-4244-7956-6/10/$26.00 ©2010 IEEE

by the software can avoid a complex process, and get a more efficient and accurate result. Compared with the high cost of the EMI testing, HyperLynx can find out the EMI hidden troubles when the circuits are designed, and give the designer recommendations for improvement.

A. Pre-layout Simulation

The drivers are DOUT3+ and DOUT3- (pin 10 and pin 11), which are the signal ports of DS90LV031ATM, and the receivers are RINA+ and RINA- (pin 1 and pin 2), which are the signal ports of DS90LV032ATM. They are interconnected by the straight line that contains four vias, and swap the layers two times, as shown in Fig. 2.

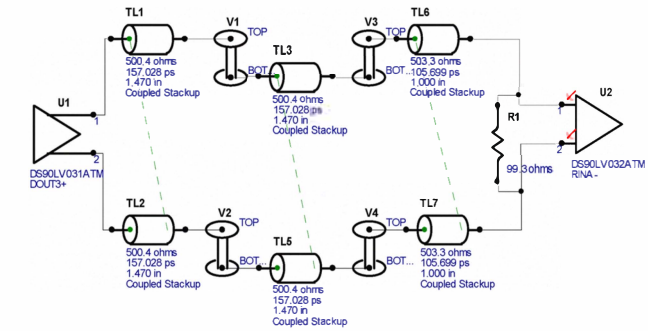

Figure 2. Topology of the differential pair

The transmission lines are coupled microstrip lines, and the differential termination is R1 which connects the positive and negative lines. Generally, the structure of stackup, substrate thickness, width of the line, and the separation are set in order to control the characteristic impedance of the differential pair to about 100ohm. In the Fig. 2, the substrate thickness is 10mil, trace thickness is 0.5mil, trace length is 3.940in, and a pair of the vias locates at 1.470in, the other pair locates at 2.940in, the drill diameter of the vias is 18mil, and pad size is 20mil. The relationship between trace width and separation when the differential impedance is 100ohm is shown in Fig. 3. One set of the reasonable data is 10mil in width and 7mil in separation. Thus the differential impedance is 101.4ohm, and the differential termination is set to this value.

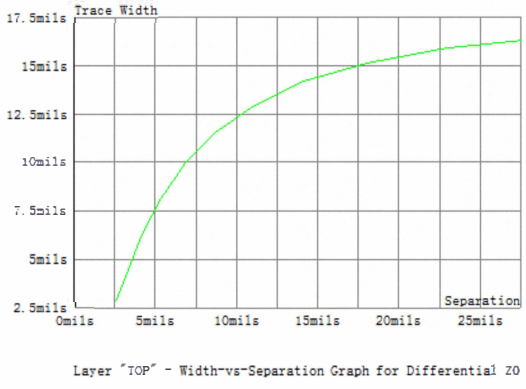

Figure 3. Relationship between trace width and separation

Test the performance of the circuit, the result of signal integrity analysis at the receiver is shown in Fig. 4. The result of eye diagram analysis is shown in Fig. 5. The eye diagram is made by pseudo random binary sequence, of which the length is 127, the bit interval is 3.759ns, and random jitter is 5% of the interval. The parameters are shown as Table I.

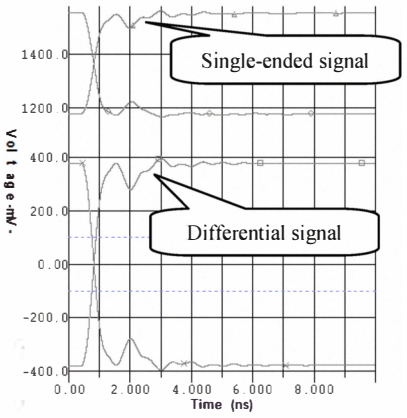

Figure 4. Rising time=351.652ps, overshoot=18.42mV

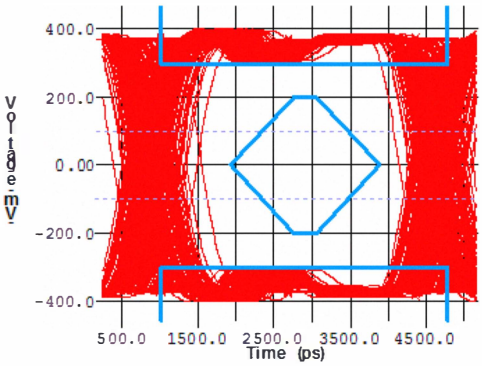

Figure 5. Eye diagram of pre-layout simulation

TABLE I. KEY PARAMETERS

Eye Width	Eye Height at 0.5UI	Zero-crossing distortion	Noise Margin
2.598ns	628.5mV	1.2032ns	286.26mV

The eye mask in the diagram is STAT1_TX. The "open eye" illustrates that the bit error rate (BER) is low, and the system works properly.

B. Post-layout Simulation

As the routing has completed, post-simulation can get more accurate analysis data than that of pre-simulation. The routing can apply the parameters in the pre-simulation, shown as Fig. 6. UDRV1 is DS90LV031, and URCV2 is DS90LV032.

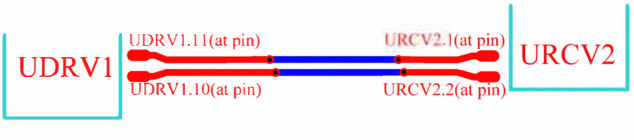

Figure 6. Routing of the differential pair

The result of signal integrity simulation at receiver is shown in Fig. 7. The eye diagram under the same conditions is shown in Fig. 8, and its parameters are shown as Table II.

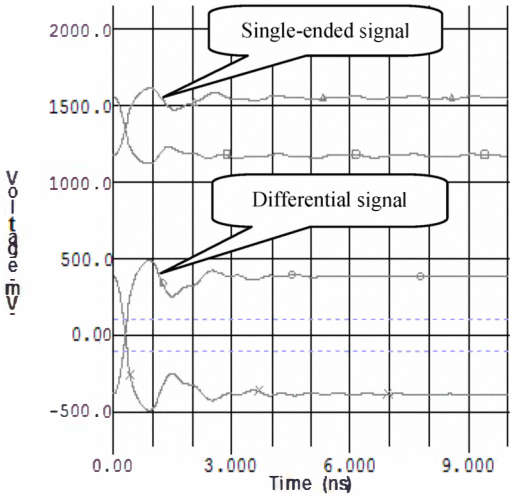

Figure 7. Rising time=334.904ps, overshoot=86.89mV

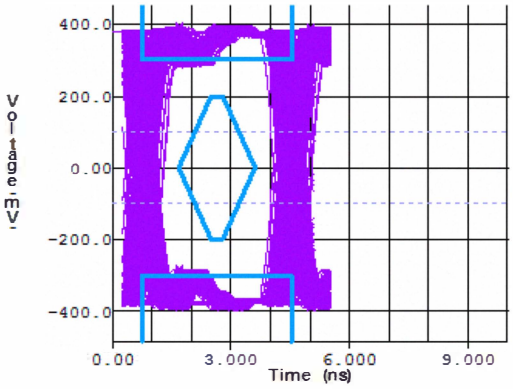

Figure 8. Eye diagram of post-layout simulation

TABLE II. KEY PARAMETERS

Eye Width	Eye Height at 0.5UI	Zero-crossing distortion	Noise Margin
2.325ns	601.9mV	1.2212ns	266.60mV

The overshoot and ringing both are large. Fig. 9 shows the eye diagram of which the bit interval is 0.7ns. Its parameters are shown as Table III.

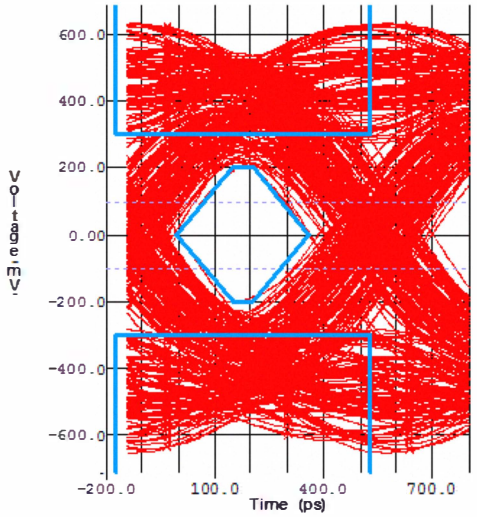

Figure 9. Eye diagram at a high frequency

TABLE III. KEY PARAMETERS

Eye Width	Eye Height at 0.5UI	Zero-crossing distortion	Noise Margin
358.440ps	404.3mV	342.63ps	209.76mV

It is clear that the zero-crossing distortion is larger and the noise margin is smaller. The "double eyelids" shows the crosstalk between the traces. Adjust the traces. In allusion to the vias that must be used, their equivalent impedance are usually lower than that of the transmission line by 12%. They are the spots where the impedance is discontinuous. However, reference [1] proposed that the reflection made by vias was very little, and the reflection coefficient was about -0.06. The major effects of vias are on the power distribution net and prolonging the rising time.

For the transmission line is short, the effect of the dissipation coefficient of the substrate is small on the eye diagram. The main factors that affect the performance are the trace width and the consistency of routing. Wider trace can help depress the influence of the "skin effect", so the eye diagram will be improved. According to the width-separation curve, the width and separation are both set to 12mil. Then the characteristic impedance of a single line is 69.6ohm, and the differential impedance is 100.2ohm. The value of terminal resistor is set to 100ohm. The drill diameter of vias is set to 15mil, and pad size is set to 20mil. A smaller via is conducive to reducing the reflection. If possible, thinning the PCB or shortening the distance between the pins and the vias are useful as well.

The results are shown in Fig. 10 and Table IV.

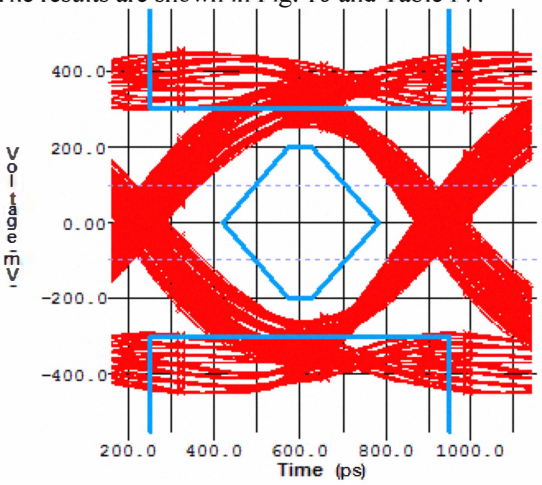

Figure 10. Improved eye diagram at the high frequency

TABLE IV. KEY PARAMETERS

Eye Width	Eye Height at 0.5UI	Zero-crossing distortion	Noise Margin
484.787ps	552.4mV	191.04ps	270.31mV

And the result of signal integrity simulation at the receiver is shown in Fig. 11.

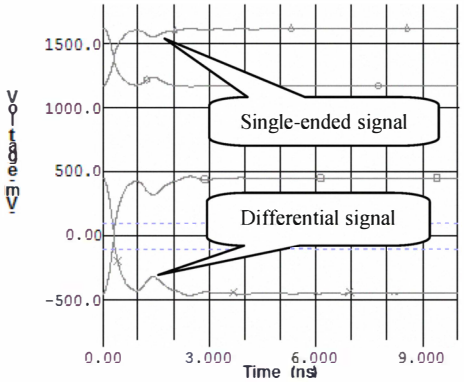

Figure 11. Rising time=327.873ps, overshoot=19.68mV

The overshoot is reduced by 67.21mV, the average rising time is reduced by 7.031ps, and the ringing is reduced at the same time.

IV. CONCLUSION

Compared with traditional methods that the topology, stackup, and routing are fixed by the experience of designers, and the relational tests are processed after the PCB has been manufactured, the simulation tool—— HyperLynx can be used to analyze the performances of specified nets, and the hidden troubles can be corrected directly. Meanwhile the design rules are optimized in time, and the transmission quality of the signals can be guaranteed. The practice proves that the circuits work well, and the design efficiency is improved.

REFERENCES

[1] Li Wen-bin, Yan Xue-long. Simulation Analysis of Via in High-speed PCB [J]. Mechanical Engineering & Automation, No.1. 2010, pp.57~59.

[2] Wang Liang, Zhou Runjing. Analysis of Singal Integrity Based on SPECCTRA Quest [J]. Conference Proceedings of the Seventh International Conference on Electronic Measurement & Instrument, 2005, Vol.6, pp.6-211~6-214.

[3] ZHANG Ge-zi,,JIN Li-hua. Simulation and analysis of high-speed differential via [J]. Information Technology, No.5. 2007, pp.99~101.