A Comprehensive Signal Integrity Study of Differential Pairs Routed within a PCB Via Field

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Abstract— **Printed circuit board (PCB) via fields can cause signal integrity (SI) degradation to high speed bus channel PCB wiring in the form of: differential to common mode conversion, crosstalk and impedance mismatch. This is especially the case when differential pairs are close to via anti-pads, when trying to manage multiple differential pairs in between two vias which are tightly pitched from each other and/or when PCB layer misregistration is considered. An electromagnetic modelling study is carried out in this paper where two differential pairs are wired in between two columns of vias. Different design parameters are varied including the pitch between the two via columns, the spacing between the differential pairs and the number of vias in the column. Observations are made based on the presented results furthering the understanding of the phenomena that takes place and towards better PCB design implementations.**

I. Introduction

High speed bus channel sections are required to ensure good SI in order to transfer and decipher data from one end of the channel to another efficiently and accurately. This requirement is becoming more and more critical as data rates increase and previously inconsequential channel design details become important [1]. High speed bus channels are typically composed of multiple sections within a PCB including: (1) open area wires to carry signals within the same PCB layer in regions which are not space-limited or noisy, (2) PCB vias which are utilized to transition signals between PCB layers and (3) pin area wires to carry signals within the same PCB layer through a noisy pin/via region due to the presence of close-by aggressors in tight wiring channels. Additionally, cables and connectors can exist within the high speed bus channel to transition between different PCBs or simply within one PCB to increase reach (as with the cable scenario).

Of interest in this paper, is the differential strip-line wiring within a PCB via field. Wiring in a PCB via field is typically done when wiring in/out of module package components and connectors or through voltage regulators, etc. Such wiring, though un-preferred, may be unavoidable in many cases. Differential wiring in a via field can encounter impedance mismatch due to the need to neck down wiring sometimes or due to an asymmetric wiring environment. Also due to asymmetry, differential wiring may experience differential to common conversion. Additionally, significant amounts of crosstalk typically aggress on a differential pair in a via field either from other closely spaced differential pairs within the same layer or from differential pairs on other layers through via anti-pads.

In designing high speed channels, wiring through sensitive PCB regions like via fields needs to be planned to minimize the SI degradation [2]. To quantify the degradation amount given a particular scenario, electromagnetic modelling is generally carried out. Pertaining to via fields different factors need to be examined in order to arrive at the optimal solution. Such factors include: (1) the closest via pitches as these determine the width of the wiring channel and thus affect the proximity of the differential pair to the via anti-pad, (2) the number of vias which a differential pair will be wired by, (3) the number of differential pairs within a particular channel and (4) the pair to pair spacing between differential pairs within a wiring channel (if multiple differential pairs exist within a wiring channel) versus the pair to anti-pad edge spacing. Improving the conditions for better SI in one factor might degrade conditions for other factors and thus not yield better SI. Consequently, the matrix of sensitivities needs to be understood to make well informed design decisions. An electromagnetic modelling sensitivity study is carried out in this paper. The study considers differential wiring within a via field varying different wiring conditions. The following sections in this paper cover the modelling setup and parameters, SI simulation results and observations/discussion.

II. Modelling of Differential Striplines in Via Fields

Fig. 1(a) shows a simplified diagram of the setup that was considered for the analysis carried out in this work. As can be seen, part of the wiring in the 1 inch channel passes through the via field region. The number of vias on the side was varied between 0 and 10. Three trace layers were modelled within the via field. A top view of a single section of the differential wiring that passes through a single wiring layer within the via field is shown in Fig. 1(b), where the diameter of the anti-pad (D), the via drill diameter (d), the trace width (W), the via pitch (A), the in-pair spacing (InP) and pair to pair spacing (P2P) are noted. The differential stripline studied in this work was designed for 85 Ohms with the dimensions listed in Table. 1. The differential striplines were designed for a dielectric material having ε_r=3.5 and tan_δ=0.005 @1GHz, dielectric thickness of 9mils between the ground planes and a 1.2mil trace thickness with a vertical spacing from the bottom edge of the trace to the ground layer below of 4 mils. As the goal of this work was to evaluate the sensitivity of the striplines passing through the via regions, the via pitch (A) and the pair to pair spacing (P2P) were varied to reflect possible wiring dimensions in a multilayer PCB environment. The lower half of the Table. 1 shows the dimensions varied. It can be seen that

a total of 16 variations were considered for a single section of the via region.

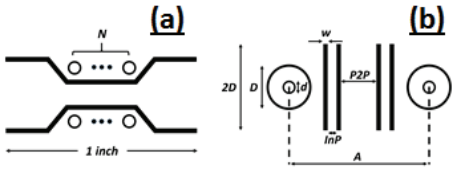

Fig. 1. (a) Analysis setup considered for this study. Two differential pairs pass through via field region. (Each black line represents a differential pair); (b) Top view of a single section of the differential wiring in via field region.

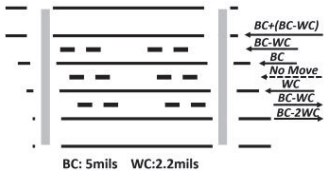

Fig. 2. Cross-sectional view of a single section of PCB structure with 6 differential striplines adjacent to vias. Layer misregistration values are also shown.

TABLE I
PARAMETERS OF A SINGLE VIA SECTION

Parameters	Values (mil)
D	28
d	10
w	3.3
InP	5.2
Varied Pitch (mil)	Varied Pair to Pair Spacing (mil)
A=60	$P2P$=4, 5.2, 7, 9
A=65	$P2P$=4, 7, 10.2, 12, 14
A=70.7	$P2P$=4, 7, 10, 13, 15.9, 18, 20

Table.1. Parameters of a single via field wiring section.

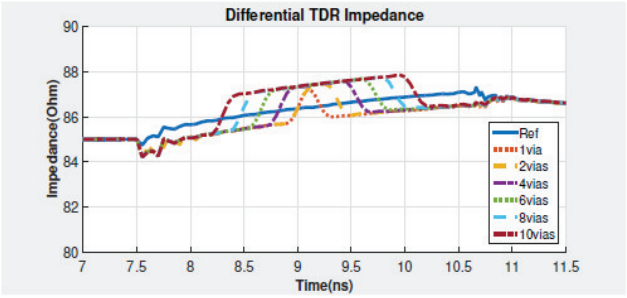

Fig. 3. Differential impedance of a 1 inch channel with different number of the via sections cascaded (A=65mils, P2P=7mils).

Fig. 2 shows the cross-sectional view of the stripline model considered for this work. Six differential stripline pairs were distributed amongst three signal layers (two pairs per layer). Two vias were placed on each side of the two differential pairs along with their antipads. PCB layer misregistration was considered in the modelling to cover worst case SI conditions. Due to signal and ground layer misalignment, misregistration may drive more layer to layer crosstalk, differential to common mode conversion and impedance mismatch. The layer misalignments considered for this study are shown in Fig. 2. The differential pair in the middle layer closest to the via antipad edge was chosen as the analysis victim pair to cover the worst case scenario.

Stripline models in the open area with 20mil pair to pair spacing and with no via exposure were also generated with similar dimensions. To form the channel shown in Fig. 1(a), combinations of this model and the via section models were cascaded to form a 1 inch channel. In this work, the number of via sections (N) were chosen to vary between 0, 1, 2, 4, 6, 8 and 10. The channel with 0 via sections is the baseline reference for comparison as it represents the optimal scenario. As a result of having 7 different via section options and 16 total via pitch/pair to pair spacing combinations, a total of 97 1inch channel cases (represented by Fig. 1(a)) were generated and analyzed in this study.

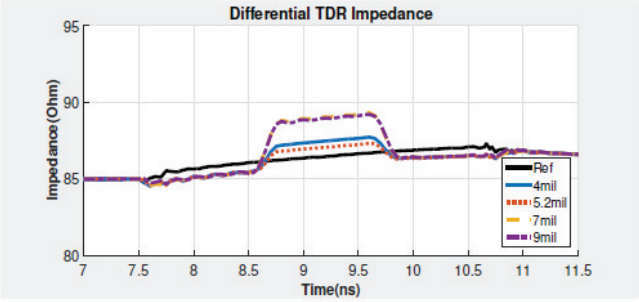

Fig. 4. Differential impedance of a 1 inch channel under various pair to pair spacing with 6 via sections cascaded (A=60mils).

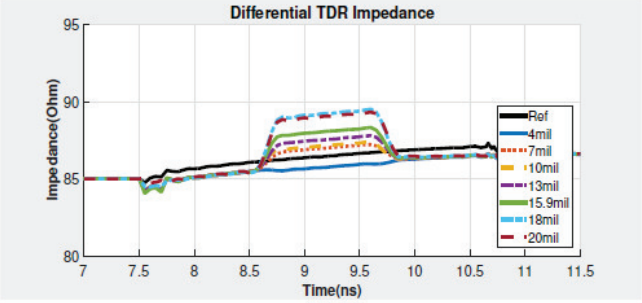

Fig. 5. Differential impedance of a 1 inch channel under various pair to pair spacing with 6 via sections cascaded (A=70.7mils).

III. SIMULATION ANALYSIS

For each of the aforementioned 97 cases, the differential impedance of the victim was studied. Fig. 3 shows the differential impedance of 1 inch channels cascaded with various number of via sections that have a pitch of 65 mils and pair to pair spacing of 7 mils. As can be seen, an inductive impedance mismatch appears as via sections are included in the channel. With more via sections in the channel, expectedly a longer delay impedance mismatch is observed. It is also clear that the reference scenario, with no via field wiring, shows no impedance mismatch. Figures 4 and 5 show the differential impedance of the channel for different pair to pair spacings with via pitches 60 and 70.7 mils respectively. It can be noticed that, in general, the differential impedance mismatch increases as the pair to pair spacing increases. This can be alluded to the fact that as the pair to pair spacing increases, the victim pair is closer to the antipad. This causes the reduction of the differential pair environment symmetry and less ground coverage driving a decrease in capacitance. Worthy to note is that for the largest pair to pair spacings, the differential

impedances observed get closer to each other. This may be explained by the fact that as the differential pair gets lesser ground coverage as a whole, the differential pair environment asymmetry decreases. Also worthy to note is that the least pair to pair spacing in both figures 4 and 5, does not yield the lowest impedance mismatch compared to the reference scenario. The lowest impedance mismatch is shown for the second lowest pair to pair spacing of 7mil. The reason for that is most likely due to victim pair environment assymtery generated by the proximity from the other pair even though the victim pair is furthest from the antipad edge. Additionally, to demonstrate the impact of a tight via pitch on the channel impedance, one can compare the results in figures 4 and 5 having 7 mils pair to pair spacing. As seen in these cases, the differential impedance increases as the pitch goes down to 60 mils. The 70.7 mil pitch channel had an impedance closer to 85 Ohms (reference case) compared to the other channels.

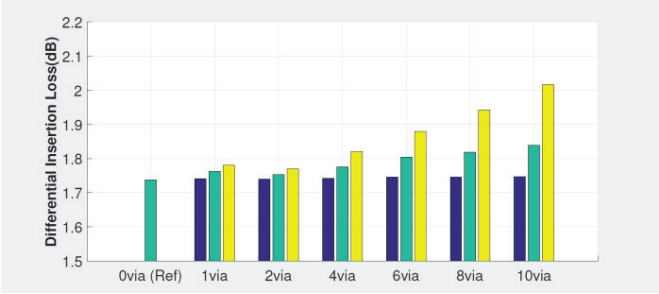

Fig. 6. Summary of the differential insertion loss for the 97 cases.

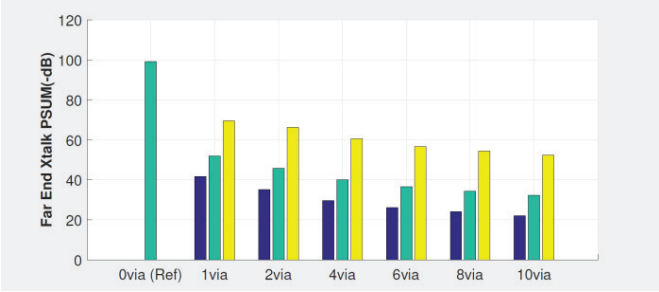

Fig. 7. Summary of the power sum crosstalk for the 97 cases.

To further investigate the impact from the via region with respect to the via pitch and the pair to pair spacing, a statistical analysis of the 97 cases in frequency domain was carried out. The data is shown as bar plots at 16 GHz (nyquist frequency for 32Gb/s baud rate) in figures 6, 7 and 8. Each bar plot has a reference value which is taken from the cascaded 1 inch channel without any via sections. Each plot contains 6 groups (number of via section in channel) with each group showing the absolute value of the minimum, the maximum, and the scenario which is the value closest to the average of the 16 data points. Looking at the insertion loss in Fig. 6, the reference channel has an insertion loss of 1.74 dB. The minimum loss from all groups is almost equal to the reference case insertion loss. It is worthy to note that the minimum for all groups was found from channels that had maximum via pitch of 70.7 mils and a pair to pair spacing of 7 mils. The maximum insertion loss in each group increases as the number of via sections in the 1inch channel increases going from 1.78dB to over 2dB. The maximum insertion losses for 5 out of 6 groups are found from the channels with via pitch of 65 mils and pair to pair spacing of 14 mils. This corresponds to one of the scenarios having some of the most victim to antipad interaction and as a result maximum impedance mismatch.

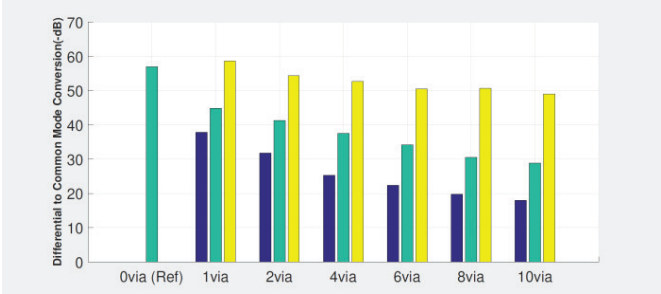

Fig. 8. Summary of the differential to common model conversion for 97 cases.

Figures 7 and 8 show the statistical results of the power sum of cross talk and the differential to common mode conversion respectively. Clearly, in Fig. 7, both of the minimum and the maximum crosstalk values within each group increases as the number of the cascaded vias increases. Furthermore, the channels which produced the worst crosstalk levels that is shown as the shorter bar in each group all have a via pitch of 70.7 mils and pair to pair spacing of 20 mils, while the best cases all have a via pitch of 70.7 mils and pair to pair spacing of 7 mils. The worst cases fall within the cases which have most victim pair to antipad interaction, while the best cases fall within the cases furthest from the antipad but not the closest to the other differential pair. Similar best case/worst case behavior can also be observed from Fig. 8 for differential to common mode conversion. From the results in this section, it is shown that when wiring in via fields it is preferred to be within the largest via pitch, far from the antipad while still not too close to the other pair on the same layer. It is also shown that less via field wiring length is preferred if needed to wire through via fields.

IV. Conclusion & Future Work

The SI sensitivities of the differential striplines passing through via regions were investigated in this work. Different wiring scenarios were analyzed considering factors which matter for differential wiring in via fields. It was found that wiring through via fields can have significant impact on SI if not properly designed/anticipated for. Future work will study the available data further to make more deductions in addition to studying full channel effect of the generated models in time domain simulations.

References

[1] E. Bogatin. *Signal integrity: simplified*. Upper Saddle River, NJ: Prentice Hall Profession, 2004.

[2] R. Bates. "Speed Electrical Transmission Line Design and Characterization," presented at Topical Workshop on Electrictronics For Particle Physics, Karlsruhe Institute of Technology, Germany, September, 2016.