Signal Integrity for USB 3.1 Gen 2 Front End Challenging Loss Budget

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***Abstract*—This works presents rigorous full-wave modeling efforts to meet the design challenges and tight loss budget allowed for protocol analyzer intended for USB 3.1 Gen 2.0 operating at 10 Gbps. The design cycle starts from the basic foundation of building a robust stackup for high quality signal integrity for high speed applications using ANSYS HFSS. The models do include the actual manufacturing design parameters and constrains of fab house. This is very imperative to guarantee a properly working first prototype and to eliminate the hassle of several prototype iterations. Impedance, losses, via transition, discontinuities, cross talk, and layout routing are all optimized to meet the challenging requirements of front end loss budget for USB protocol analyzer. Experimental measurements are presented to validate the simulation results**

***Keywords*—HFSS; full-wave; signal integrity; SuperSpeed 10Gbps; Type C connector; USB 3.1 Gen 2.0**

I. Introduction

The trend of communication protocols is the increase of speed from one generation to the next. This requires attentive focus on accurate modeling of interconnect, vias, and discontinuities in the passage of high-speed data of the RF front end. Moreover, the competitive industrial environment is pushing for fast release of product. This means that there is no much room of tolerance for a product re-spins. It should work from the first prototyping. From very early stages of design, the signal integrity engineer is challenged to devise a systematic methodology for rigorous full-wave modeling on a system level in frequency domain to assess the return loss, insertion loss, near cross talk, and far cross talk. Time domain analysis is also valuable to determine the quality of eye parameters such as eye width, eye height, bit error rate, and jitter.

Recently, the USB promoter group introduced the next generation doubling the speed to 10 Gbps [1]. Quickly after that they introduced a universal type-C connector that plugs in either direction [2]. Associated with that is the constrained loss budget [3] allocated to host, device and cable assembly as shown in Fig. 1. In this work, we present successful steps for designing the RF front end protocol analyzer of USB 3.1 Gen 2.0 (10 Gbps) implementing the newly introduced type C connector for USB applications and complying with the allowed loss budget. The purpose of the USB analyzer is to examine the performance and assess traffic errors; signal tapping is active; and tapped signals are a partial replica of the actual traffic. From testing and analyzing point of view, the probing has to be designed to not perturb the link between host and device.

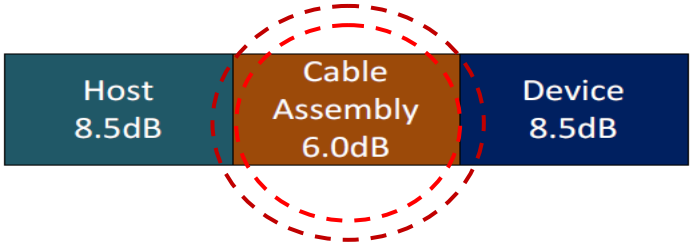

Fig. 1. Loss budget for USB Gen 2.0 super speed using C connector

II. USB Analyzer Front End Challenge

A. Problem Description

Per specs, the allowed loss budget of cable assembly for USB 3.1 Gen 2.0 (SuperSpeed 10 Gbps) is 6.0 dB and the remainder of allocated power loss budget is divided equally between host and device as shown in Fig. 1. The analyzer is considered part of the cable assembly as illustrated in Fig. 2. This figure shows signal path from host to device or vice versa through analyzer where the tapped signal goes to FPGA for protocol analysis purposes. The signal travels through receptacle/plug connector on the host and device, cable from host to analyzer, cable from analyzer to device. For a total cable length of 0.6 m between host and device including the mated connectors on each side, the loss budget is quite close to 6.0 dB compliant with specs requirements. This leaves almost 0 dB as loss budget for analyzer added in between host and device path. In other words, the extra path that the signal undergoes within the analyzer should have insertion loss of 0 dB.

B. Front End Full-Wave Modeling Efforts

The design process starts with the full-wave modeling of microstrip and stripline impedances based on the actual stackup parameters and material properties. Via transition and discontinuities are optimized. For example, the proximity effect of connector enclosure on the microstrip differential impedance shown in Fig. 3 is modeled using ANSYS HFSS [4]. The impedance with connector shield in close proximity

should be considered as this will lead to a different impedance value if not modeled properly. Moreover, the effect of high-speed trace coating is analyzed for optimum performance [5]. The tapping circuit is optimized to introduce the minimal loss while maintaining signal integrity parameters such as return loss better than 20 dB up to 5 GHz, minimal insertion loss and crosstalk. The approach adopted in modeling the RF front end is to be divided into subsections; model each subsection individually; and cascade all the pieces together to get the S-parameters of the entire RF path. More results, stackup parameters, and material properties will be discussed during presentation.

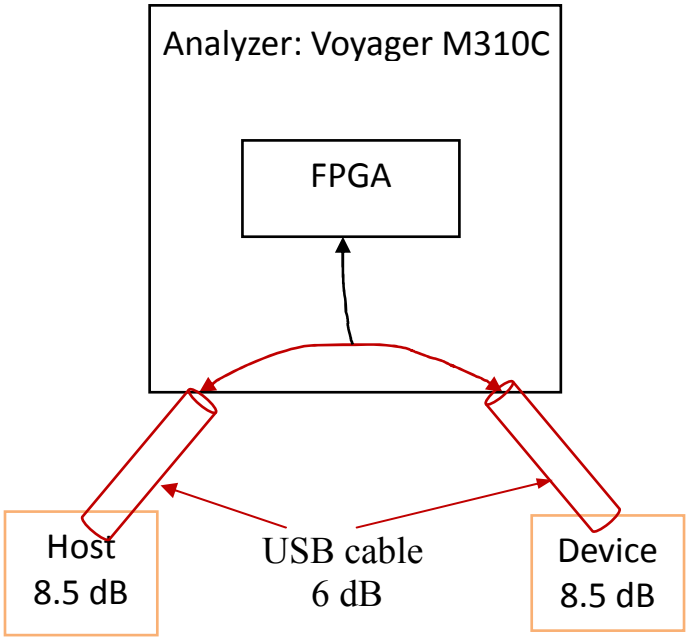

Fig. 2. Cartoon showing USB analyzer inserted between host and device through USB cables. Not to scale.

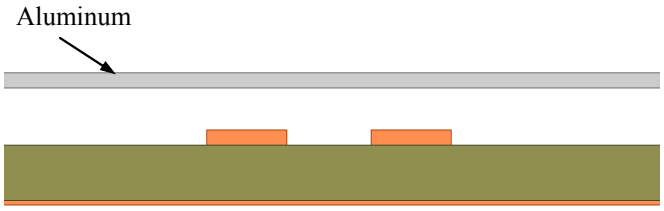

Fig. 3. HFSS model to study effect of USB C-connector enclosure on microstrip differential impedance. Aluminum sheet represents the bottom of USB connector enclosure.

III. Measurements and Testing

The setup to test the electrical performance of the USB analyzer is shown in Fig. 4. It consists of the USB analyzer, two 0.3 m cables with C connectors (plug) that mate with the C connectors (receptacle) at the front end of the USB analyzer, and adapter boards (designed in-house for the purpose of measurements). The adapter board has C connector (receptacle) on one end that mates with the cable plug C connector and SMA connector on the other side to connect to vector network analyzer for frequency measurements or to real time scope for time domain measurements. Variation of insertion loss versus frequency shown in Fig. 5 indicates that the loss at 5 GHz (Nyquist frequency) is compliant to specs requirements. Return loss measurements versus frequency are shown in Fig. 6. The measured return loss is below 10 dB up to the Nyquist frequency of 5 GHz. The eye diagrams shown in Fig. 7 and Fig. 8 are in agreement with the frequency domain results. The required CTLE of 5 dB giving a quite wide open eye is to compensate for the insertion loss of 5 dB at the Nyquist frequency of 10 Gbps speed.

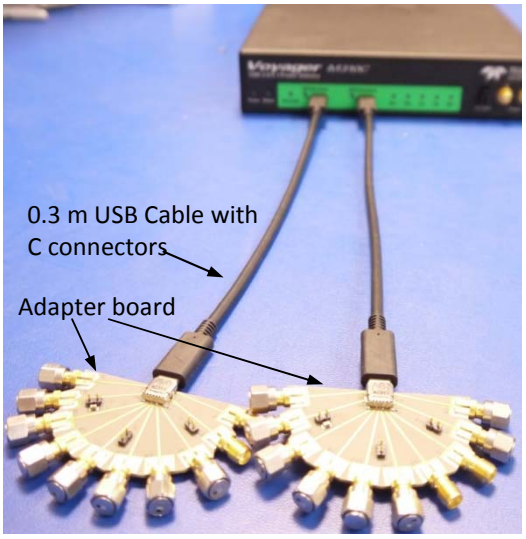

Fig. 4. Measurement setup for frequency and time domains to assess the performance of built USB analyzer.

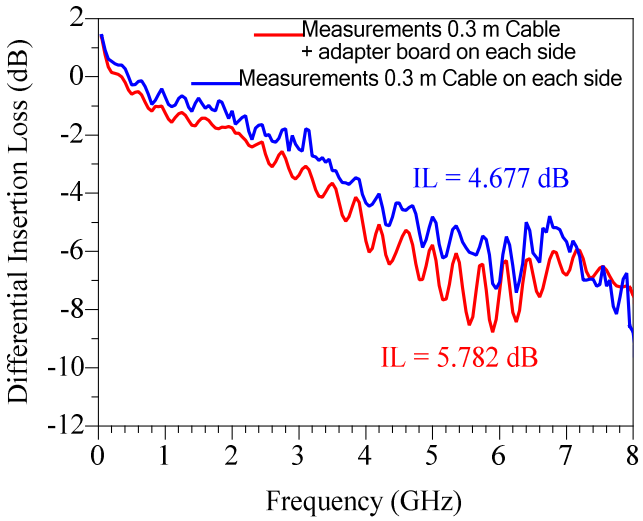

Fig. 5. Measured insertion loss versus frequency with and without adapter board

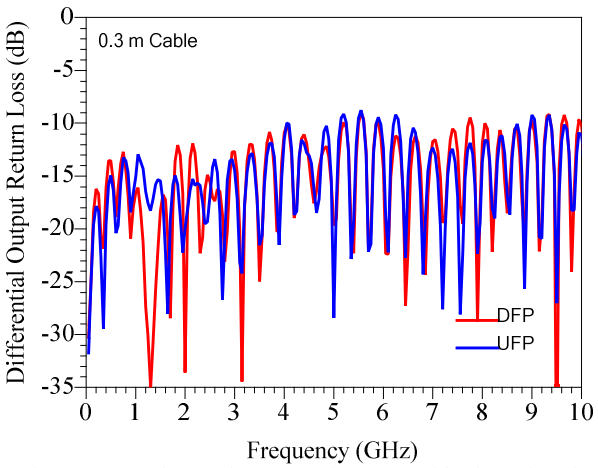

Fig. 6. Measured return loss versus frequency with adapter board

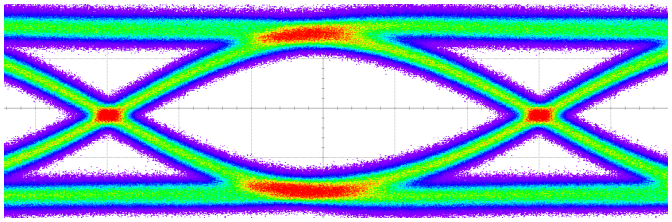

Fig. 7. Measured eye diagram for the signal path from downstream facing port (DFP) to upstream facing port (UFP): applied CTLE = 5 dB, eye height = 431.7 mV, eye width = 83.6 ps.

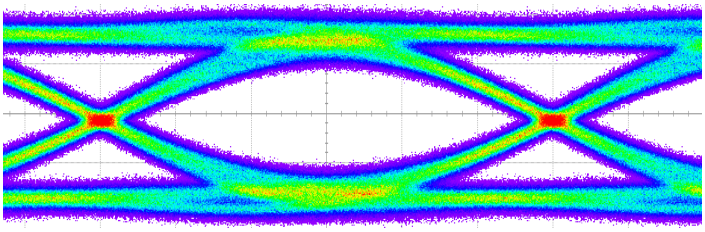

Fig. 8. Measured eye diagram for the signal path from UFP to DFP: applied CTLE = 5 dB, eye height = 353.1 mV, eye width = 84.2 ps.

CONCLUSION

In this work, we presented the design challenges of the front end of USB 3.1 Gen 2.0 (SuperSpeed 10 Gbps) protocol analyzer. A well designed and optimized front end of USB analyzer adds 0 dB of insertion loss to the cable assembly portion which is compliant with USB specs. Simulation results are in good agreement with actual measurements and testing in frequency and time domain. Actual recording of traffic using the USB analyzer was performed successfully at Gen 2.0 speed of 10 Gbps.

REFERENCES

[1] Universal serial bus 3.1 specification, USB Implementers Forum, Inc., Rev 1.0, July 26, 2013.

[2] Universal serial bus type-C Cable and connector specification, USB 3.0 Promoter Group, Rev 1.0, August 11, 2014.

[3] H. Heck, USB 3.1 loss budgets, Rev 0.0, December 29, 2014.

[4] ANSYS HFSS, Pittsburgh, PA, Version 15.0.3, 2014.

[5] M. A. EL Sabbagh, "Full-Wave Modeling of RF Front End for Successful Design of DDR4 Interposer for Probing Purposes," Electrical Performance of Electronic Packaging and Systems (EPEPS), 2014 IEEE 23rd Conf., Portland, OR, Oct. 2014, pp. 113–116.