Hardware accelerator for EV3a

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I. Introduction

Since EV3a algorithm has already existed. As a result, we would like to improve it performance by realizing a specific hardware architecture. Common technique in digital design involve pipelining, caching and so on. In this final project, we'll be using these technique to reduce time complexity of EV3a algorithm.

II. Design Flow Chart

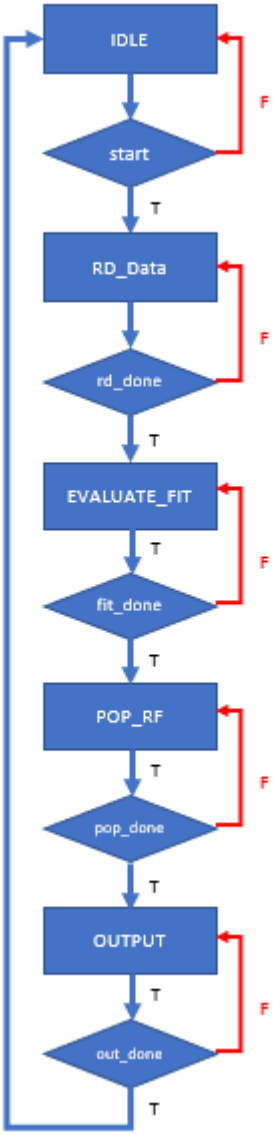


Fig. 1:ASM Chart

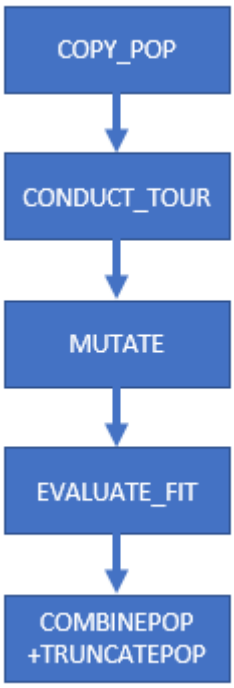
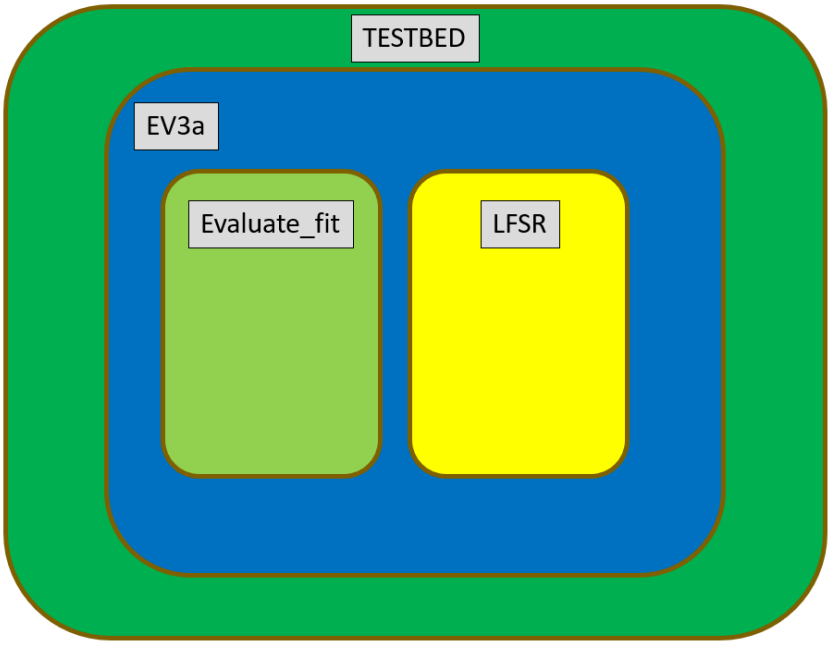


Fig. 2:POP_RF flow chart

III. Hardware specification

Block diagram



Input-output interface

Evaluate fit

Signal Name	I/O	Width	Simple Description
Self_energy	I	4*3	Bus extension s.t it can be loaded in 1 cycle
Interact_energy	I	4*3*3	Bus extension s.t it can be loaded in 1 cycle
Num_particleType	I	2	Number of types of particle
Ind_state	I	2*11	All of state in a individual
clk	I	1	Posedge triggered Clock
rst_n	I	1	Asynchronous negedge Reset
In_valid	I	1	Indicate the data reading in is valid
start	I	1	Start calculation
Ind_fit	O	10	Individual fitness
Out_valid	O	1	Indicate the data out is valid
done	O	1	Done calculation

EV3a

Signal Name	I/O	Width	Simple Description
Num_generations	I	8	Number of generations for EA
Self_energy	I	4	Reading in Self_energy Vector which depends on Num_Particles
crossoverFraction	I	8	Crossover population depends
Interact_energy	I	4	Reading in interaction Matrix which depends on Num_Particles
Num_particleType	I	2	Number of types of particle
Pop_size	I	8	The number of population size
Ind_state_in	I	2*11	State_input
clk	I	1	Posedge triggered Clock
rst_n	I	1	Asynchronous negedge Reset
In_valid	I	1	Indicate the data reading in is valid
Mutate_rate_in	I	8	Mutate_rate
Min_fit_out	O	10	The lowest fit of the individual
done	O	1	Done
Best_ind_state	O	2*11	Best individual depends on number of particles
Best_ind_mut	O	8	Best Mutate_rate

LFSR (linear feedback shift register)

Signal Name	I/O	Width	Simple Description
In_valid	I	1	Indicate the data seed is valid
random_seed	I	8	Random seed
clk	I	1	Posedge triggered clock
rst_n	I	1	Asynchronous negedge Reset
random_num_ff_o	O	8	Random 8 bit number

IV. Expectation

We hope the output fitness will meet the expectation value. And the total calculation time(clk_period*clk_cycle time) can be as small as possible.

V. Reference

HW6 EV3a