**Hardware accelerator for EV3a**

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1. Introduction

Since EV3a algorithm has already existed. As a result, we would like to improve it performance by realizing a specific hardware architecture. Common technique in digital design involve pipelining, caching and so on. In this final project, we’ll be using these technique to reduce time complexity of EV3a algorithm.

1. Design Flow Chart

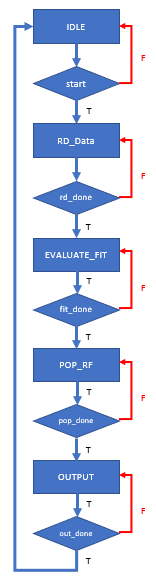
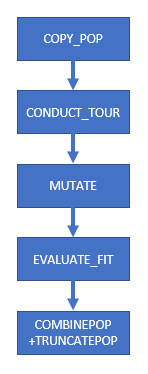
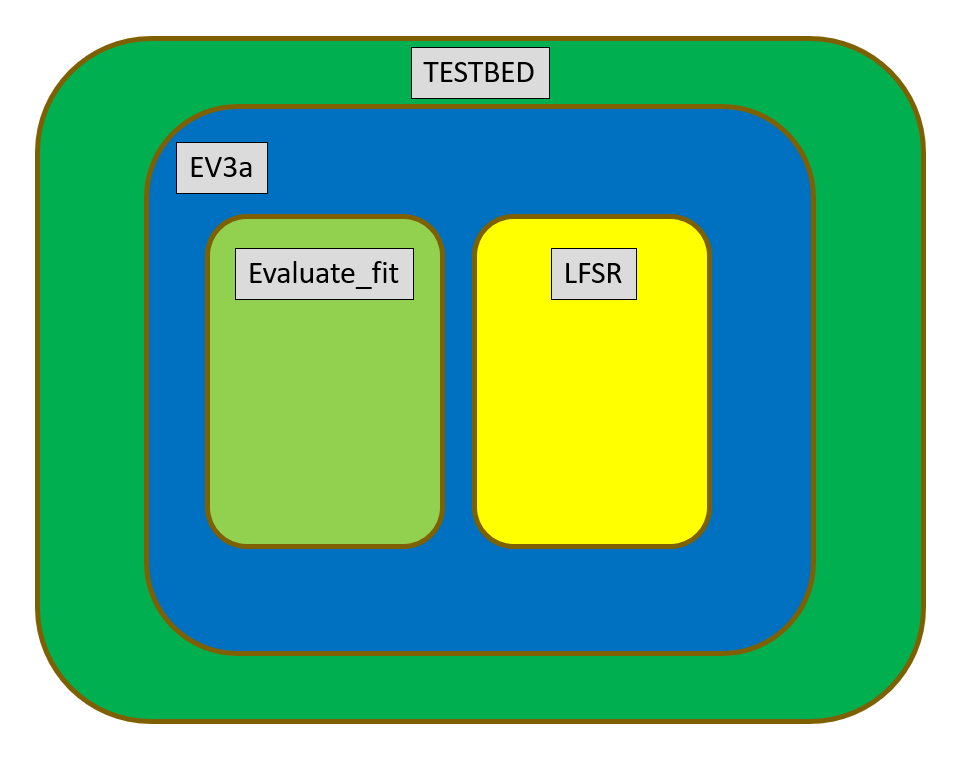
 

Fig. 2:POP\_RF flow chart

Fig. 1:ASM Chart

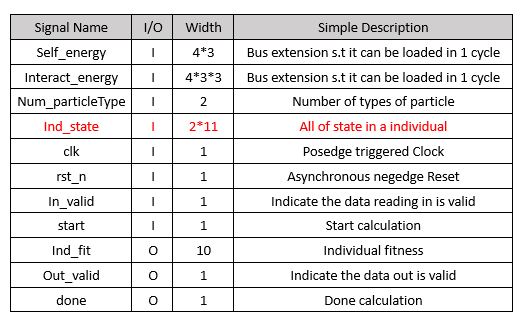
1. Hardware specification

* Block diagram

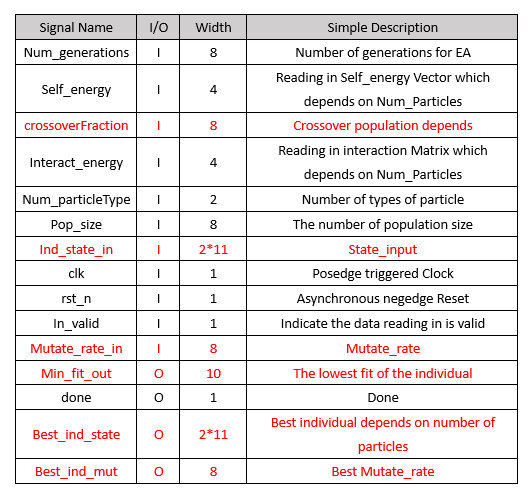


* Input-output interface

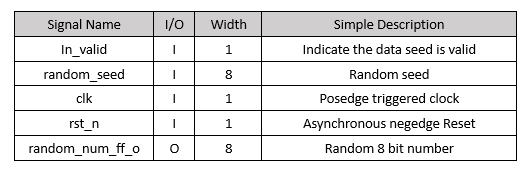
Evaluate fit



EV3a



LFSR (linear feedback shift register)



1. Expectation

We hope the output fitness will meet the expectation value. And the total calculation time(clk\_period\*clk\_cycle time) can be as small as possible.

1. Reference

HW6 EV3a