HSPICE
Memory - SRAM

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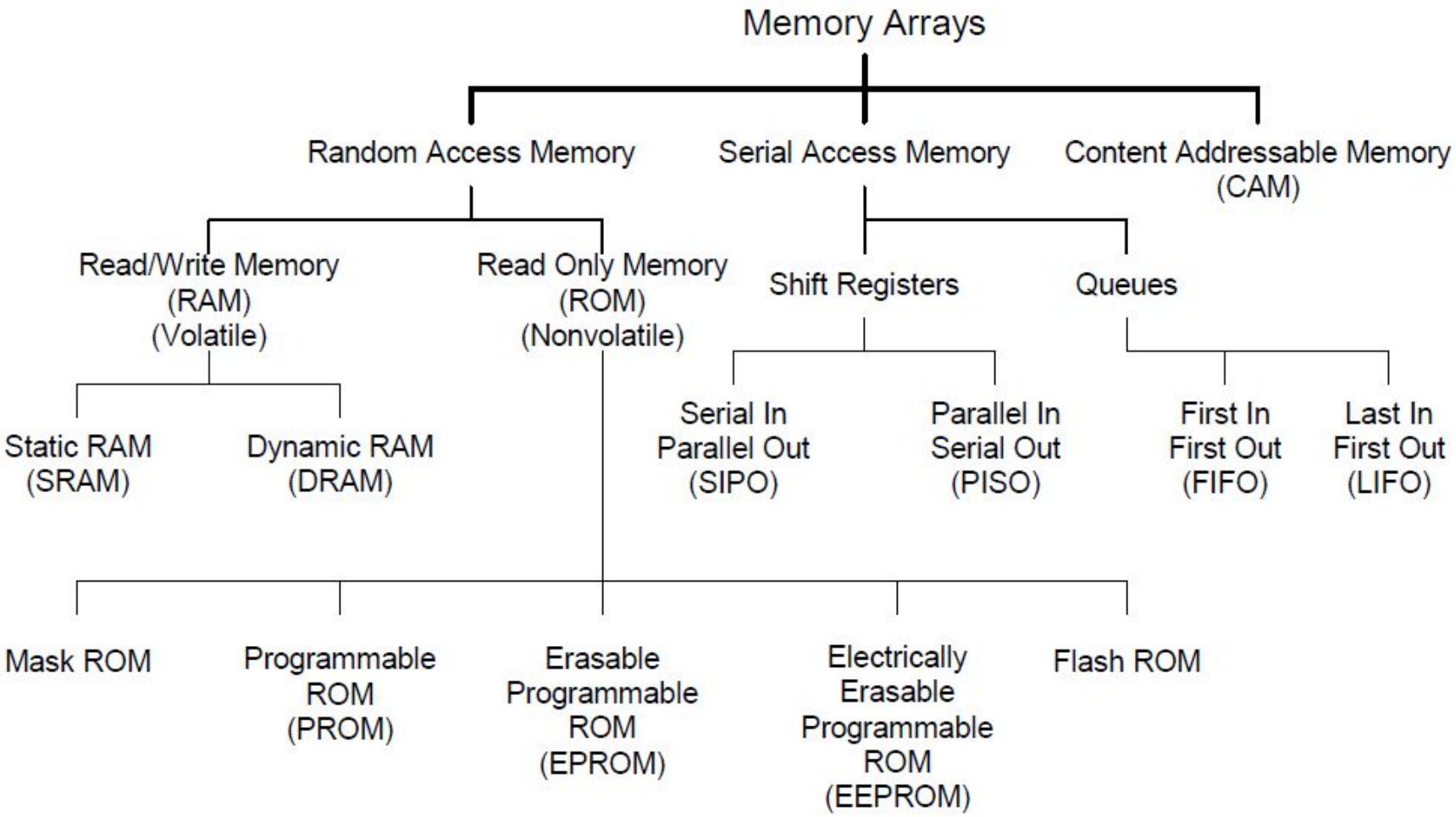
Memory Categories

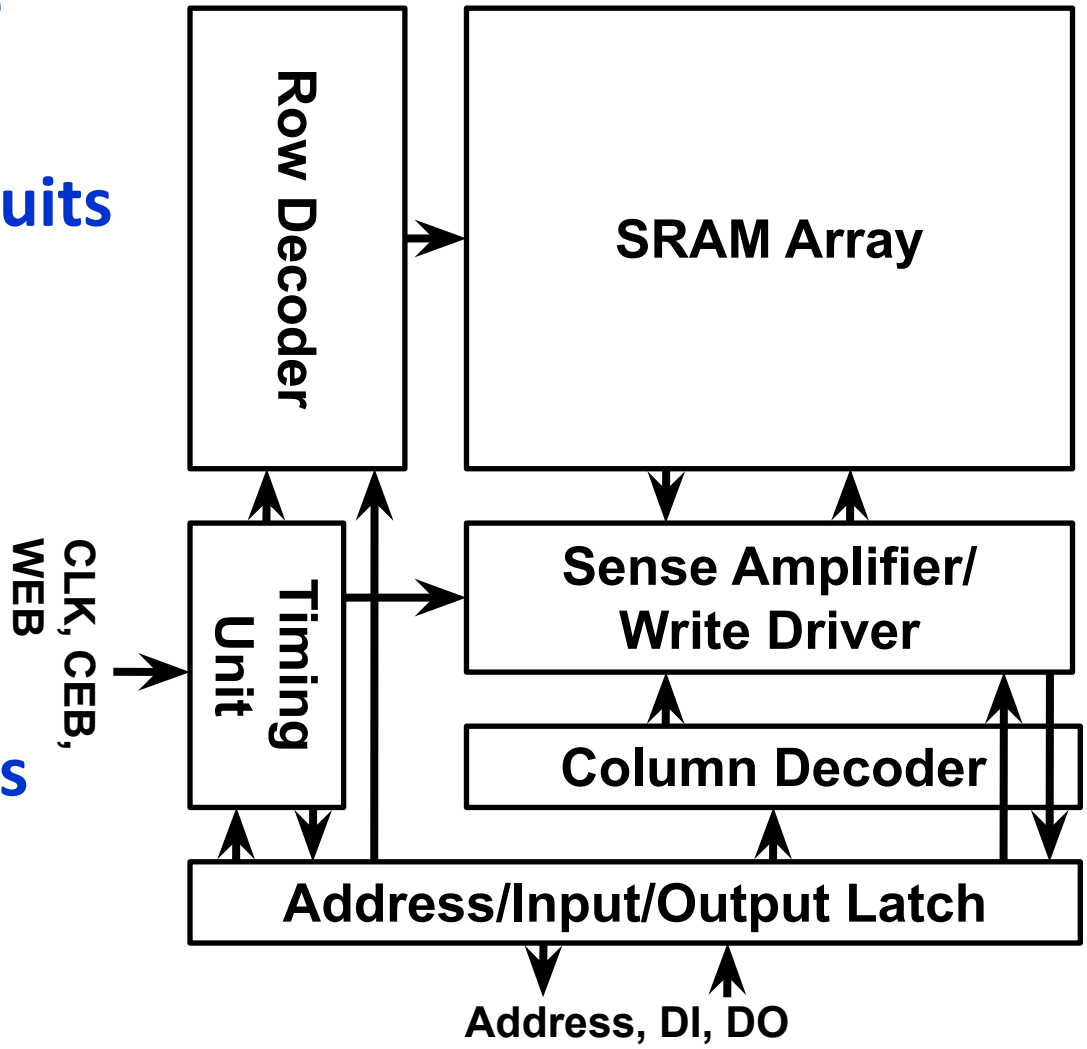


Memory Categories

- RAM : Random Access Memory
  - Historically defined as memory array with individual bit access
- ROM : Read Only Memory
  - Write typically requires high voltages or erasing by UV light
- Volatility vs. Non-volatile of Memory
  - Volatile memory loses data over time or when power is removed (ex : RAM)
  - Non-volatile memory stores data even when power is removed (ex : ROM)
- Static vs. Dynamic Memory
  - Static : holds data as long as power is applied (SRAM)
  - Dynamic : must be refreshed periodically (DRAM)

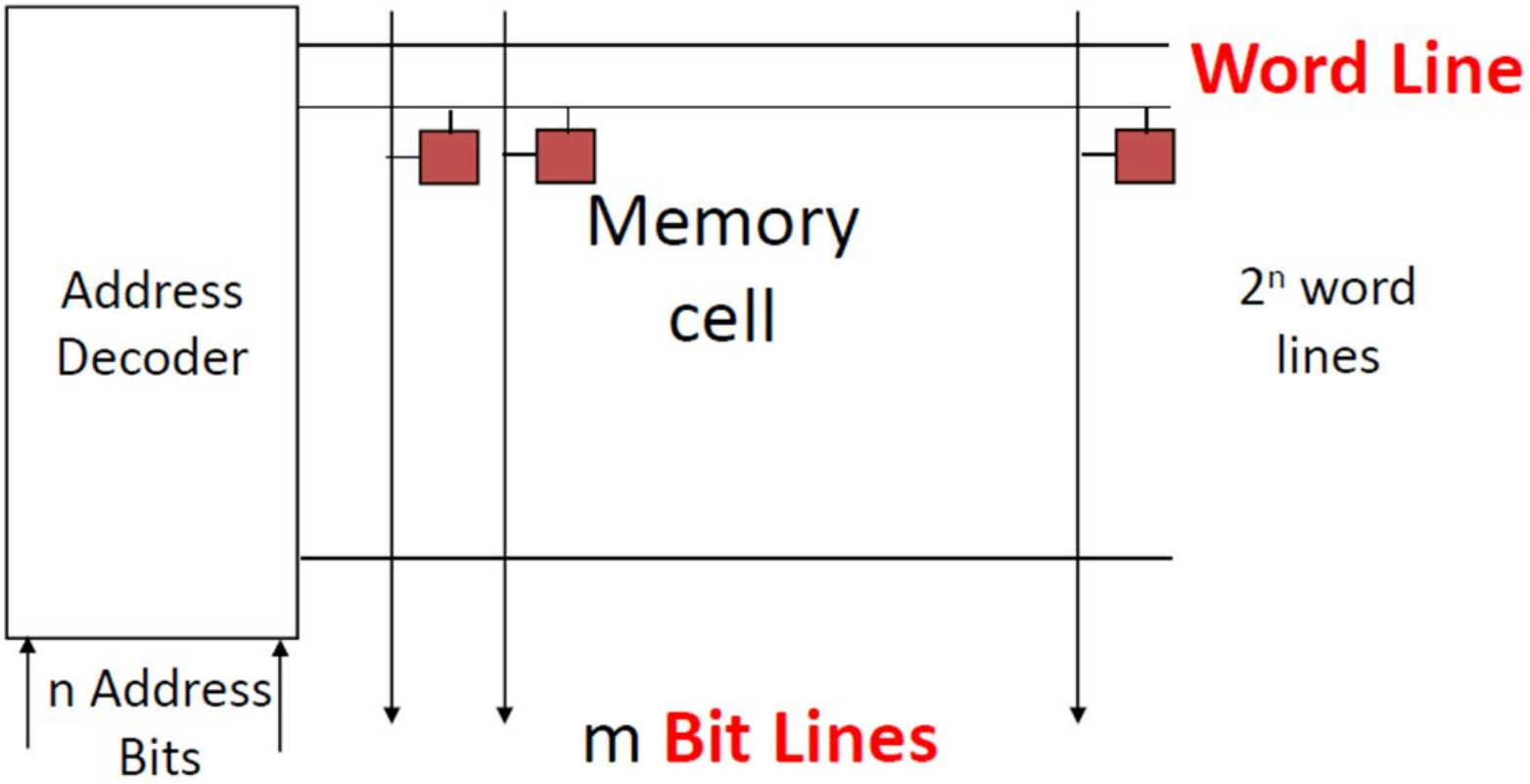
SRAM Architecture

- **SRAM basic structure**
  - SRAM Array
- **SRAM Peripheral Circuits**
  - Sense amplifier
  - Write Driver
  - Row decoder
  - Column decoder
  - Timing unit
- **SRAM I/O Latches/FFs**
  - Address Latch
  - Input latch
  - Output latch



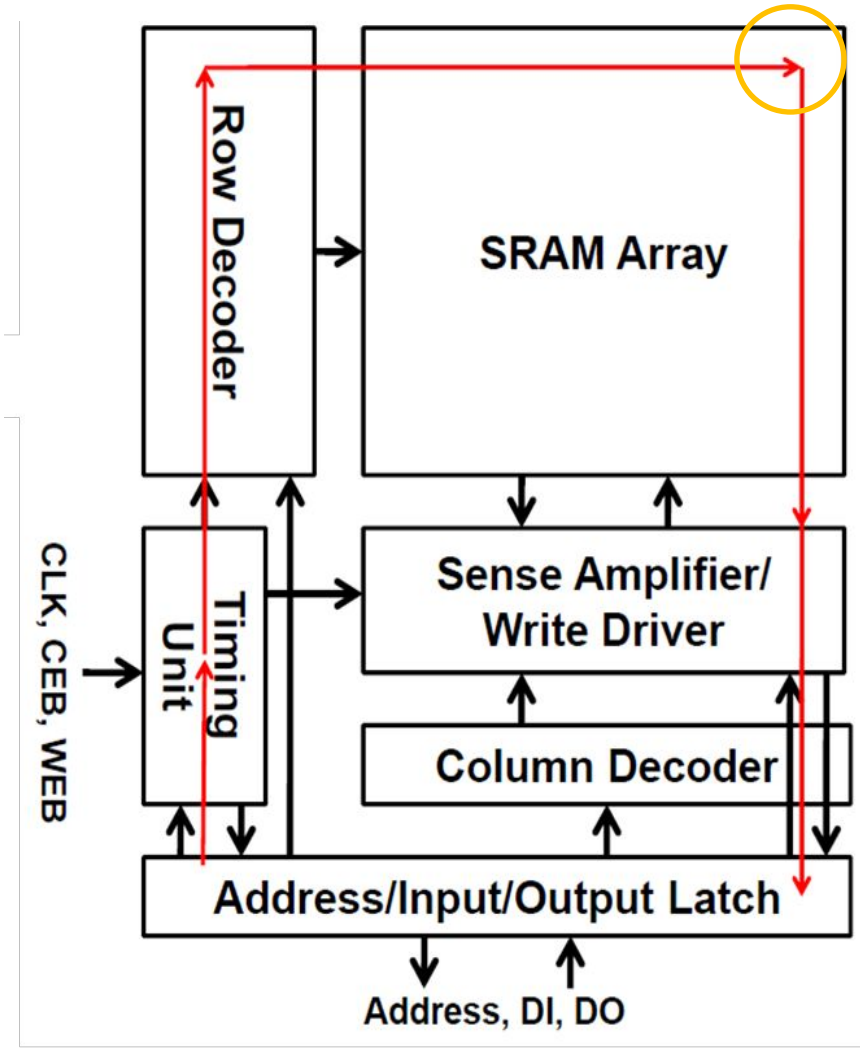
SRAM Array

- 2^n *words* of 2^m *bits* each



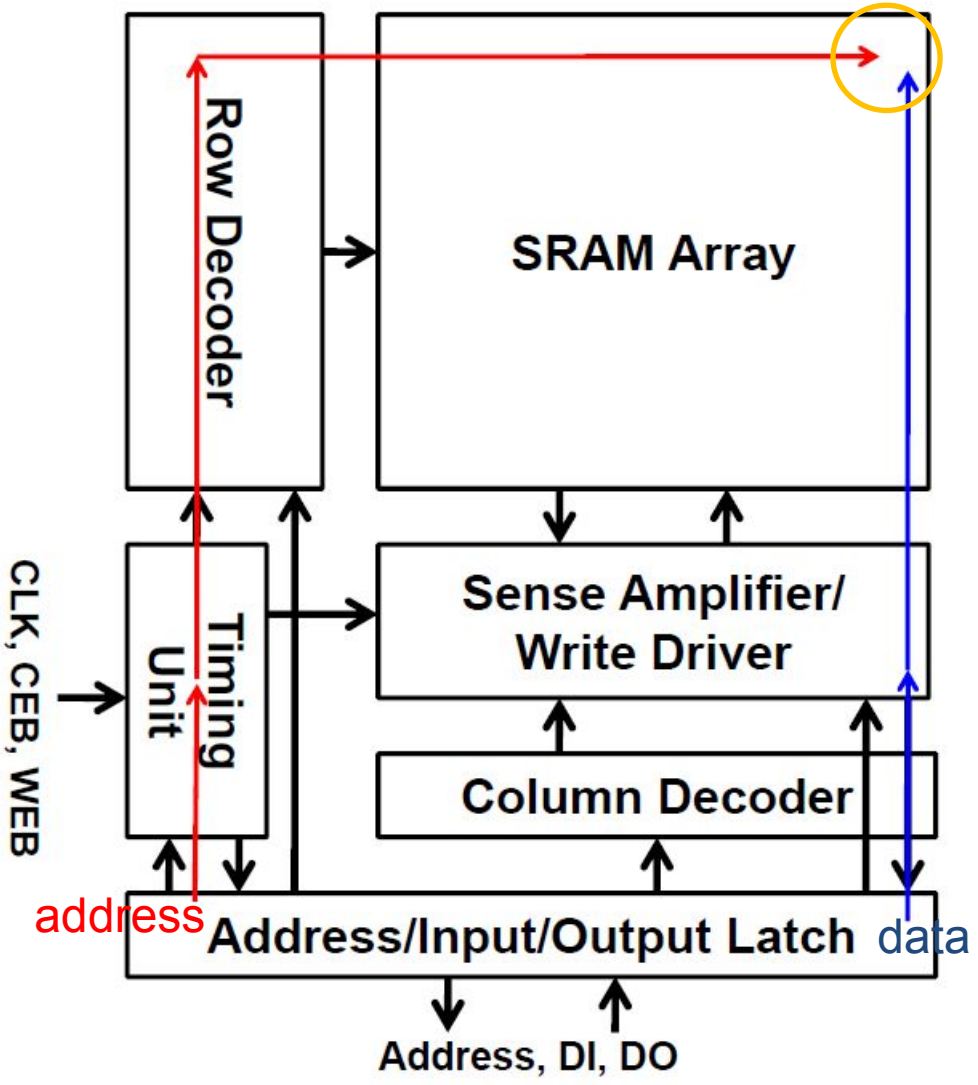
Read Operation in Global Circuits

- **Read Path**
  - Address latch
  - Timing Unit
  - Row Decoder (WL driver)
  - SRAM Array
  - Selected WL
  - Selected BL pairs
  - Sense Amplifier
  - Output latch



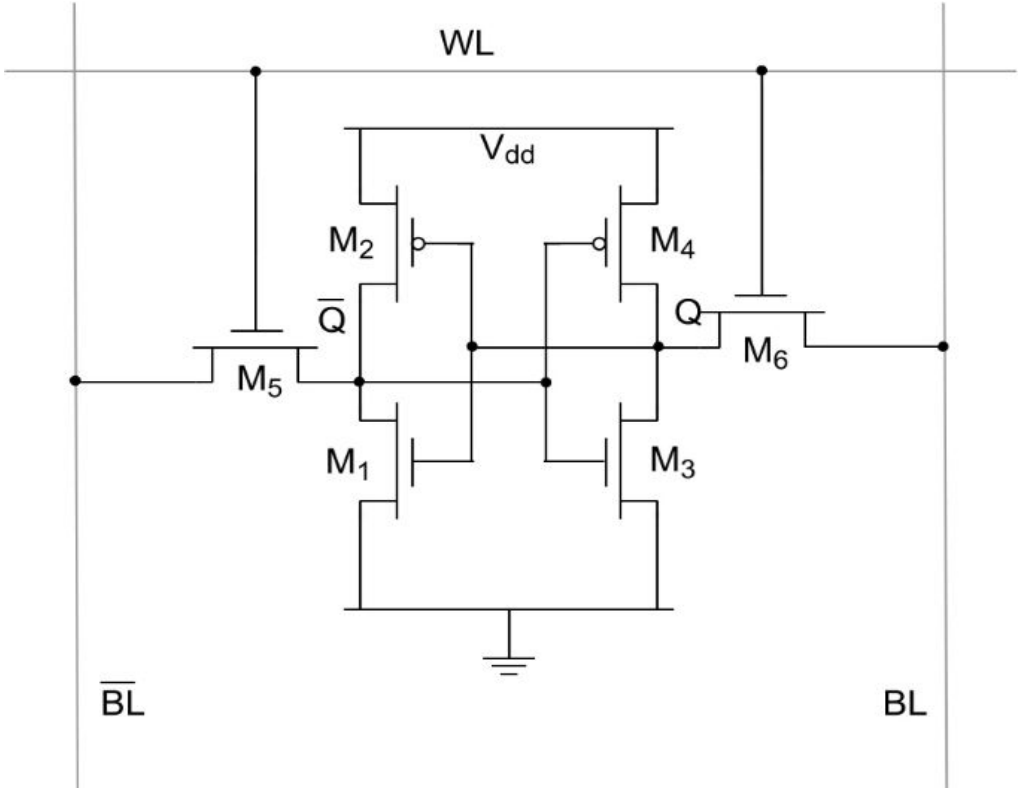
Write Operation in Global Circuits

- **Data Path**
  - Input latch
  - Write Driver
  - SRAM Array (Selected BL pairs)
- **Control Path**
  - Address latch
  - Timing Unit
  - SRAM Array (Selected WL)



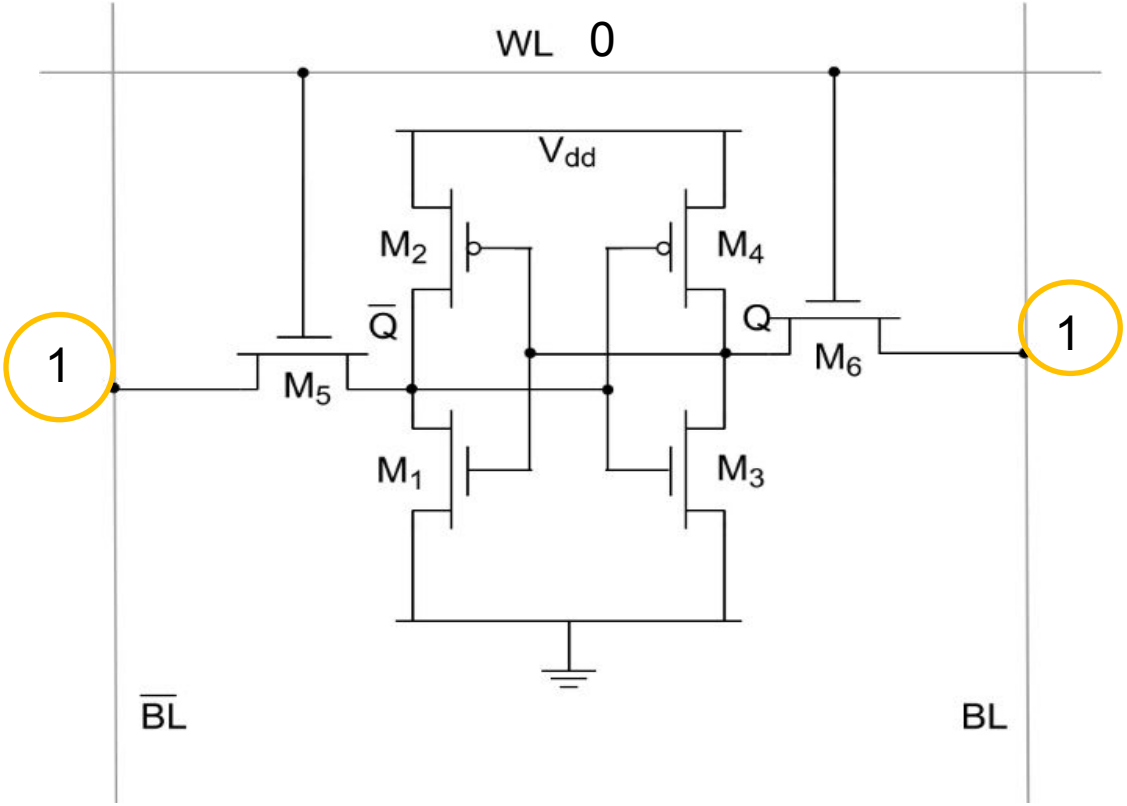
6T SRAM Cell

- Cross-coupled inverter to latch/store data
- Bi-directional access transistor
  - ∵ NMOS : ”strong 0 weak 1” when passing data
    ∴ SRAM cell is written through data 0 side.



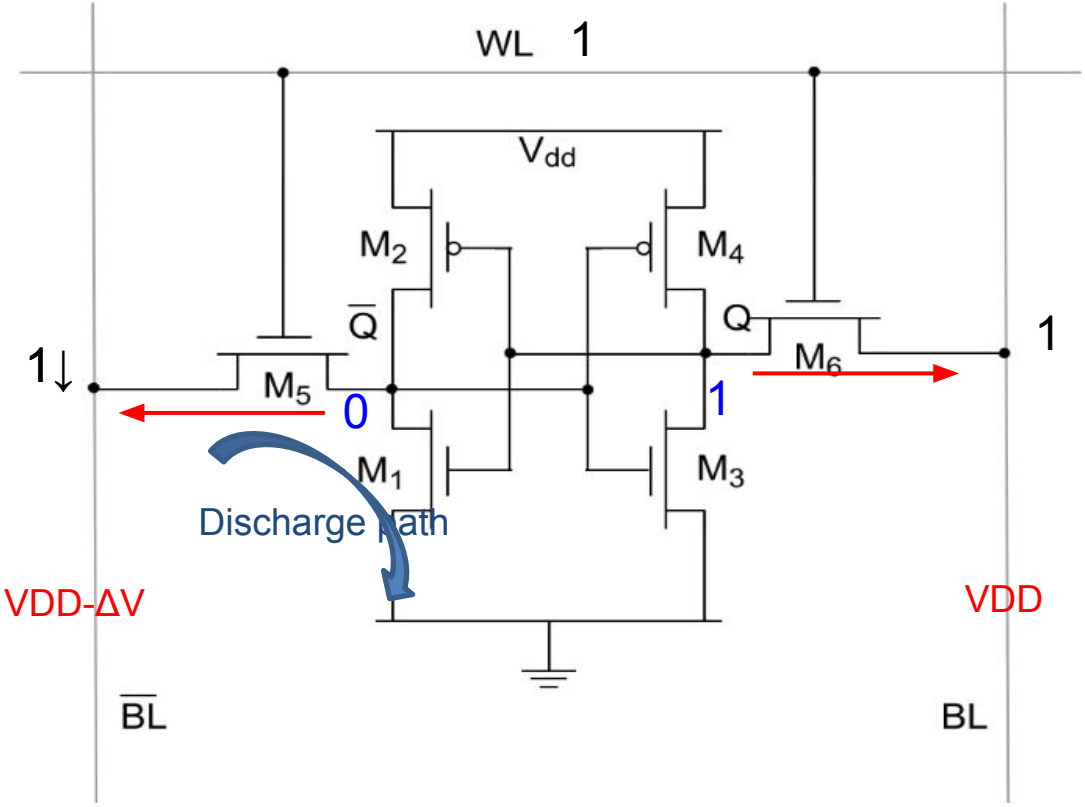
6T SRAM Cell - Hold

- When power on and no read/write operation command input.
- Bit line & bit line bar is pre-charged, preparing for the command input and do the operations.



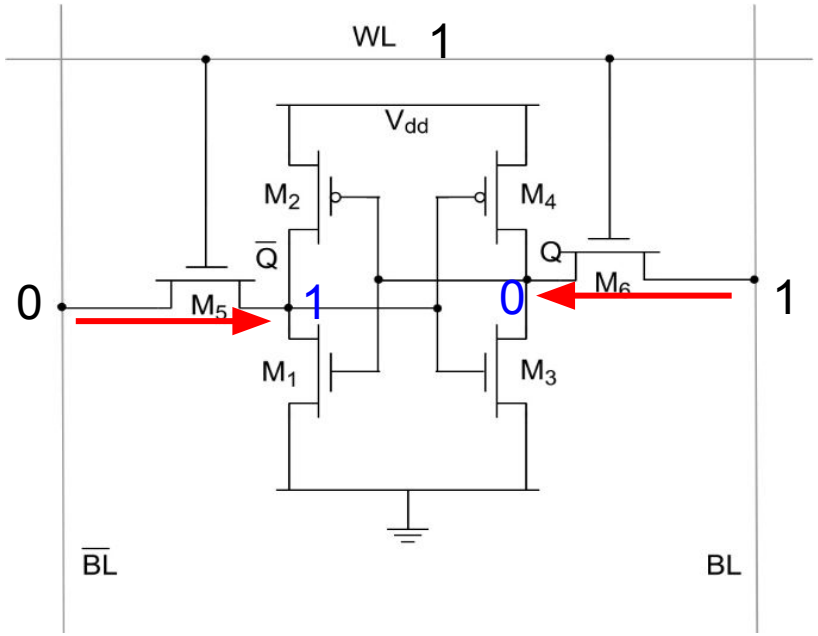
6T SRAM Cell - Read

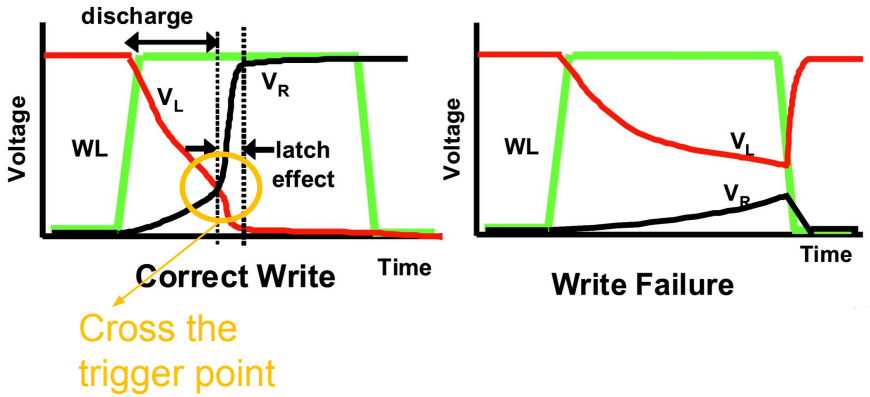
- Open word line (pull high) and make the pass transistor opened.
- Data (Q & Q bar) influences bit line & bit line bar. The voltage difference on bit line & bit line bar is small and hard to be sensed by ordinary logic gate correctly. To solve the problem, we need sense amplifier at the bottom of array.
- The sensing time in read operation is the critical path of the SRAM because there are many cell on the column and each size of MOS in cells is small.



6T SRAM Cell - Write

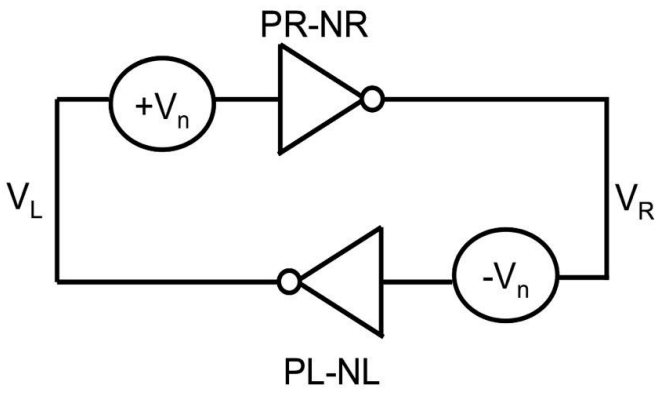
- Write circuit makes bit line & bit line bar transfer to its value.(input 0, input bar 1)
- Open word line and write the value to Q & Q bar.
- Because NMOS pass strong 0 weak 1, the value is written into the cell mainly by “0” side.

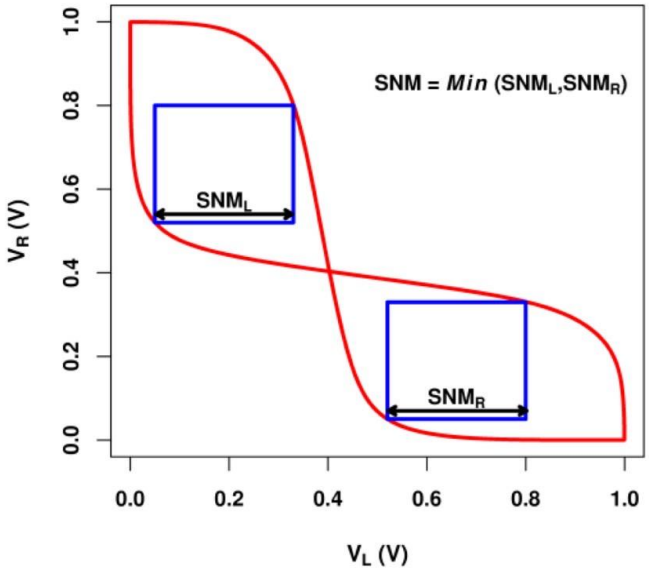




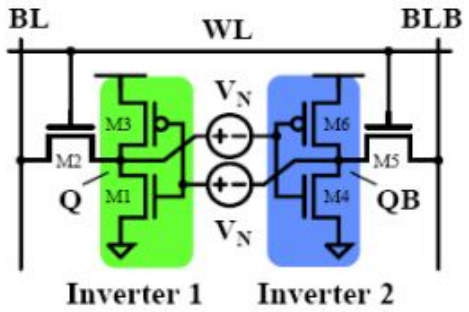
Static Noise Margin (SNM): Butterfly Curve

- SNM: The maximum value of "Vn" that can be tolerated by the flip-flop before changing state
- Standby (or Retention) SNM : word line low
- Read SNM (RSNM) : word line high

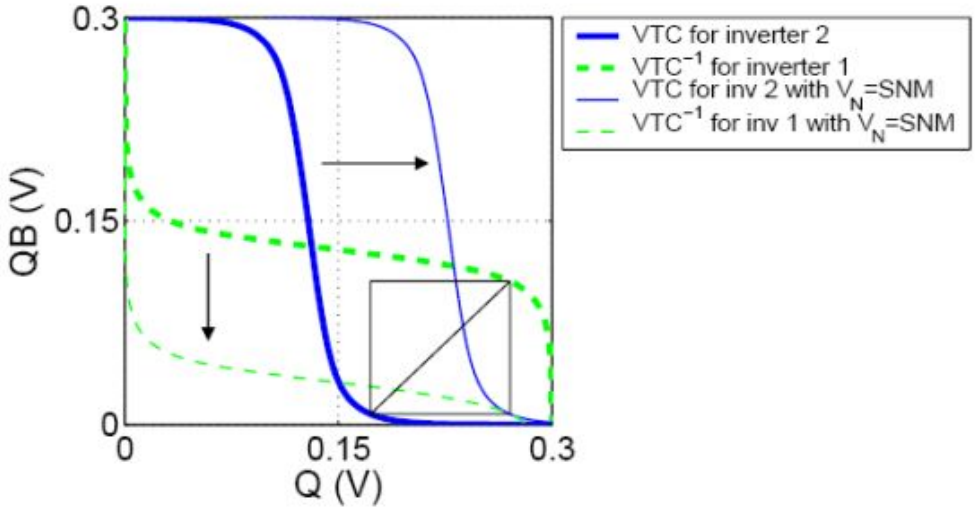


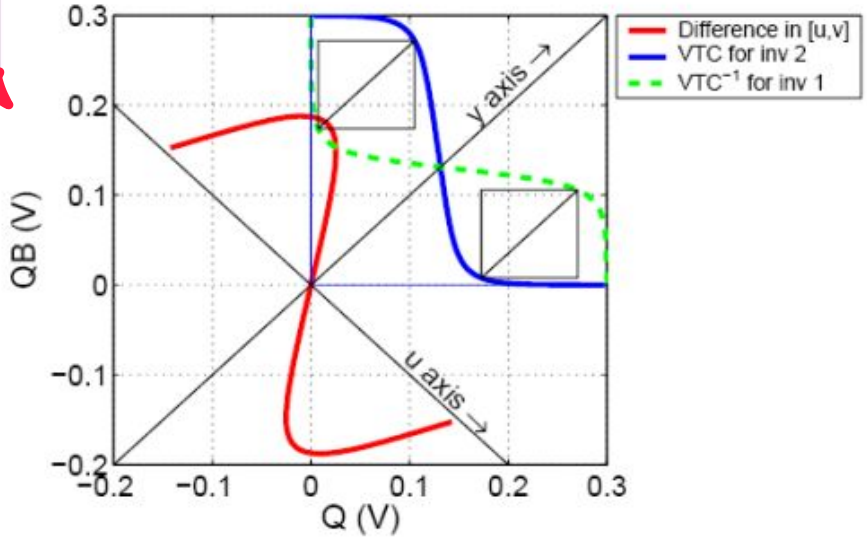


Static Noise Margin (SNM): Butterfly Curve



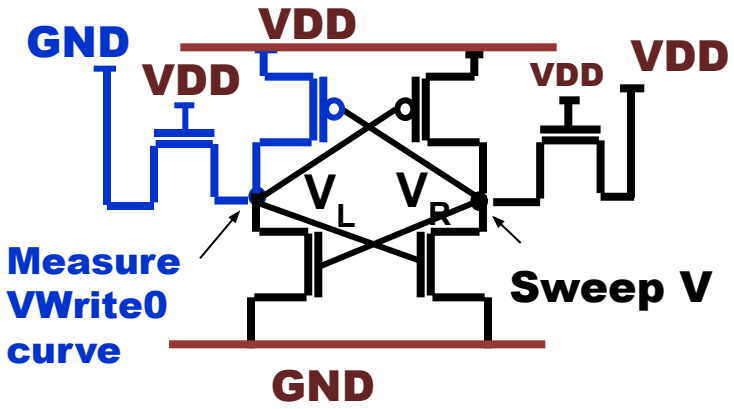
SNM is length of side of the largest embedded square on the butterfly curve

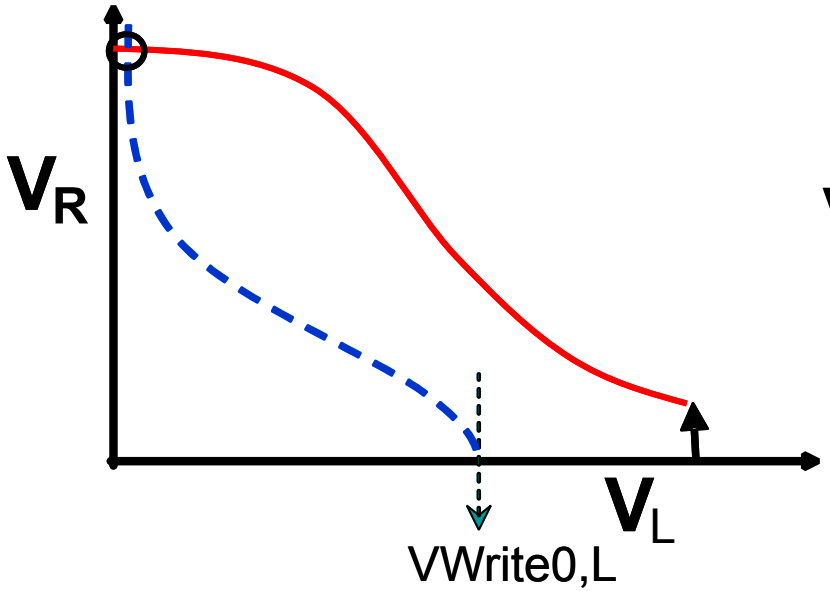


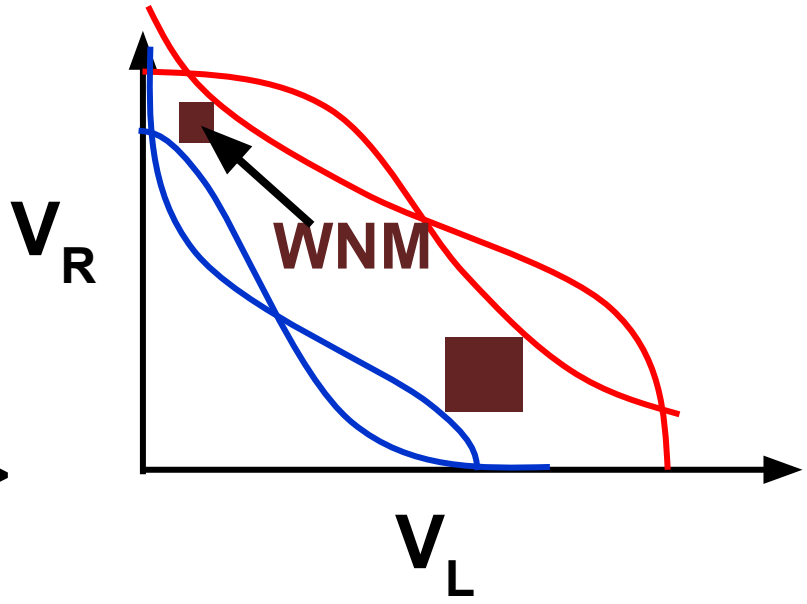


E. Seevinck, F. List, J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells" JSSC, Oct '87.

Write-ability and Write Margin

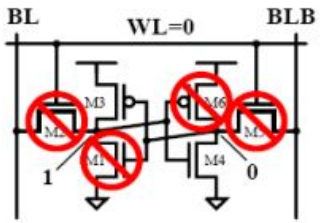


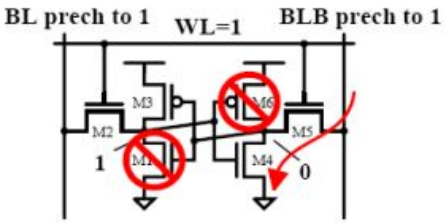


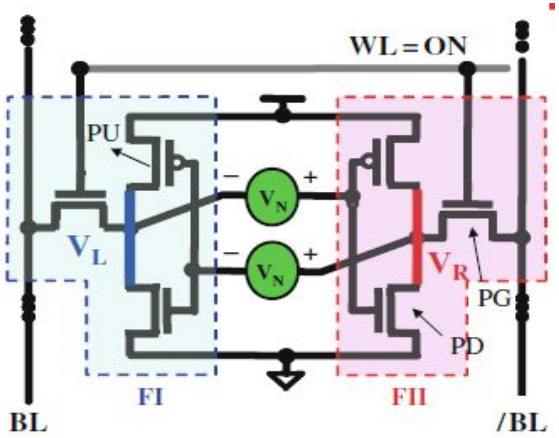


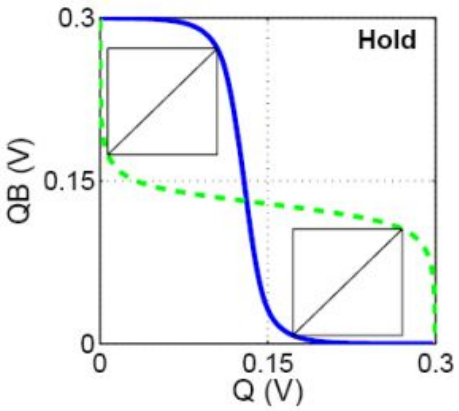
Exercise

- Using 7nm FinFET model to design an 6T SRAM and measure its WM and HSNM and RSNM
- Show the wave form :
  - SNM (show signal : v1, v2)
    - Hold SNM
    - Read SNM
    - Write SNM

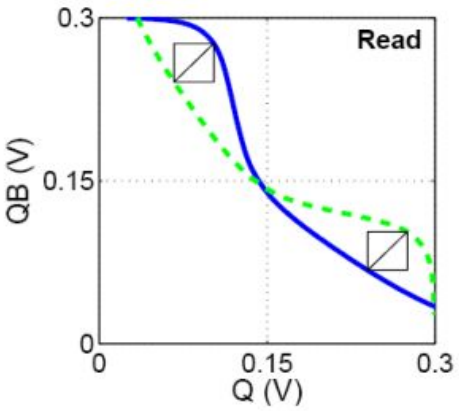








Hold



Read

Exercise Notice

② Edit of voltage.

- BL & BLB : I prefer using ".ic" command instead of using ordinary voltage definition because BL & BLB would be floating after pre-charged in the real circuit.

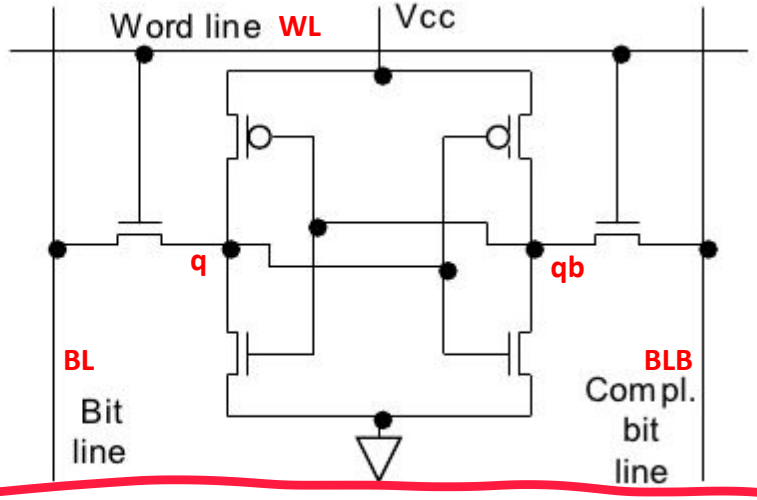
```
.ic V(??.BL)= ?? * ?? need to be edited
.ic V(??.BLB)= ?? * ?? need to be edited
```

- Adding the capacitor on BL & BLB is to make the simulation closer to reality. (if the wave form is weird you can adjust by yourself)

```
CBLB BLB GND BITCAP
CBL  BL  GND BITCAP
```

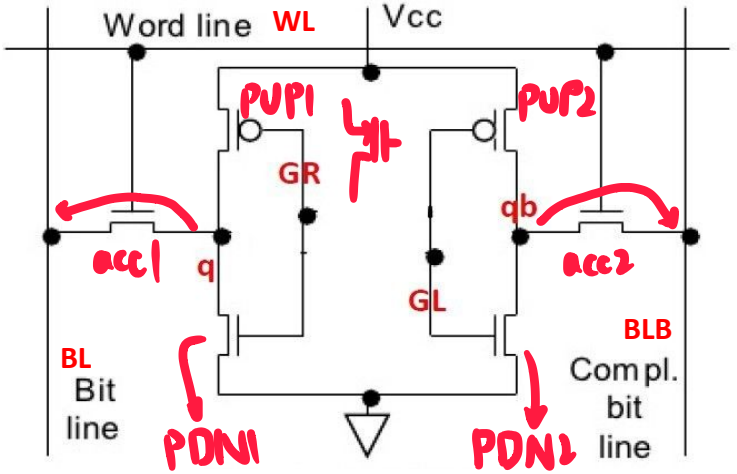
Exercise Hint

- Ordinary case :



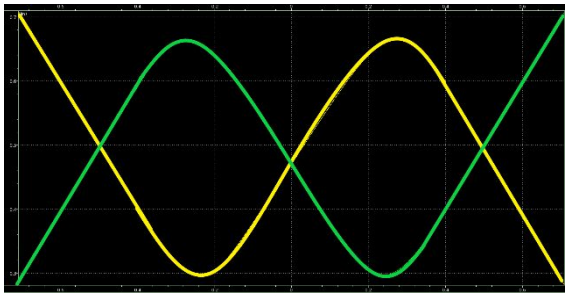
① Create this SRAM hspice schematic.

- SNM :

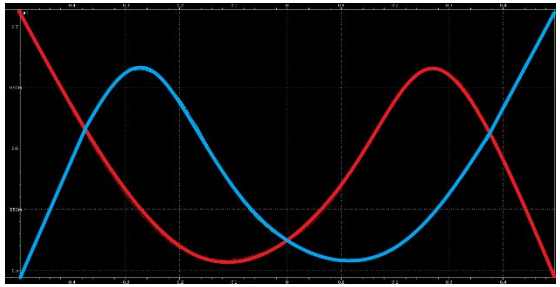


Exercise SNM Wave Form Hint

- Hold SNM wave form :



- Read SNM wave form :



- Write SNM wave form :