ASAP7 PDK

DESIGN RULE MANUAL

PDK Release 1p5

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1 Concerning This Manual

1.1 COPYRIGHT

1.2 Terminology and Conventions Used in This Manual

1.2.1 Terminology

BEOL: Refers to ‘back-end-of-line’ interconnect (M1-M9) and via layers (V1-V8).

End-cap: The term is typically used across the manual in the context ‘via with/without/with no (metal) end-cap’ and implies whether or not an instance of via is enclosed by the top metal—upper of the two interconnect layers that the via connects—on either sides by a stipulated amount.

EUV: Refers to ‘extreme ultra-violet’ rays. In places, the term has been used to refer to EUV-based lithography.

FEOL: Refers to ‘front-end-of-line’ layers, viz. WELL, FIN, GATE, ACTIVE, GCUT, NSELECT, PSELECT, SLVT, LVT, and SDT.

LELE: Refers to ‘Litho-etch litho-etch’—a lithography technique.

MOL: Refers to ‘middle-of-line’ layers, viz. LIG, LISD, and V0.

SE: Refers to ‘single exposure’.

SADP: Refers to ‘self-aligned double patterning’—a lithography technique.

SAV: Refers to ‘self-aligned via’

Top metal: Refers to an interconnect layer with respect to which a via is self-aligned.

1.2.2 Notes On Conventions

1. The figures provided in this manual are not drawn to scale and in some figures the geometries have been accentuated for the purpose of illustration. Therefore, designers must not to base their interpretation of rules solely on the scale at which the figures are drawn.
2. Pitch rules are an exception to the rule type ‘spacing’, in that their rule value does not denote the distance between the exterior side of edges, but rather between (same orientation) centerlines of the polygons for which the pitch rule is specified. Fig. 1.2.1 illustrates generic horizontal and vertical pitch rules.
3. If an exact width rule, such as W.1 in Fig. 1.2.2 (a), or an exact pitch rule, such as S.1 in Fig. 1.2.2 (a), has been defined, then it follows from these rules that any different width or pitch value, either larger or smaller than the stipulated rule value, will be in violation of the rule, as shown in Fig. 1.2.2 (b). The cross (×) in Fig. 1.2.2 (b) indicates a rule violation.
4. Fig. 1.2.3 illustrates the definition of terms ‘interacting’ and ‘not interacting’. For any two polygons to be classified as ‘interacting’, one of the polygons must either lie completely within, or intersect, or touch—except when it is at a single point (vertex)—another polygon. All Layer1 polygons interact with the Layer2 polygon in Fig. 1.2.3 (a), while none of the Layer1 polygons interact with the Layer2 polygon in Fig. 1.2.3 (b).
5. If the terms ‘horizontal’ or ‘vertical’ are not used in a particular rule, then assume that both of them apply.
6. The term ‘channel’ refers to the region formed by the intersection of the layer ACTIVE and GATE.
7. Unless otherwise stated, assume that the rules are for layer geometries that do not interact with the layer SRAMDRC.
8. Polygons ‘P’ and ‘Q’ in Fig. 1.2.4 (a) are said to be ‘on the same net/connected’ as they share the same electrical node ID, while polygons ‘R’ and ‘S’ in Fig. 1.2.4 (b) are said

to be ‘not on the same net/different nets/not connected’ since they have different electrical node IDs.

9. The terms ‘along the length’ and ‘along the width’ denote the direction—defined with respect to a geometry—along which a particular rule is specified and are independent of either the x or y axis (see Fig. 1.2.5). The former term refers to the direction along which the geometry has a larger edge, while the latter refers to the direction along which the geometry has a shorter edge.
10. Referring to Fig. 1.2.6, the vias in Fig. 1.2.6 (a) are said to be ‘fully-aligned’ with respect to each other, those in Fig. 1.2.6 (b) are said to be ‘partially aligned’ with respect to each other, while the vias in Fig. 1.2.6 (c), (d), and (e), are said to be ‘not aligned’ with respect to each other.

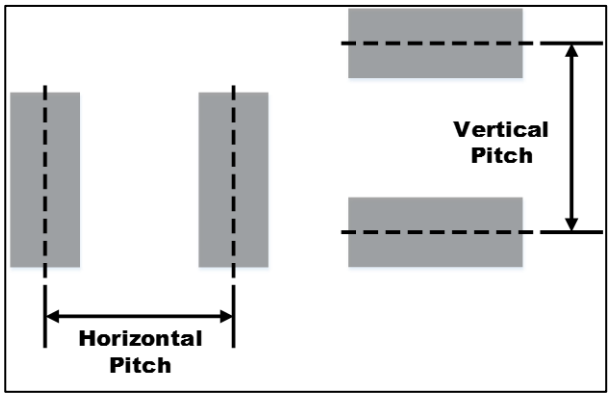

Fig. 1.2.1 Horizontal and vertical pitch definition.

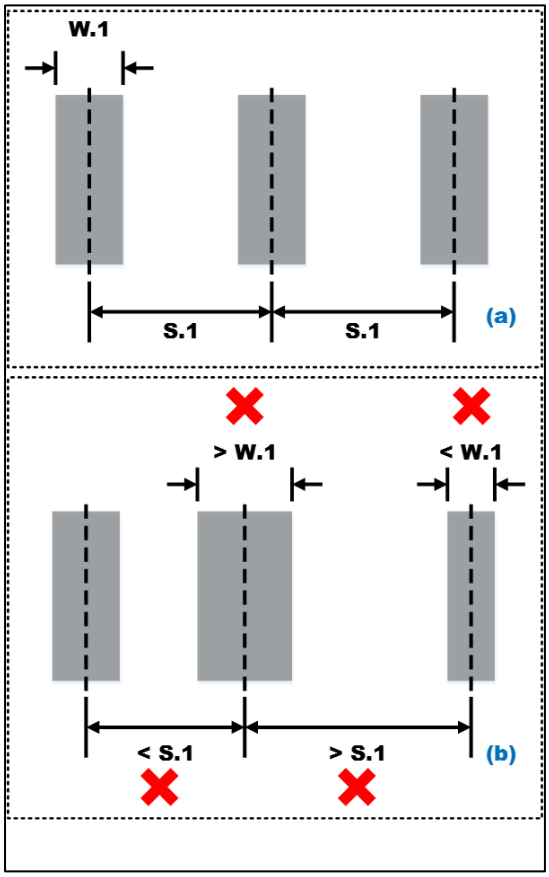

Fig. 1.2.2 Exact spacing and width convention.

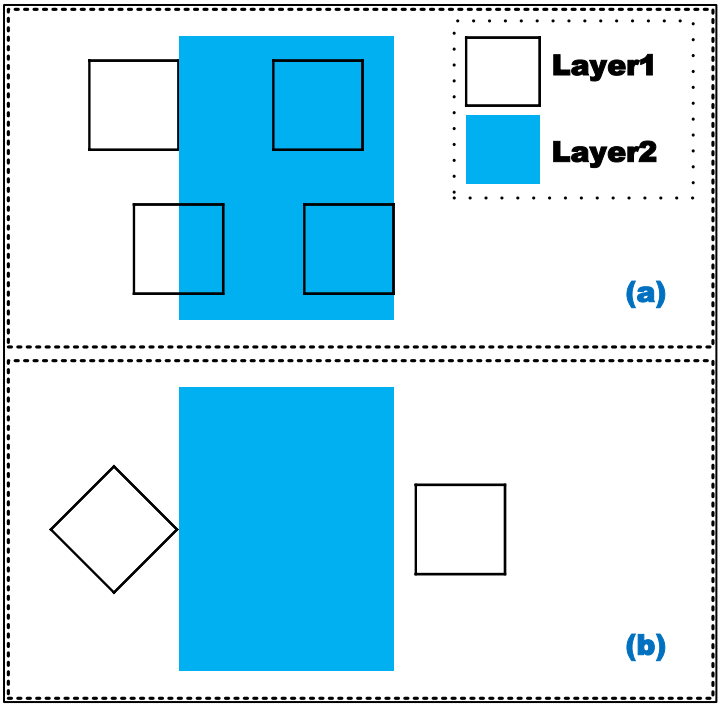

Fig. 1.2.3 Illustration of the terms 'interacting' and 'not interacting'. (a) All Layer1 polygons interact with the Layer2 polygon. (b) None of the Layer1 polygons interact with the Layer2 polygon.

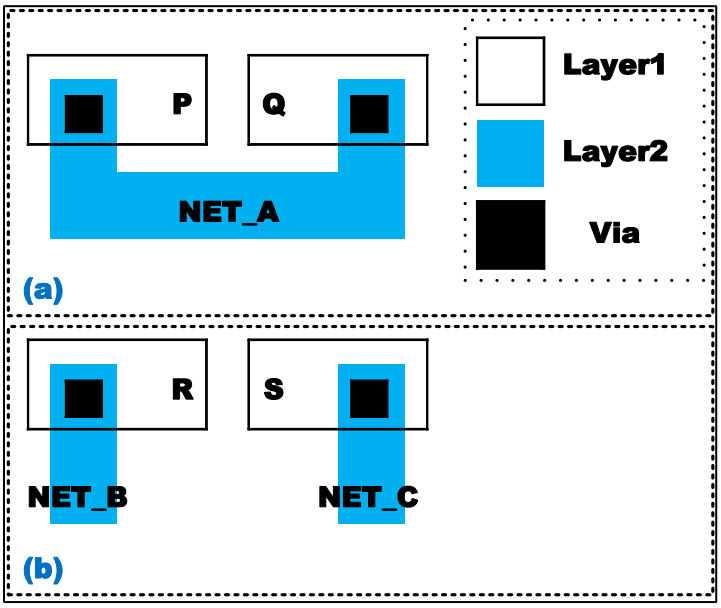

Fig. 1.2.4 Illustration of the terms 'on the same net' and 'not on the same net/different nets'. (a) Polygons 'P' and 'Q' are on the same net. (b) Polygons 'R' and 'S' are on different nets.

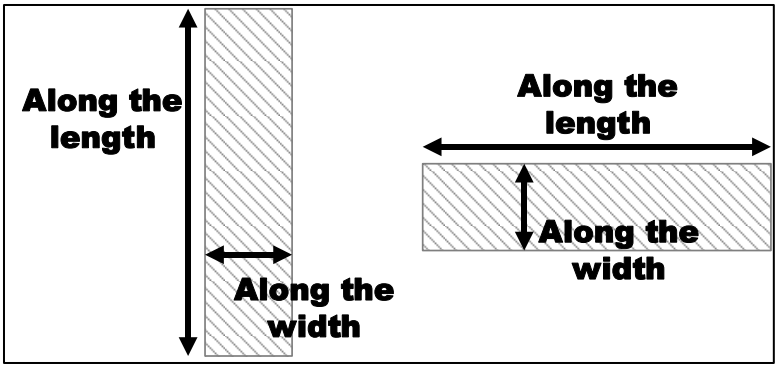

Fig. 1.2.5 Illustration of the terms 'along the length' and 'along the width'.

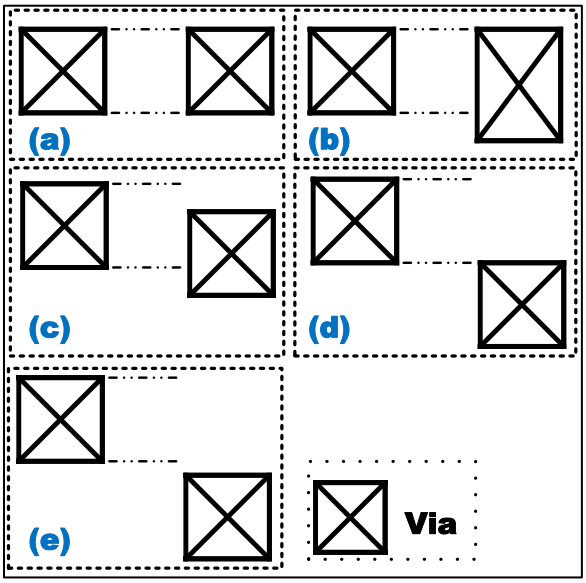

Fig. 1.2.6 Illustration of the terms (a) 'fully aligned', (b) 'partially aligned' and (c-e) 'not aligned'.

1.2.3 Rule Name Convention

Rule name for intra-layer rules: PrimaryLayer.Type.Number

Rule name for inter-layer rules: PrimaryLayer.SecondaryLayer.Type.Number

An inter-layer rule refers to a rule defined between two different layers and an intra-layer rule refers to a rule defined for a single layer.

'PrimaryLayer' and 'SecondaryLayer' represent the layers for which a rule is written. The string 'Type' may have the values listed in Table 1.2.1 below:

Type	Description	Figure
A	An area rule (inter/intra layer).	Fig. 1.2.7 (a)
EN	An enclosure rule (inter layer). Denotes the distance between the exterior side of one layer's edge and the interior side of another layer's edge, where one of the layer geometry lies completely within another layer geometry.	Fig. 1 10 (b)
EX	An extension rule (inter layer). Denotes the distance between the exterior side of one layer's edge and the interior side of another layer's edge, where one of the layer geometry lies partially within another layer geometry.	Fig. 1 10 (c)
GEOMETRY	A geometry check. Stipulates the permitted shape geometry.	
L	A length (intra layer) rule. Denotes the length of a polygon's edge. The scope of this rule type is not limited to just the distance between the interior side of edges of a layer geometry.	Fig. 1 10 (d)
LUP	Latch-up prevention rule.	-
OV	An overlap rule (inter layer). Denotes the distance between interior side of edges of two layers.	Fig. 1 10 (e)
R	A recommended rule (may be waived).	-
S	A spacing rule (inter/intra layer). Denotes the distance between the exterior side of edges of one or two layers.	Fig. 1 10 (f)
SRAM	SRAM related rules—these rules apply to SRAM cells and may be waived for the other cells.	-
W	A width rule (intra layer). Denotes the distance between interior side of edges of a specific layer.	Fig. 1 10 (g)
AUX	Auxiliary rules—the ones that do not fall under any of the above categories (may not be waived).	-

Table 1.2.1 Rule types and their description.

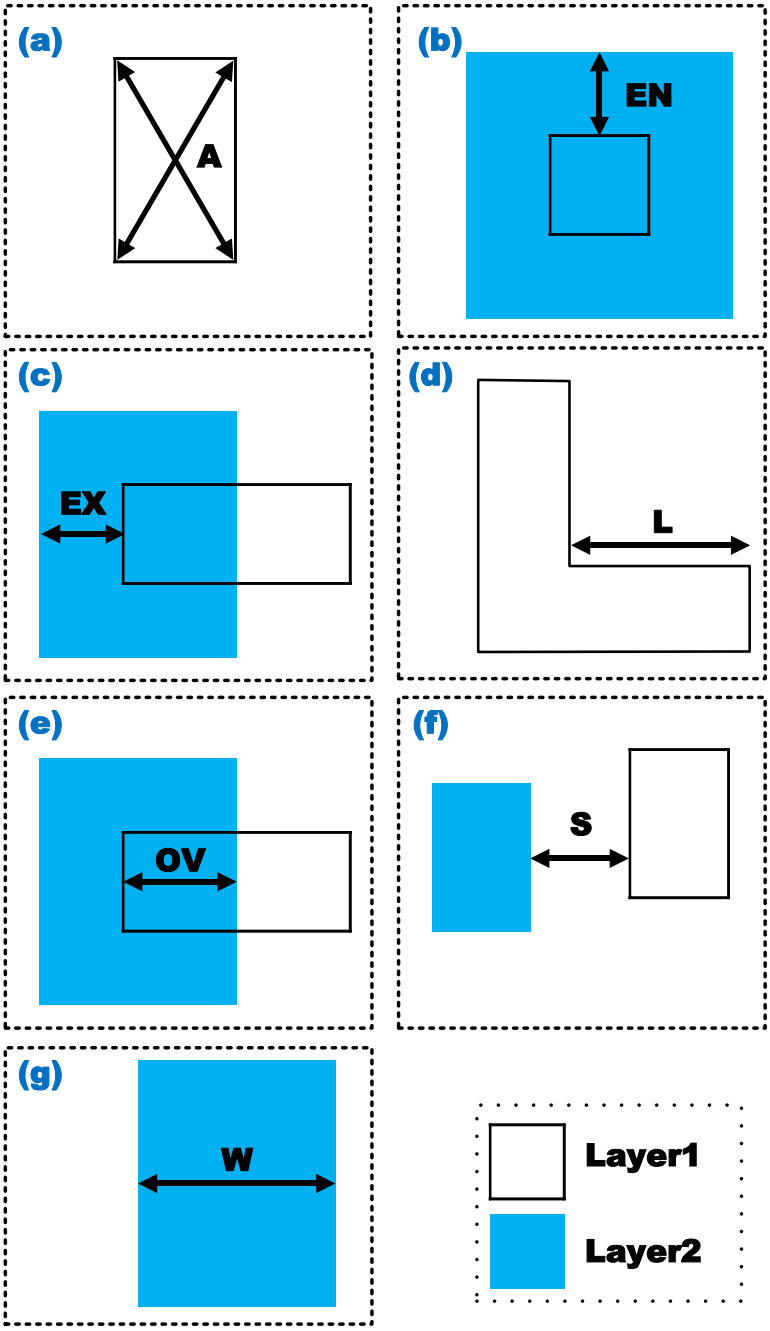

Fig. 1.2.7 Illustration of rule types.

2 Layer Information

2.1 Front-End-of-Line (FEOL) Layer Information

Layer Name	Mask ID	Description	Lithography	Patterning
WELL	1	N-Well	193i	SE
FIN	2	Fin	193i	SAQP
GATE	7	Metal gate without double patterning (assuming coloring is done later)	193i	SADP
GCUT	10	GATE metal cut	EUV	SE
ACTIVE	11	ACTIVE area for fin definition	EUV	SE
SDT	88	Source-drain trench. A layer that connects the layer ACTIVE to LISD	EUV	SE
NSELECT	12	N-implant	193i	SE
PSELECT	13	P-implant	193i	SE
SLVT	97	Super low threshold adjust mask	193i	SE
LVT	98	Low threshold adjust mask	193i	SE
SRAMVT	110	Threshold adjust mask for SRAMs	193i	SE

Table 2.1.1 Front-end-of-line layer information.

2.2 Middle-of-Line (MOL) Layer Information

Layer Name	Mask ID	Description	Lithography	Patterning
LIG	16	GATE interconnect layer	EUV	SE
LISD	17	Source-drain interconnect layer	EUV	SE
V0	18	Via connecting LIG and LISD to M1	EUV	SE

Table 2.2.1 Middle-of-line layer information

2.3 Back-End-of-Line (BEOL) Layer Information

Layer Name	Mask ID	Description	Lithography	Patterning
M1	19	First level of interconnect metal	EUV	SE
V1	21	Via connecting M1 to M2	EUV	SE
M2	20	Second level of interconnect metal	EUV	SE
V2	25	Via connecting M2 to M3	EUV	SE
M3	30	Third level of interconnect metal	EUV	SE
V3	35	Via connecting M3 to M4	EUV	SE
M4	40	Fourth level of interconnect metal	193i	SADP
V4	45	Via connecting M4 to M5	193i	LELE
M5	50	Fifth level of interconnect metal	193i	SADP
V5	55	Via connecting M5 to M6	193i	LELE
M6	60	Sixth level of interconnect metal	193i	SADP
V6	65	Via connecting M6 to M7	193i	LELE
M7	70	Seventh level of interconnect metal	193i	SADP
V7	75	Via connecting M7 to M8	193i	LELE
M8	80	Eighth level of interconnect layer	193i	SE
V8	85	Via connecting M8 to M9	193i	SE
M9	90	Ninth level of interconnect metal	193i	SE
V9	95	Via connecting M9 to Pad	193i	SE
Pad	96	Pad for IOs	193i	SE

Table 2.3.1 Back-end-of-line layer information.

2.4 Marker Layer Information

Layer Name	Mask ID	Description	Lithography	Patterning
DUMMY	8	Special layer for indicating dummy GATE	-	-
SRAMDRC	99	Special layer to enable SRAM related DRCs	-	-
BOUNDARY	100	Place and route boundary layer	-	-

Table 2.4.1 Marker layer information.

3 Physical Design Rules

3.1 Geometry Check

Rule	Rule Type	Description	Operator	Value	Units	Notes
GEOMETRY.NONORTHOGONAL	Width	Non-orthogonal shapes are not allowed	-	-	-	-

Table 3.1.1 Geometry check.

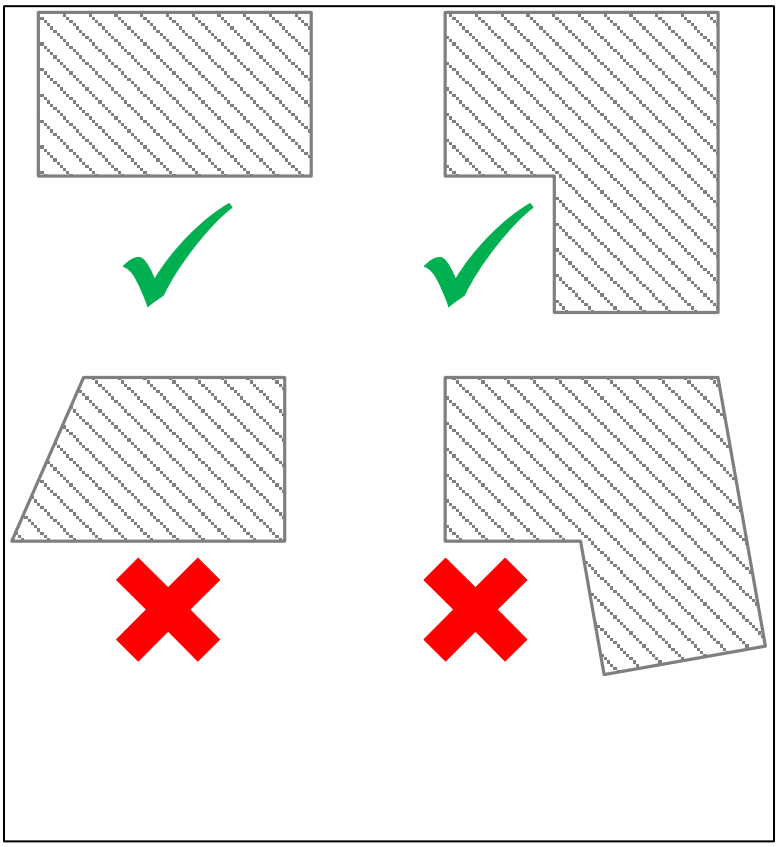

Fig. 3.1.1 Illustration of geometry check.

3.2 WELL Design Rules

Rule	Rule Type	Description	Operator	Value	Units	Notes
WELL.W.1	Width	Minimum horizontal width of WELL	≥	108	nm	-
WELL.W.2	Width	Minimum vertical width of WELL	≥	54	nm	-
WELL.S.1	Spacing	Minimum vertical spacing between WELL layer polygons	≥	108	nm	-
WELL.S.2	Spacing	Minimum horizontal spacing between WELL layer polygons	≥	54	nm	-
WELL.A.1A	Area	Minimum area of WELL	≥	5832	nm-sq	1
WELL.A.1B	Area	Minimum enclosed area of WELL	≥	5832	nm-sq	1
WELL.GATE.EX.1	Extension	Minimum horizontal extension of WELL past GATE (not cut by GCUT layer)	≥	7	nm	-
WELL.GATE.EX.2	Extension	Minimum vertical extension of WELL past GATE (not cut by GCUT layer) that does not interact with SRAMDRC	≥	7	nm	-

Table 3.2.1 WELL design rules.

NOTES

1. A WELL layer polygon with minimum vertical and horizontal widths constitutes a WELL layer polygon with minimum area.

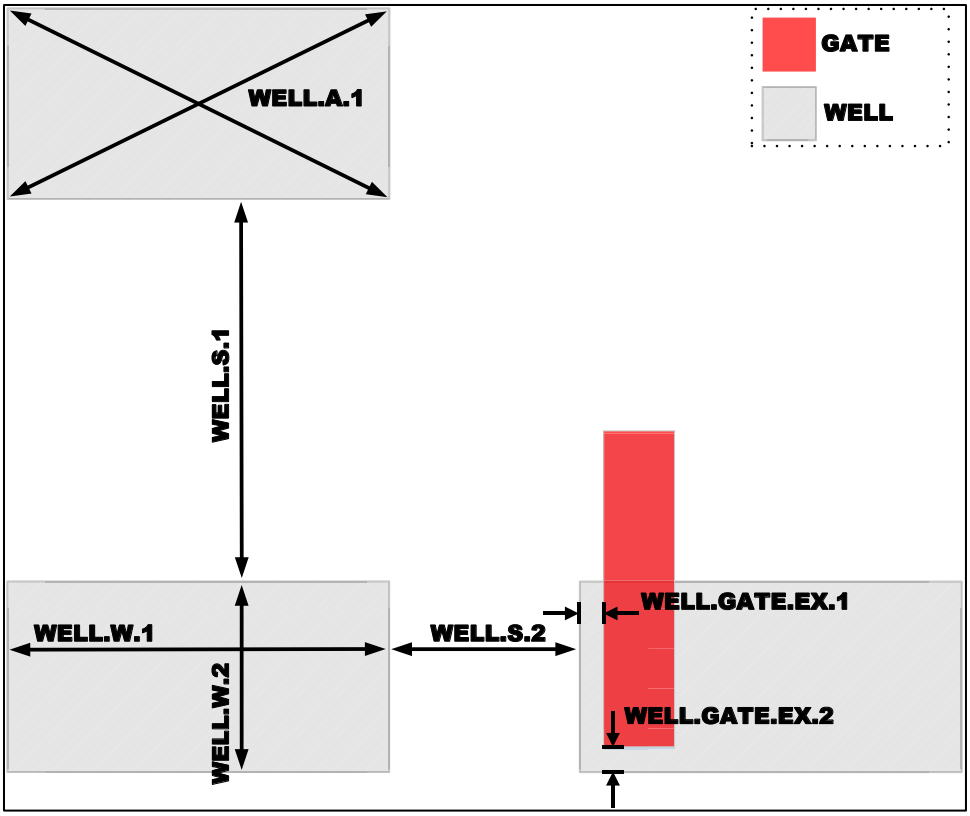

Fig. 3.2.1 Illustration of WELL design rules.

3.3 FIN Design Rules

Rule	Rule Type	Description	Operator	Value	Units	Notes
FIN.W.1	Width	Exact vertical FIN width	==	7	nm	-
FIN.W.2	Width	Minimum horizontal FIN width	≥	108	nm	-
FIN.S.1	Spacing	Exact vertical FIN pitch	==	27	nm	1
FIN.AUX.1	Auxiliary	FIN may not bend	-	-	-	-

Table 3.3.1 FIN design rules.

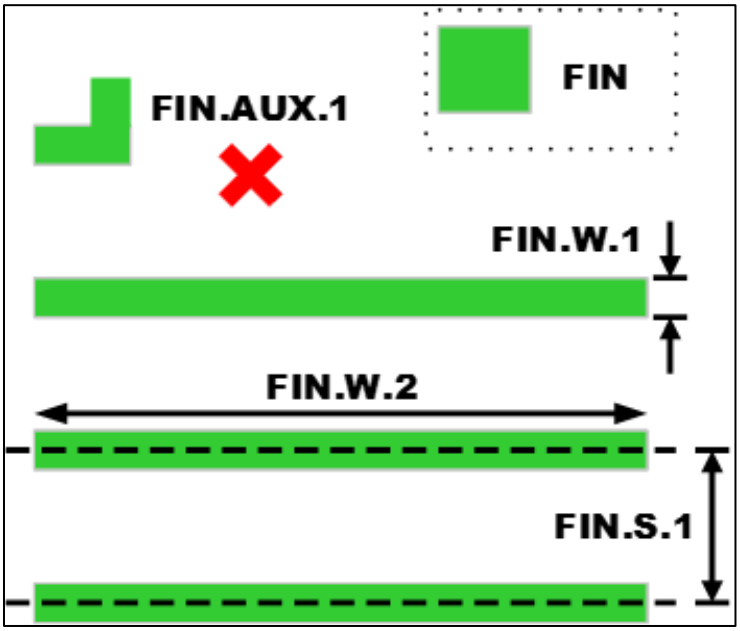

Fig. 3.3.1 Illustration of FIN design rules.

NOTES

1. When running hierarchical DRC, ensure that the FIN layer polygons have equal length along the x-axis.

3.4 GATE Design Rules

Rule	Rule Type	Description	Operator	Value	Units	Notes
GATE.W.1	Width	Exact horizontal GATE width	==	20	nm	-
GATE.W.2	Width	Minimum vertical GATE width	≥	40	nm	-
GATE.S.1	Spacing	Exact horizontal GATE pitch	==	54	nm	1
GATE.S.2	Spacing	Minimum horizontal GATE spacing	≥	34	nm	-
GATE.S.3	Spacing	Every GATE (not cut by GCUT and not interacting with the layer SRAMDRC) must have at least one other GATE within 54 nm of its surrounding along the horizontal axis. The spacing being the distance between centers of the two GATE layer polygons.	==	54	nm	-
GATE.AUX.1	Auxiliary	GATE may not bend	-	-	-	-
GATE.AUX.2	Auxiliary	GATE may not be discontinuous along the vertical axis. Use GCUT layer to mark cuts in the GATE	-	-	-	2,3
GATE.ACTIVE.AUX.3	Auxiliary	ACTIVE layer vertical edge may not lie inside, or coincide with, the GATE layer	-	-	-	-
GATE.ACTIVE.EX.1	Extension	Minimum vertical extension of GATE (not cut by GCUT) past ACTIVE	≥	4	nm	-
GATE.ACTIVE.EX.2	Extension	Minimum horizontal extension of ACTIVE interacting with GATE (not cut by GCUT layer) past GATE (not cut by GCUT layer)	≥	25	nm	-
GATE.ACTIVE.S.4	Spacing	Minimum horizontal spacing between ACTIVE and GATE (not cut by GCUT and not interacting with ACTIVE)	≥	9	nm	-

Table 3.4.1 GATE design rules.

NOTES

1. When running hierarchical DRC, ensure that the GATE layer polygons not cut by GCUT have equal length along the y-axis.
2. Referring to Fig. 3.4.2 (a), discontinuity—achieved by drawing two separate GATE layer polygons—in the layer GATE along vertical axis is not permitted. Instead, it is marked by the presence of the layer GCUT (see Fig. 3.4.2 (d)).
3. The terms ‘GATE cut by GCUT’ and ‘GATE not cut by GCUT’ have been used in this manual. Referring to Fig. 3.4.2 (d), the term ‘GATE cut by GCUT’ indicates the region formed by the intersection of layers GATE and GCUT (depicted by the rectangle with diagonal pattern fill), whereas the term ‘GATE not cut by GCUT’ refers to the GATE regions over which GCUT is not present.

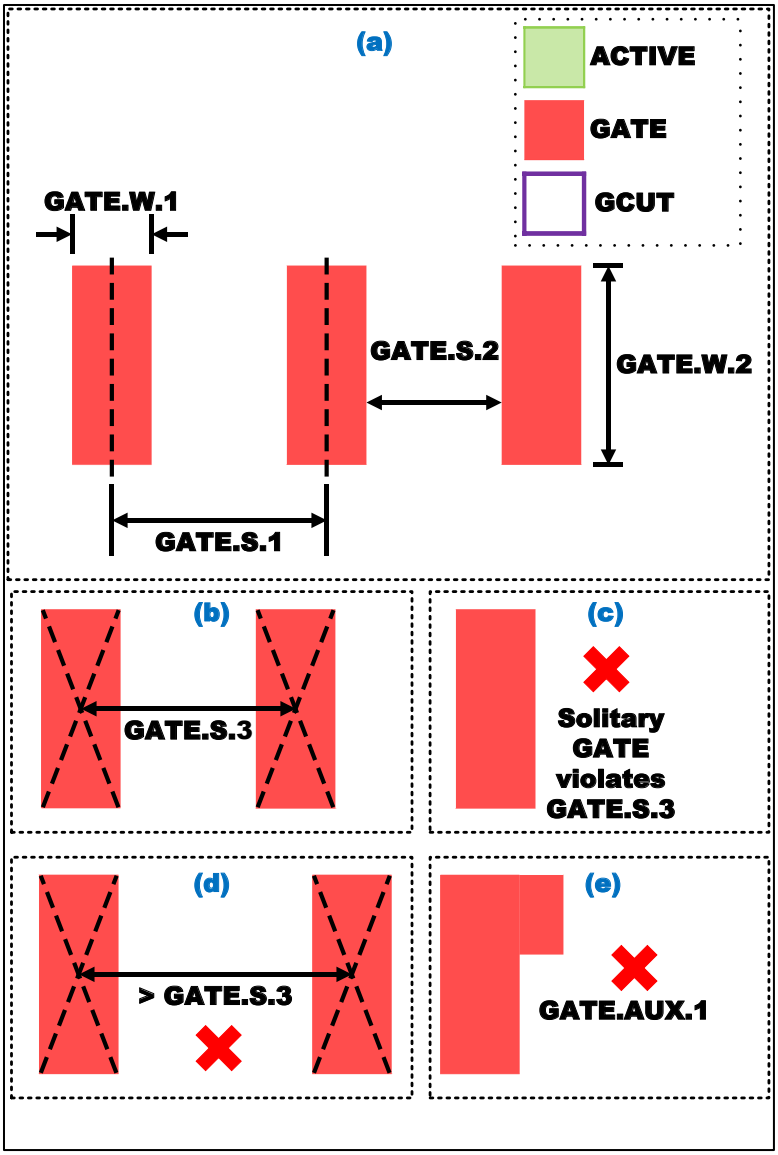

Fig. 3.4.1 Illustration of GATE design rules (1 of 2; see Fig. 3.4.2).

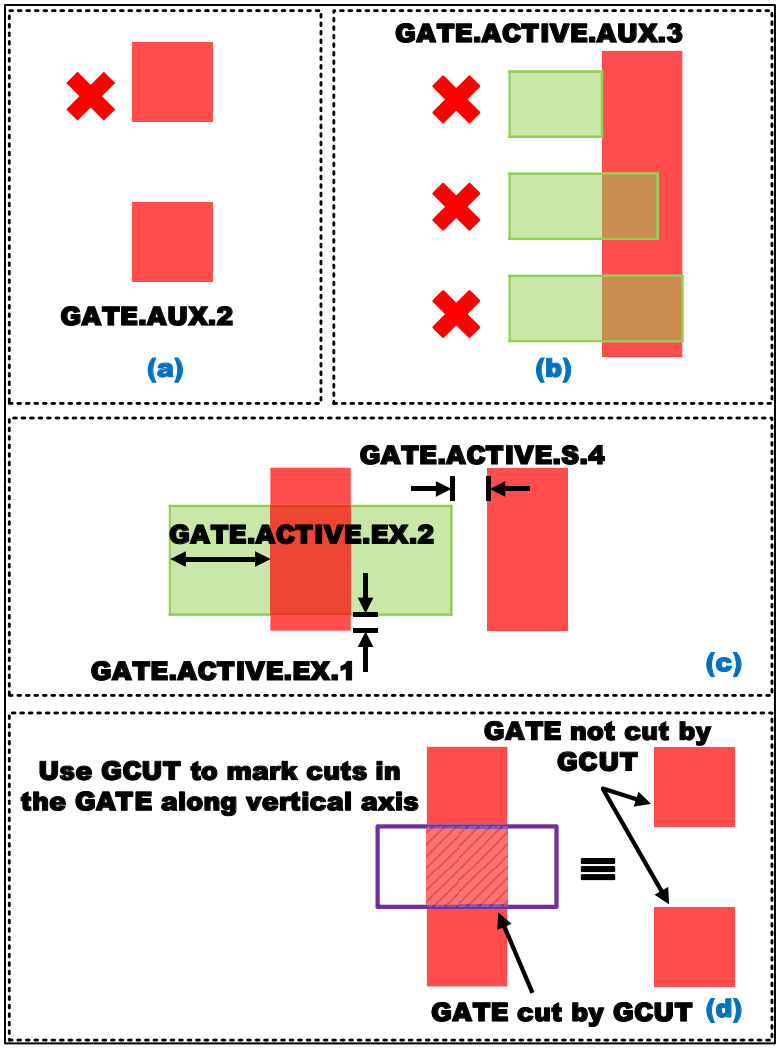

Fig. 3.4.2 Illustration of GATE design rules (2 of 2; see Fig. 3.4.1).

3.5 ACTIVE Design Rules

Rule	Rule Type	Description	Operator	Value	Units	Notes
ACTIVE.FIN.EX.1	Extension	Minimum vertical extension of ACTIVE past FIN	≥	10	nm	-
ACTIVE.W.1	Width	Minimum vertical width of ACTIVE	≥	27	nm	-
ACTIVE.W.2	Width	ACTIVE layer vertical width increment is an integer multiple of	==	27	nm	-
ACTIVE.W.3	Width	Minimum horizontal width of ACTIVE	≥	16	nm	-
ACTIVE.S.1	Spacing	Minimum vertical spacing of ACTIVE	≥	27	nm	-
ACTIVE.S.2A	Spacing	Minimum horizontal spacing between ACTIVE layers forming source/drain regions (of different transistors) on different nets	≥	92	nm	1,2
ACTIVE.S.2B	Spacing	Minimum horizontal spacing of ACTIVE	≥	38	nm	-
ACTIVE.WELL.S.4	Spacing	Minimum spacing of ACTIVE (outside the layer SRAMDRC) to WELL is	≥	27	nm	-
SRAM.ACTIVE.WELL.S.5	Spacing	Minimum spacing of ACTIVE (interacting with the layer SRAMDRC) to WELL is	≥	13.5	nm	-
ACTIVE.WELL.EN.1	Enclosure	Minimum enclosure of ACTIVE (outside the layer SRAMDRC) by WELL is	≥	27	nm	-
SRAM.ACTIVE.WELL.EN.2	Enclosure	Minimum enclosure of ACTIVE (interacting with the layer SRAMDRC) by WELL is	≥	13.5	nm	-

Table 3.5.1 Active design rules (1 of 2; see Table 3.5.2).

Rule	Rule Type	Description	Operator	Value	Units	Notes
ACTIVE.A.1A	Area	Minimum area of an ACTIVE layer polygon that does not interact with layer SRAMDRC	≥	864	nm-sq	-
ACTIVE.A.1B	Area	Minimum enclosed area of an ACTIVE layer polygon that does not interact with layer SRAMDRC	≥	864	nm-sq	-
SRAM.ACTIVE.A.2A	Area	Minimum area of an ACTIVE layer polygon that interacts with layer SRAMDRC	≥	432	nm-sq	-
SRAM.ACTIVE.A.2B	Area	Minimum enclosed area of an ACTIVE layer polygon that interacts with layer SRAMDRC	≥	432	nm-sq	-
ACTIVE.AUX.1	Auxiliary	ACTIVE must always be enclosed by NSELECT or PSELECT, such that no ACTIVE layer edge(s) coincide with NSELECT or PSELECT layer edge(s).	-	-	-	-
SRAM.ACTIVE.AUX.2	Auxiliary	ACTIVE layer polygons not belonging to an SRAM cell, i.e. those that are either completely outside the SRAMDRC layer or those that do not intersect the SRAMDRC layer, may not touch the SRAMDRC layer	-	-	-	-
ACTIVE.AUX.3	Auxiliary	A notch in ACTIVE along vertical axis is not allowed.	-	-	-	-
ACTIVE.LUP.1	Auxiliary	Maximum distance, to prevent latch-up, between ACTIVE forming a MOS device and ACTIVE forming a bulk/substrate contact within the same WELL/substrate	≤	30	um	-

Table 3.5.2 Active design rules (2 of 2; see Table 3.5.1).

NOTES

1. Known Issue: At present, the DRC deck does not support the rule ACTIVE.S.2A for ACTIVE layer polygons (forming source/drain) interacting with the layer SRAMDRC. Regardless of this, the rule must be followed for ACTIVE layer polygons (forming source/drain) interacting with the layer SRAMDRC as well.
2. Known Issue: This rule erroneously checks for vertical spacing between ACTIVE layer polygons (forming source/drain), when it is only intended for checking the horizontal spacing. Any violations associated with this DRC may be waived, if vertical spacing is being checked.

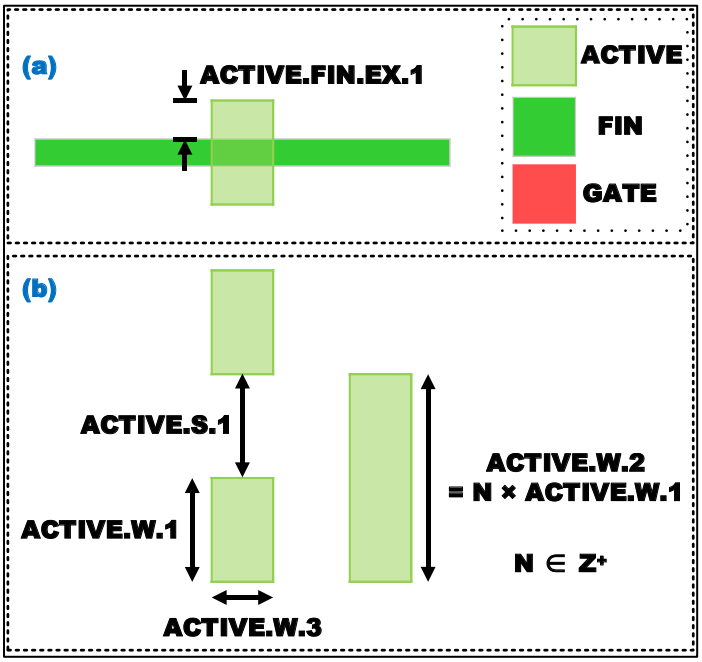

Fig. 3.5.1 Illustration of ACTIVE design rules (1 of 4; see Fig. 3.5.2, Fig. 3.5.3, and Fig. 3.5.4).

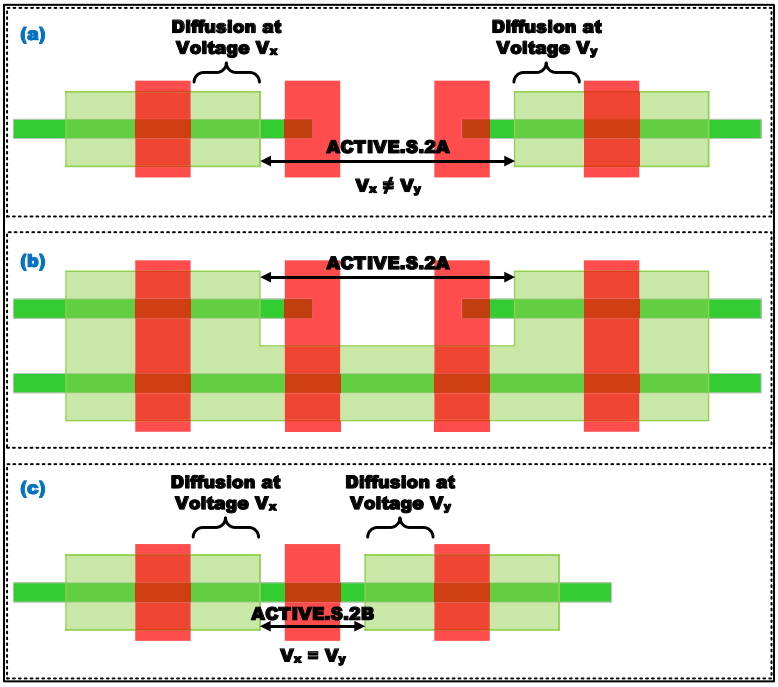

Fig. 3.5.2 Illustration of ACTIVE design rules (2 of 4; see Fig. 3.5.1, Fig. 3.5.3, and Fig. 3.5.4).

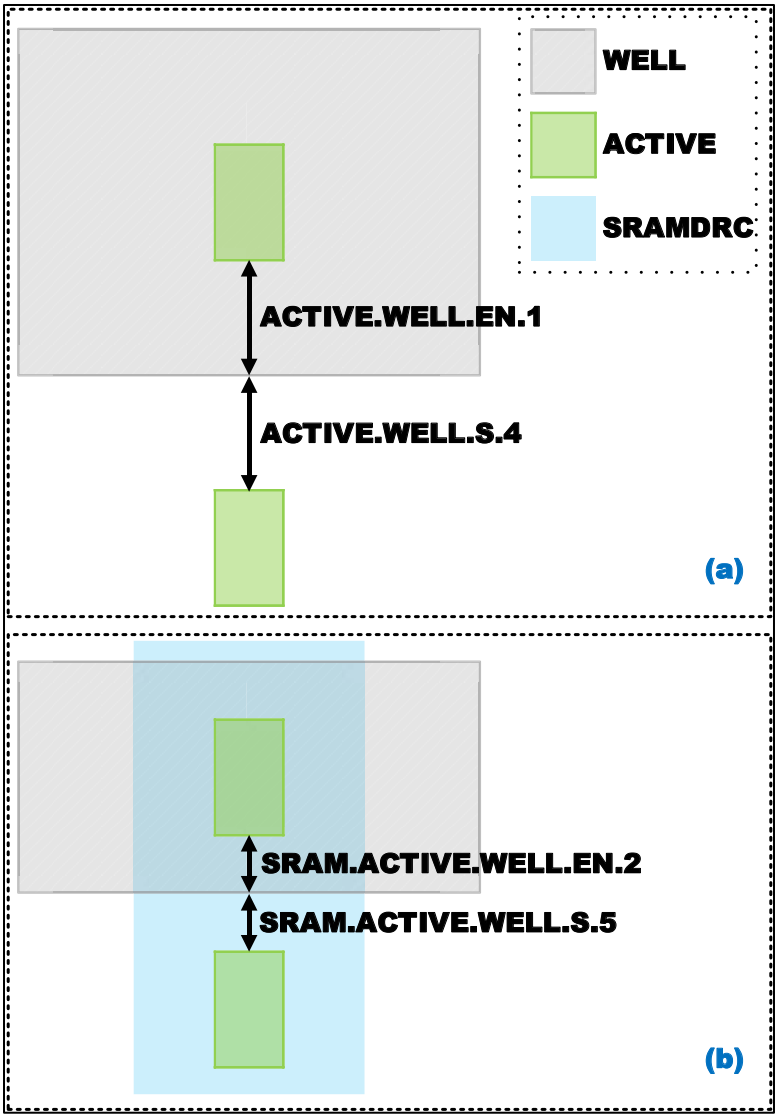

Fig. 3.5.3 Illustration of ACTIVE design rules (3 of 4; see Fig. 3.5.1, Fig. 3.5.2, and Fig. 3.5.4).

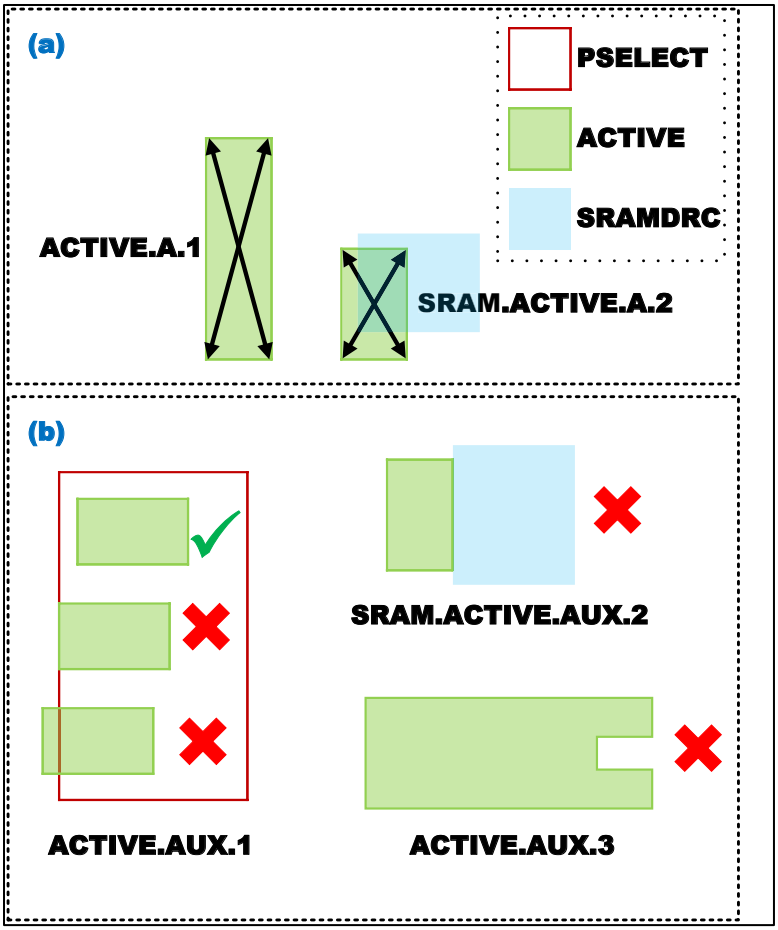

Fig. 3.5.4 Illustration of ACTIVE design rules (4 of 4; see Fig. 3.5.1, Fig. 3.5.2, and Fig. 3.5.3).

3.6 GCUT Design Rules

Rule	Rule Type	Description	Operator	Value	Units	Notes
GCUT.W.1	Width	Minimum vertical width of GCUT	≥	17	nm	-
GCUT.ACTIVE.S.1	Spacing	Minimum vertical spacing between GCUT and channel	≥	4	nm	-
GCUT.GATE.EX.1	Extension	Minimum horizontal extension of GCUT past GATE	≥	17	nm	-
GCUT.GATE.S.2	Spacing	Minimum spacing of GCUT to GATE, when the former is not being used to cut a particular polygon drawn using the latter	≥	17	nm	-
GCUT.S.3	Spacing	Minimum vertical spacing between two GCUT layer polygons	≥	35	nm	-
GCUT.AUX.1	Auxiliary	GCUT layer may not exist without the layer GATE.	-	-	-	-
GCUT.AUX.2	Auxiliary	GCUT layer vertical edge may not lie inside, or coincide with, the GATE layer	-	-	-	1
GCUT.AUX.3	Auxiliary	GCUT may not interact with channel.	-	-	-	-

Table 3.6.1 GCUT design rules.

NOTES

1. This rule ensures that a GATE layer polygon is not cut along the horizontal axis by an amount that is smaller than the minimum horizontal GATE width.

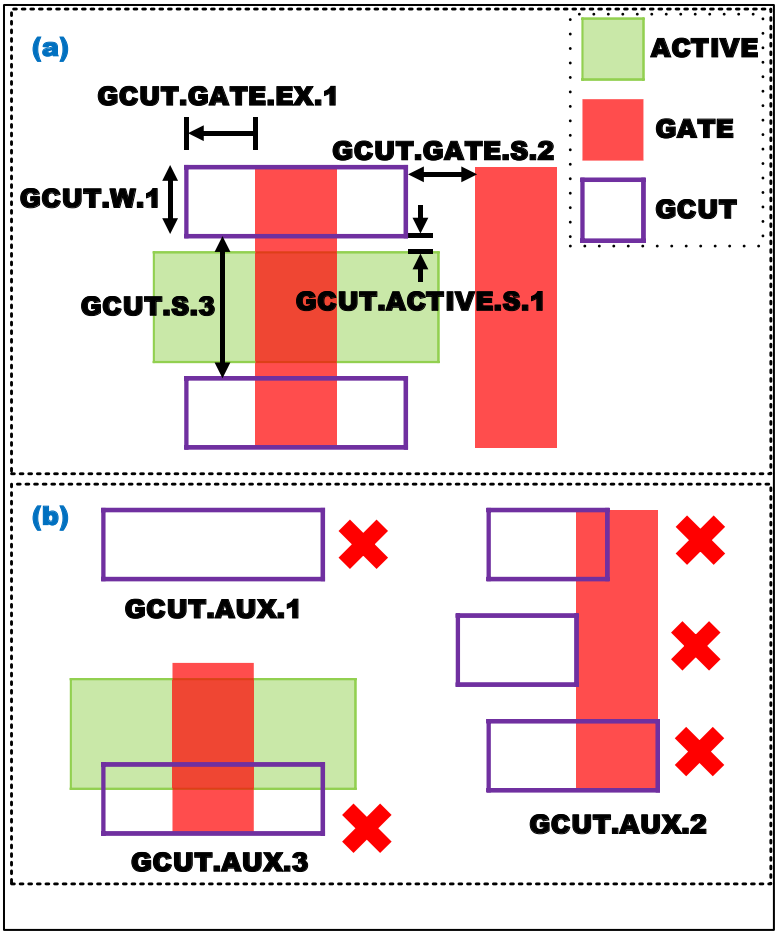

Fig. 3.6.1 Illustration of GCUT design rules.

3.7 NSELECT/PSELECT/SLVT/LVT/SRAMVT Design Rules

Unless otherwise stated, assume that the rules listed in this section apply to the layers PSELECT, SLVT, LVT, and SRAMVT as well.

Rule	Rule Type	Description	Operator	Value	Units	Notes
NSELECT.W.1	Width	Minimum horizontal width of NSELECT	≥	108	nm	-
NSELECT.W.2	Width	Minimum vertical width of NSELECT	≥	54	nm	-
NSELECT.ACTIVE.EN.1	Enclosure	Minimum horizontal enclosure of ACTIVE (not interacting with SRAMDRC) by NSELECT	≥	46	nm	-
NSELECT.ACTIVE.EN.2	Enclosure	Minimum vertical enclosure of ACTIVE (not interacting with SRAMDRC) by NSELECT	≥	27	nm	-
SRAM.NSELECT.ACTIVE.EN.3	Enclosure	Minimum horizontal enclosure of ACTIVE (interacting with SRAMDRC) by NSELECT	≥	13.5	nm	-
SRAM.NSELECT.ACTIVE.EN.4	Enclosure	Minimum vertical enclosure of ACTIVE (interacting with SRAMDRC) by NSELECT	≥	13.5	nm	-
NSELECT.GATE.EX.1	Extension	Minimum horizontal extension of NSELECT past GATE (not cut by GCUT)	≥	7	nm	-
NSELECT.GATE.EX.2	Extension	Minimum vertical extension of NSELECT past GATE (not cut by GCUT)	≥	7	nm	-
NSELECT.PSELECT.AUX.1	Auxiliary	NSELECT and PSELECT may not overlap	-	-	-	1
VT.AUX.2	Auxiliary	VT layers (LVT, SLVT, and SRAMVT) may not overlap	-	-	-	-

Table 3.7.1 NSELECT/PSELECT/SLVT/LVT/SRAMVT design rules.

NOTES

1. The rule is not applicable to SLVT, LVT, and SRAMVT.

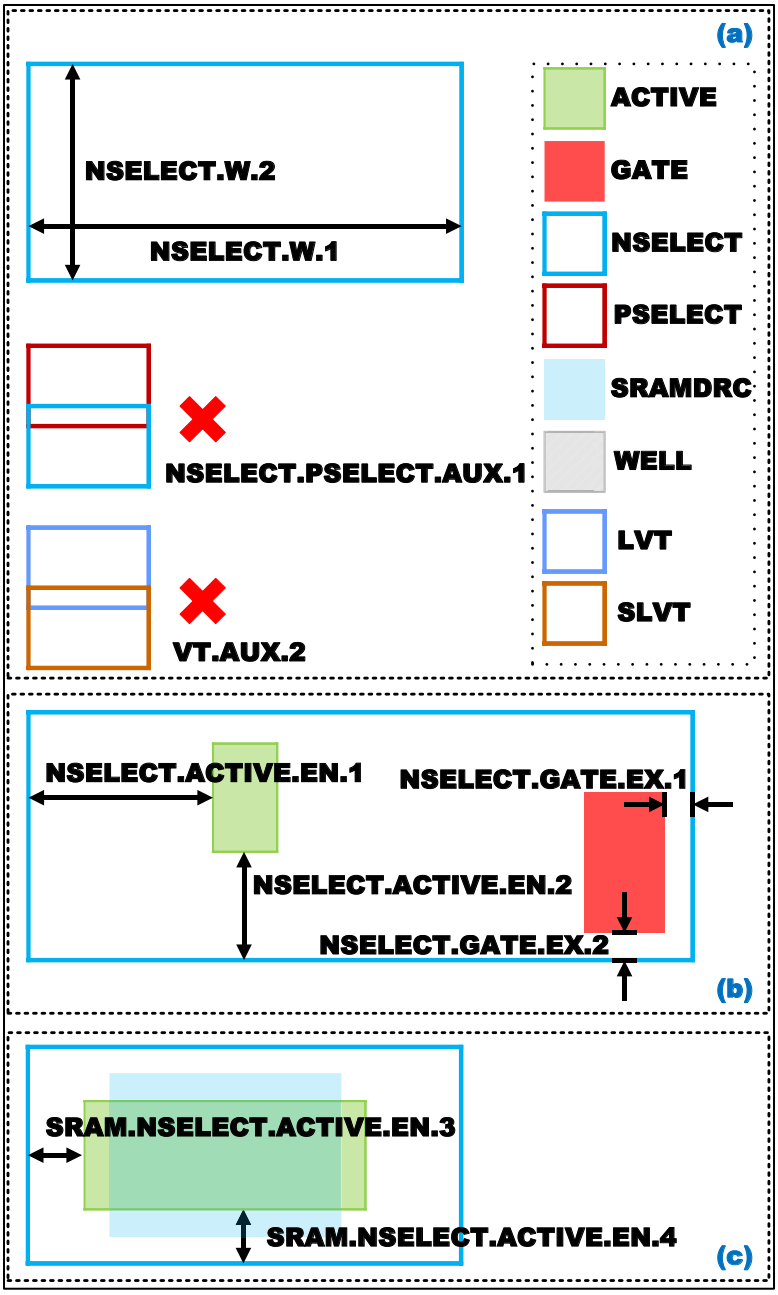

Fig. 3.7.1 Illustration of NSELECT/PSELECT/SLVT/LVT/SRAMVT design rules.

3.8 SDT Design Rules

Rule	Rule Type	Description	Operator	Value	Units	Notes
SDT.W.1	Width	Minimum horizontal width of SDT	≥	24	nm	-
SDT.W.2	Width	Minimum vertical width of SDT (not interacting with SRAMDRC)	≥	27	nm	-
SDT.W.3	Width	SDT (not interacting with SRAMDRC) layer vertical width increment is an integer multiple of	==	27	nm	-
SRAM.SDT.W.4	Width	Minimum vertical width of SDT (interacting with SRAMDRC)	≥	17	nm	-
SDT.S.1	Spacing	Minimum horizontal spacing between two SDT layer polygons	≥	30	nm	-
SDT.GATE.S.2	Spacing	Minimum horizontal spacing between SDT and GATE	≥	5	nm	-
SDT.ACTIVE.OV.1	Overlap	Minimum vertical overlap between SDT and ACTIVE	≥	27	nm	-
SDT.LISD.OV.2	Overlap	Minimum vertical overlap between SDT and LISD	≥	27	nm	-
SRAM.SDT.ACTIVE.OV.3	Overlap	Minimum vertical overlap between SDT (interacting with SRAMDRC) and ACTIVE	≥	17	nm	-
SRAM.SDT.LISD.OV.4	Overlap	Minimum vertical overlap between SDT (interacting with SRAMDRC) and LISD	≥	17	nm	-
SDT.GATE.AUX.1	Auxiliary	SDT and GATE may not overlap or touch	-	-	-	-
SDT.ACTIVE.AUX.2	Auxiliary	SDT (not interacting with SRAMDRC) horizontal edges must coincide with ACTIVE horizontal edges	-	-	-	-
SDT.ACTIVE.AUX.3	Auxiliary	SDT may not be entirely outside ACTIVE	-	-	-	-
SDT.LISD.AUX.4	Auxiliary	SDT must always be inside LISD	-	-	-	-

Table 3.8.1 SDT design rules.

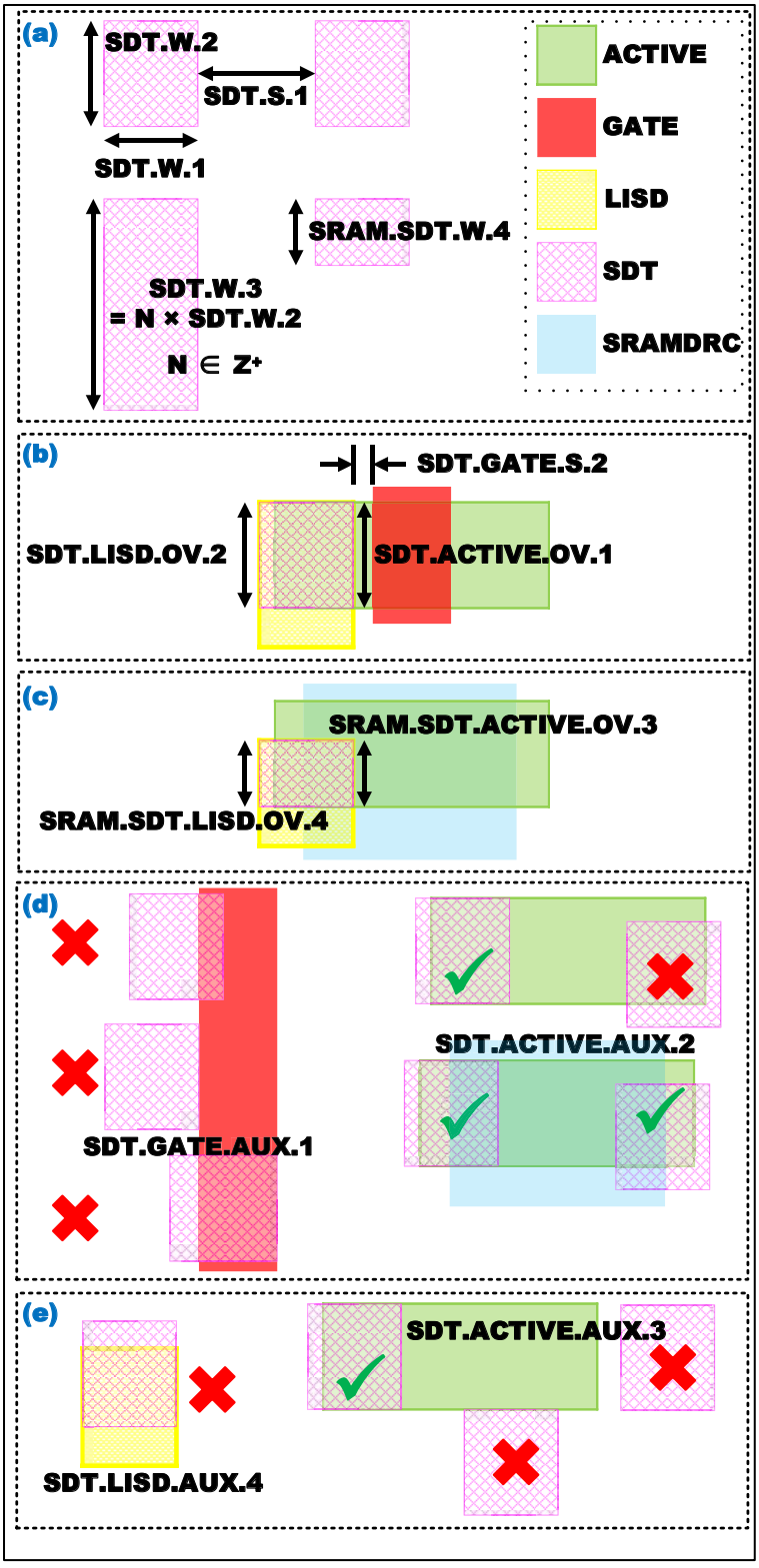

Fig. 3.8.1 Illustration of SDT design rules.

3.9 LISD Design Rules

Rule	Rule Type	Description	Operator	Value	Units	Notes
LISD.W.1	Width	Minimum width of LISD	≥	24	nm	-
LISD.S.1	Spacing	Minimum (side-to-side) spacing between two LISD layer polygons' edges, when both edges are > 36 nm	≥	18	nm	-
LISD.S.2	Spacing	Minimum (tip-to-side) spacing between two LISD layer polygons' edges, when one edge is <= 36 nm and the other edge is > 36 nm	≥	25	nm	-
LISD.S.3	Spacing	Minimum (tip-to-tip) spacing between two LISD layer polygons' (lying completely outside the layer SRAMDRC) edges, when both edges are >= 24 nm and <=36 nm	≥	27	nm	-
SRAM.LISD.S.4	Spacing	Minimum (tip-to-tip) spacing between two LISD layer polygons' (interacting with the layer SRAMDRC) edges, when both edges are <= 36 nm	≥	27	nm	-
LISD.A.1	Area	Minimum LISD area	≥	648	nm-sq	-
SRAM.LISD.AUX.1	Auxiliary	LISD layer polygons, which are either completely outside the SRAMDRC layer or which do not intersect the SRAMDRC layer, may not touch the SRAMDRC layer.	-	-	-	-

Table 3.9.1 LISD design rules.

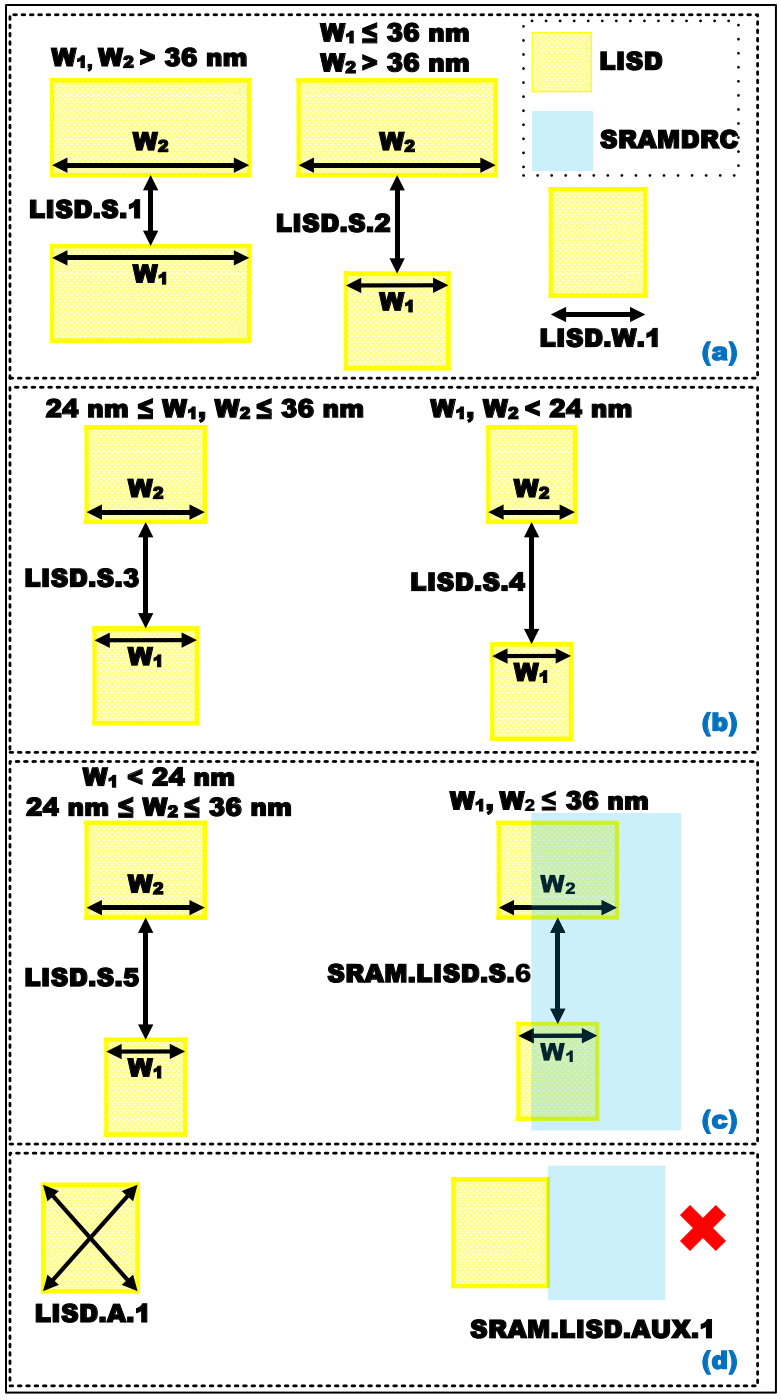

Fig. 3.9.1 Illustration of LISD design rules.

3.10 LIG Design Rules

Rule	Rule Type	Description	Operator	Value	Units	Notes
LIG.W.1	Width	Minimum width of LIG	≥	16	nm	-
LIG.S.1	Spacing	Minimum (side-to-side) spacing between two LIG layer polygons' edges, when both edges are > 36 nm	≥	18	nm	-
LIG.S.2	Spacing	Minimum (tip-to-side) spacing between two LIG layer polygons' edges, when one edge is <= 36 nm and the other edge is > 36 nm	≥	25	nm	-
LIG.S.3	Spacing	Minimum (tip-to-tip) spacing between two LIG layer polygons' (lying completely outside the layer SRAMDRC) edges, when both edges are >= 24 nm and <= 36 nm	≥	27	nm	-
LIG.S.4	Spacing	Minimum (tip-to-tip) spacing between two LIG layer polygons' (lying completely outside the layer SRAMDRC) edges, when both edges are < 24 nm	≥	31	nm	-
LIG.S.5	Spacing	Minimum (tip-to-tip) spacing between two LIG layer polygons' (lying completely outside the layer SRAMDRC) edges, when one of the edges is >= 24 nm and <= 36 nm, and the other is < 24 nm	≥	31	nm	-
LIG.LISD.S.6	Spacing	Minimum spacing between LIG and LISD layer polygons not on the same net	≥	14	nm	-
LIG.LISD.S.7	Spacing	Minimum corner-to-corner spacing between LISD and LIG not on the same net	≥	15	nm	-
LIG.SDT.S.8	Spacing	Minimum spacing between LIG and SDT layer polygons not on the same net	≥	14	nm	-

Table 3.10.1 LIG design rules (1 of 3; see Table 3.10.2 and Table 3.10.3).

Rule	Rule Type	Description	Operator	Value	Units	Notes
LIG.GATE.S.9A	Spacing	Minimum vertical spacing between LIG and GATE (not cut using GCUT) layer polygons	≥	14	nm	-
LIG.GATE.S.9B	Spacing	Minimum horizontal spacing between LIG and GATE (not cut using GCUT) layer polygons	≥	17	nm	-
LIG.GATE.S.10	Spacing	Minimum spacing between LIG and GATE (not cut using GCUT) forming a channel (GATE layer polygon over ACTIVE)	≥	5	nm	-
LIG.GCUT.S.11	Spacing	Minimum vertical spacing between LIG and GCUT	≥	5	nm	-
LIG.A.1	Area	Minimum LIG area	≥	324	nm-sq	-
LIG.LISD.A.2	Area	Minimum area of overlap between LIG and LISD	≥	128	nm-sq	-
LIG.GATE.A.3	Area	Minimum area of overlap between LIG (lying completely outside the layer SRAMDRC) and GATE (not cut using GCUT)	≥	320	nm-sq	-
SRAM.LIG.GATE.A.4	Area	Minimum area of overlap between LIG (interacting with the layer SRAMDRC) and GATE (not cut using GCUT)	≥	240	nm-sq	-
LIG.GATE.AUX.1	Auxiliary	LIG layer (lying completely outside the layer SRAMDRC) vertical edge may not lie inside, or coincide with, the GATE layer	-	-	-	-

Table 3.10.2 LIG design rules (2 of 3; see Table 3.10.1 and Table 3.10.3).

Rule	Rule Type	Description	Operator	Value	Units	Notes
SRAM.LIG.AUX.2	Auxiliary	LIG layer polygons, which are either completely outside the SRAMDRC layer or which do not intersect the SRAMDRC layer, may not touch the SRAMDRC layer	-	-	-	-
LIG.GATE.EX.1	Extension	Minimum extension of LIG (lying completely outside the layer SRAMDRC) over GATE (not cut using GCUT) on both opposite sides	≥	1	nm	-
LIG.LISD.OV.1	Overlap	Minimum overlap between LIG and LISD connected together	≥	8	nm	-
SRAM.LIG.GATE.OV.2	Overlap	Minimum overlap of LIG (interacting with the layer SRAMDRC) and GATE (not cut using GCUT)	≥	15	nm	-

Table 3.10.3 LIG design rules (3 of 3; see Table 3.10.1 and Table 3.10.2).

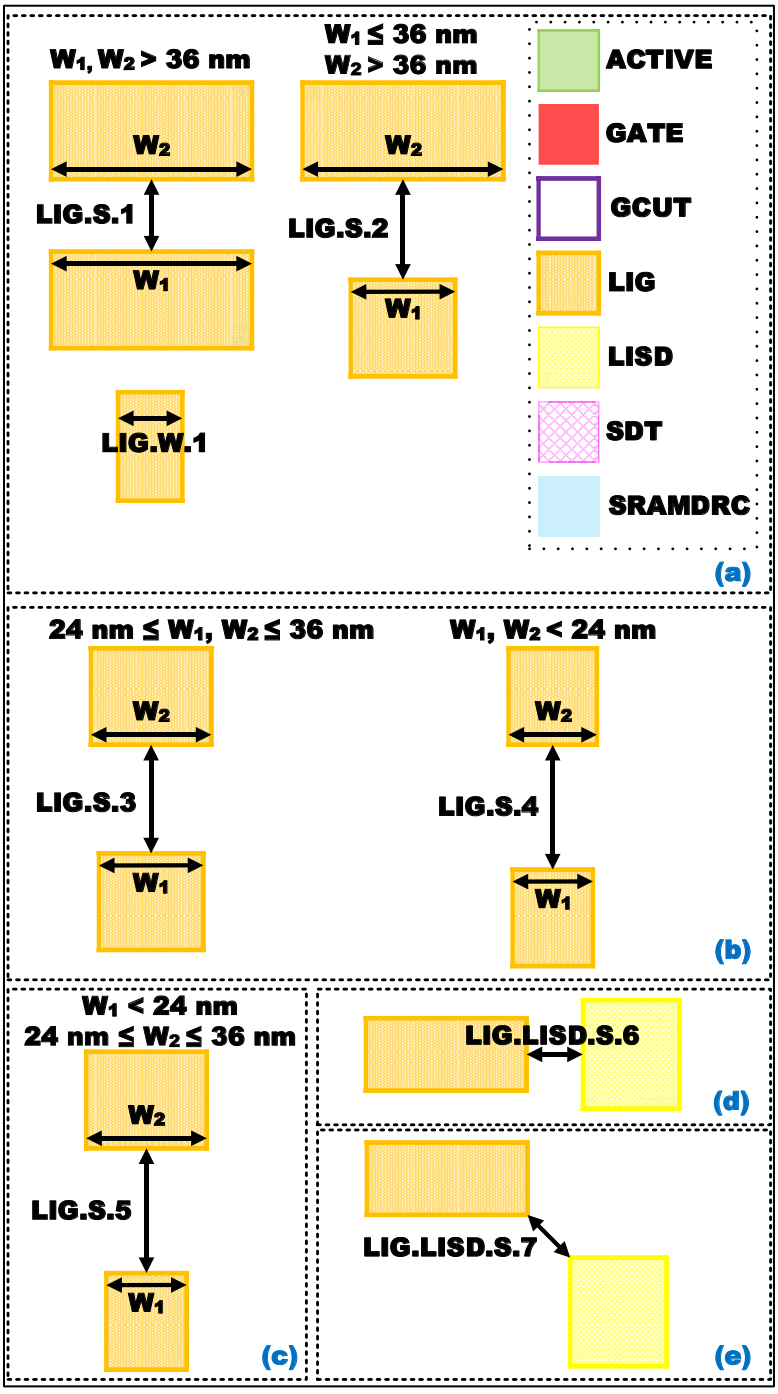

Fig. 3.10.1 Illustration of LIG design rules (1 of 2; see Fig. 3.10.2).

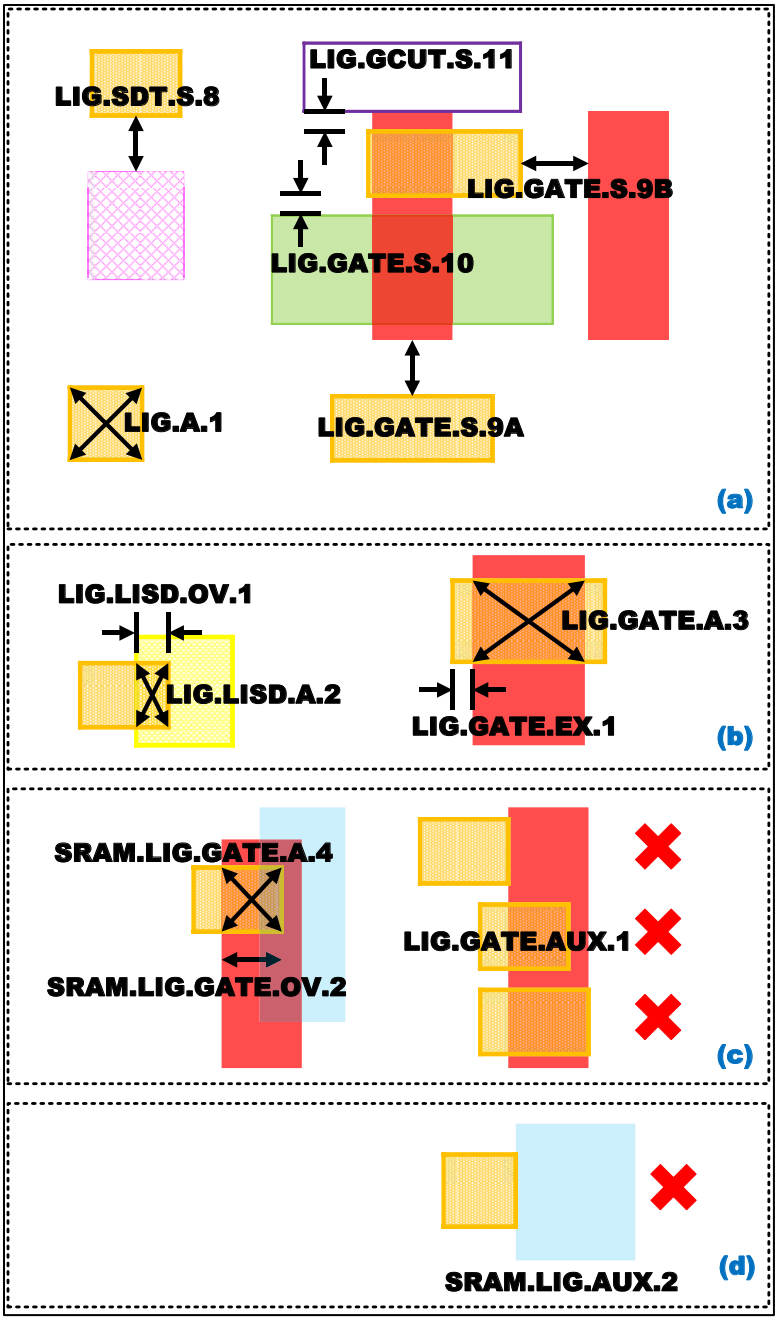

Fig. 3.10.2 Illustration of LIG design rules (2 of 2; see Fig. 3.10.1).

3.11 V0 Design Rules

Rule	Rule Type	Description	Operator	Value	Units	Notes
V0.W.1	Width	Minimum width of a V0 instance along the length of M1	≥	18	nm	-
V0.S.1	Spacing	Minimum spacing between V0 instances [on the same M1 track | on parallel M1 tracks, if they are not aligned with each other | on parallel M1 tracks, if they are fully or partially aligned with each other]	≥	[18 nm | 27 nm | 18 nm]	nm	1
V0.S.2	Spacing	Minimum corner-to-corner spacing between two V0 instances—both with a 5 nm M1 end-cap	≥	23	nm	-
V0.S.3	Spacing	Minimum corner-to-corner spacing between two V0 instances—both without a 5 nm M1 end-cap	≥	30	nm	-
V0.S.4	Spacing	Minimum corner-to-corner spacing between two V0 instances—one with and another without, a 5 nm M1 end-cap	≥	27	nm	-
V0.M1.EN.1	Enclosure	Minimum enclosure of V0 by M1 on two opposite sides	≥	(5 & 5) | (5 & 0)	nm	-

Table 3.11.1 V0 design rules (1 of 2; see Table 3.11.2).

Rule	Rule Type	Description	Operator	Value	Units	Notes
V0.LISD.EN.2	Enclosure	Minimum enclosure of V0 (interacting with LISD, but not with LIG) by LISD on at least two opposite sides is 3 nm and such a V0 must lie completely inside LISD.	==	3	nm	-
V0.LISD.EN.3	Enclosure	Minimum enclosure of V0 (sharing some, but not all its area with LISD) by LISD (interacting with LIG) on at least two opposite sides is 3 nm and such a V0 does not need to lie completely inside LISD.	==	3	nm	-
V0.LIG.EN.4	Enclosure	Minimum enclosure of LIG by V0 (interacting with LIG and not inside LISD) on two opposite sides is 1 nm.	≥	1	nm	-
V0.LIG.A.1	Area	Minimum area of overlap between V0 (interacting with LIG and not inside LISD) and LIG is 288 nm-sq.	≥	288	nm-sq	-
V0.AUX.1	Auxiliary	V0 must always interact with M1 and [LISD|LIG]	-	-	-	-
V0.LIG.AUX.2	Auxiliary	An instance of V0 (interacting with LIG but not inside LIG and not inside LISD) with an edge (parallel to the LIG length) lying inside, or touching LIG, is not permitted.	-	-	-	-
V0.M1.AUX.3	Auxiliary	V0 must exactly be the same width as M1 along the direction perpendicular to the M1 length	-	-	-	-

Table 3.11.2 V0 design rules (2 of 2; see Table 3.11.1).

NOTES

1. The lower bound in the last case will be set by M1, precluding any occurrence of V0 instances at a distance smaller than the minimum spacing between M1.

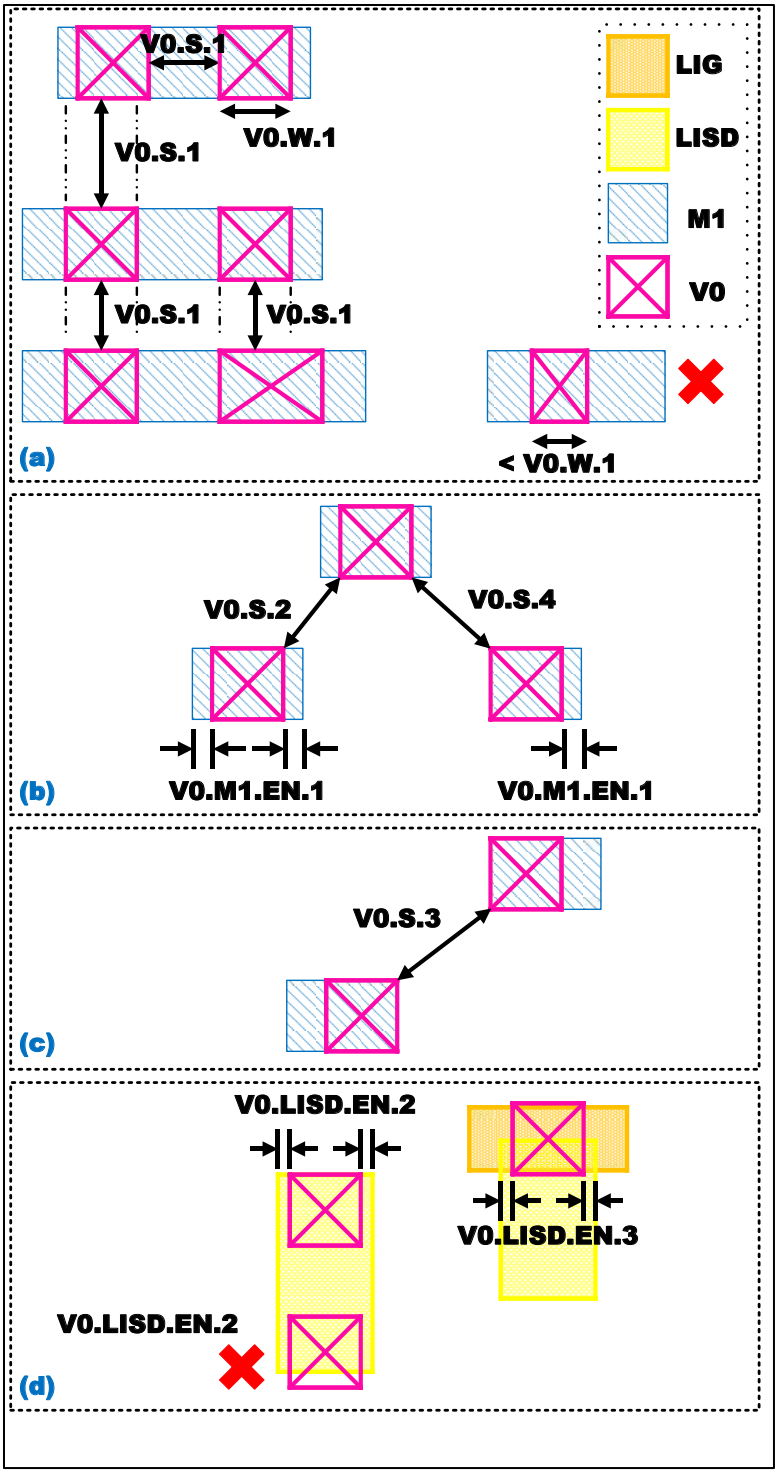

Fig. 3.11.1 Illustration of V0 design rules (1 of 2; see Fig. 3.11.2).

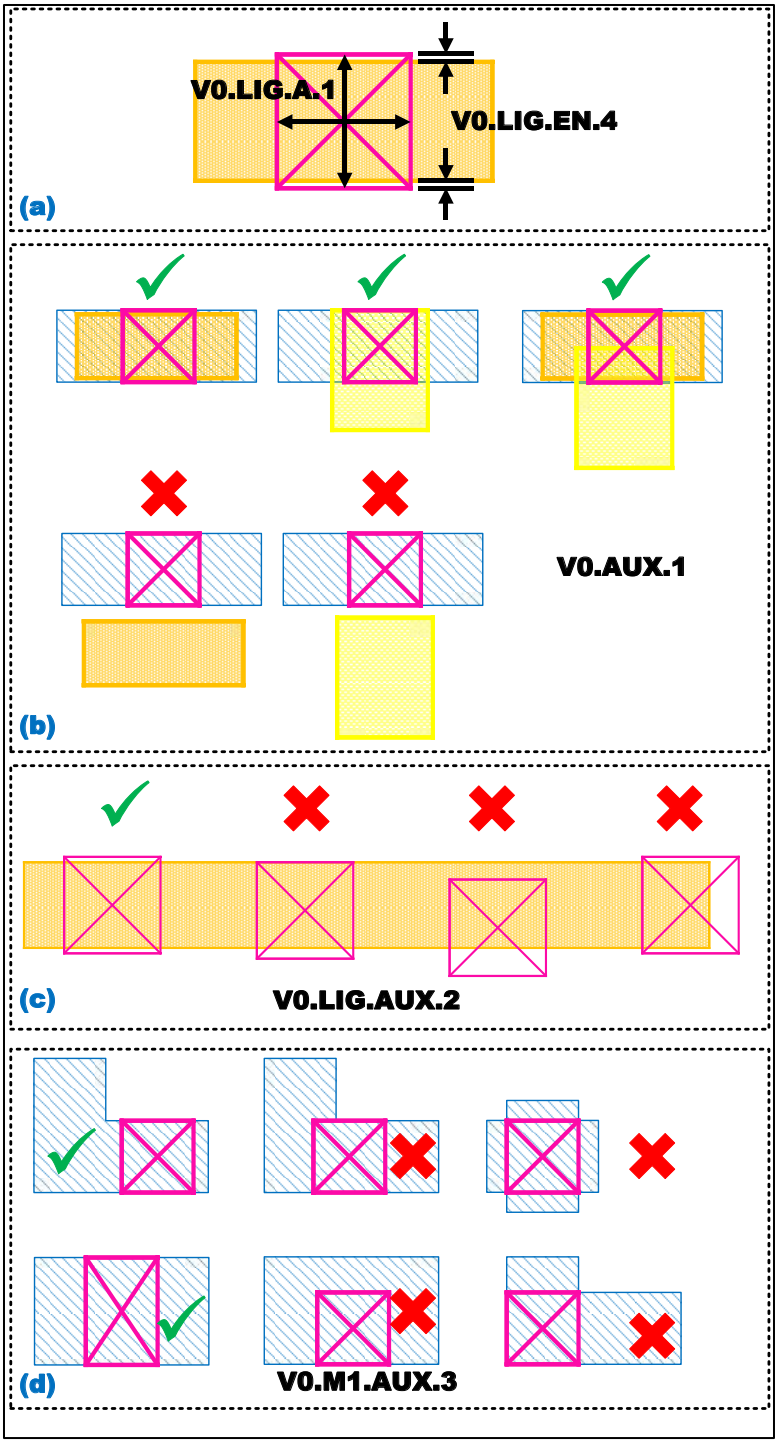

Fig. 3.11.2 Illustration of V0 design rules (2 of 2; see Fig. 3.11.1).

3.12 M1-M3 Design Rules

Unless otherwise stated, assume that the rules listed in this section for M1, apply to M2 and M3 as well.

Rule	Rule Type	Description	Operator	Value	Units	Notes
M1.W.1	Width	Minimum width of M1	≥	18	nm	-
M1.S.1	Spacing	Minimum (side-to-side) spacing between two M1 layer polygons' edges, when both edges are > 36 nm	≥	18	nm	-
M1.S.2	Spacing	Minimum (tip-to-side) spacing between two M1 layer polygons' edges, when one of the edges is <= 36 nm and the other is > 36 nm	≥	25	nm	-
M1.S.3	Spacing	Minimum (tip-to-tip) spacing between two M1 layer polygons' edges, when both edges are >= 24 nm and <= 36 nm	≥	27	nm	-
M1.S.4	Spacing	Minimum (tip-to-tip) spacing between two M1 layer polygons' edges, when both edges are < 24 nm	≥	31	nm	-
M1.S.5	Spacing	Minimum (tip-to-tip) spacing between two M1 layer polygons' edges, when one of the edges is >= 24 nm and <= 36 nm, and the other is < 24 nm	≥	31	nm	-
M1.S.6	Spacing	Minimum corner-to-corner spacing between two M1 polygons	≥	20	nm	-
M1.A.1	Area	Minimum M1 area	≥	504	nm-sq	-

Table 3.12.1 M1-M3 design rules.

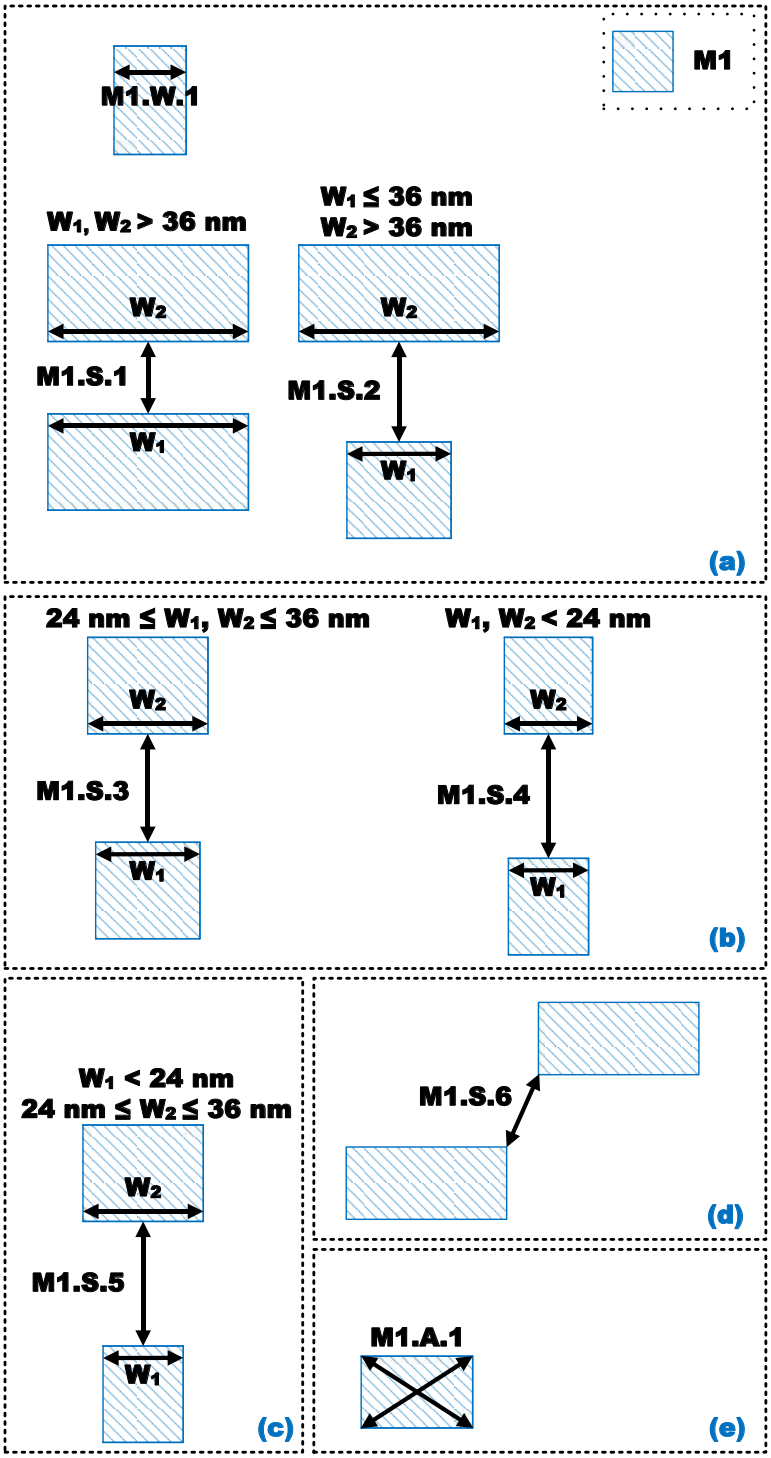

Fig. 3.12.1 Illustration of M1-M3 design rules.

3.13 V1-V3 Design Rules

Unless otherwise stated, assume that the rules listed in this section for V1—either for V1 alone or for V1 in conjunction with M1 or M2—apply to V(x) as well, whether it is for V(x) alone or for V(x) in conjunction with M(x) or M(x+1), where x=2, 3.

Rule	Rule Type	Description	Operator	Value	Units	Notes
V1.W.1	Width	Minimum width of a V1 instance along the length of M2	≥	18	nm	-
V1.S.1	Spacing	Minimum spacing between V1 instances [on the same M2 track | on parallel M2 tracks, if they are not aligned with each other | on parallel M2 tracks, if they are fully or partially aligned with each other]	≥	[18 | 27 | 18]	nm	1
V1.S.2	Spacing	Minimum corner-to-corner spacing between two V1 instances—both with a 5 nm M2 end-cap	≥	23	nm	-
V1.S.3	Spacing	Minimum corner-to-corner spacing between two V1 instances—both without a 5 nm M2 end-cap	≥	30	nm	-
V1.S.4	Spacing	Minimum corner-to-corner spacing between two V1 instances—one with and another without, a 5 nm M2 end-cap	≥	27	nm	-
V1.M1.EN.1	Enclosure	Minimum enclosure of V1 by M1 on two opposite sides	≥	5 & 2	nm	-
V2.M2.EN.1	Enclosure	Minimum enclosure of V2 by M2 on at least two opposite sides	≥	5	nm	2
V1.M2.EN.2	Enclosure	Minimum enclosure of V1 by M2 on two opposite sides	≥	(5 & 5) | (5 & 0)	nm	-
V3.M4.EN.2	Enclosure	Minimum enclosure of V3 by M4 on at least two opposite sides	≥	11	nm	-
V1.AUX.1	Enclosure	V1 must be inside M1 and M2	-	-	-	-
V1.M2.AUX.2	Auxiliary	V1 must exactly be the same width as M2 along the direction perpendicular to the M2 length	-	-	-	-

Table 3.13.1 V1-V3 design rules.

NOTES

1. The lower bound in the last case will be set by M2, precluding any occurrence of V1 instances at a distance smaller than the minimum spacing between M2.
2. V3.M3.EN.1 is similar to V2.M2.EN.1. It stipulates that the minimum enclosure of V3 by M3 on at least two opposite sides be 5 nm.

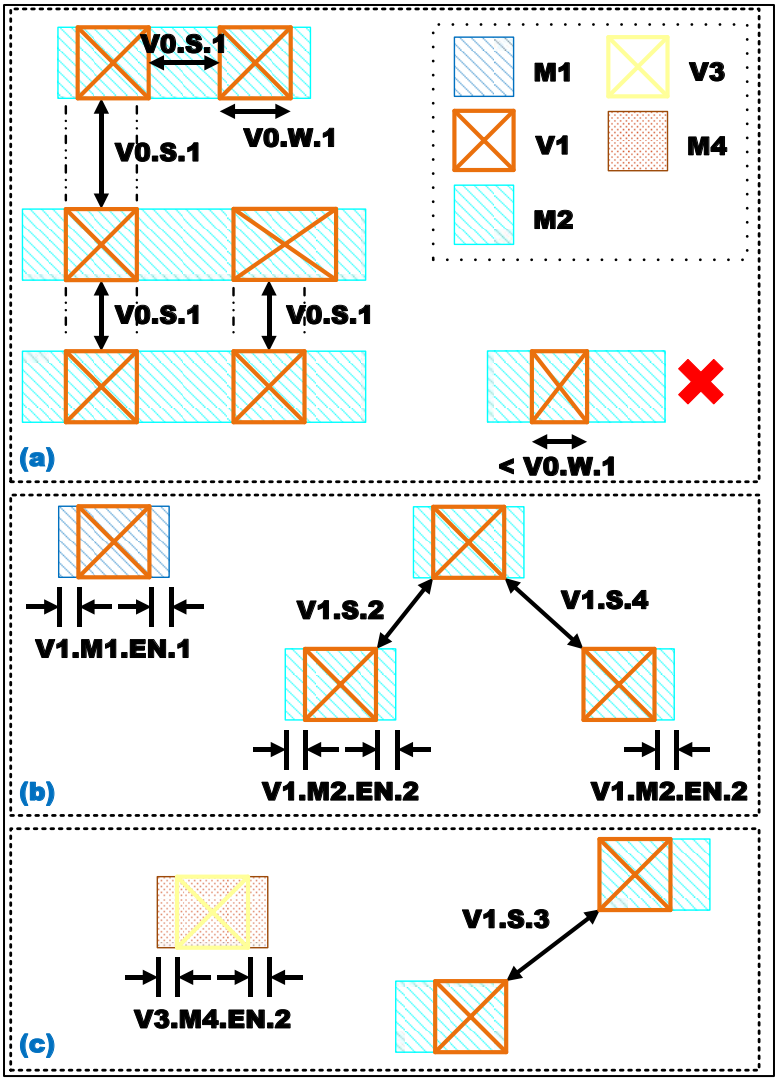

Fig. 3.13.1 Illustration of V1-V3 design rules (1 of 2; see Fig. 3.13.2).

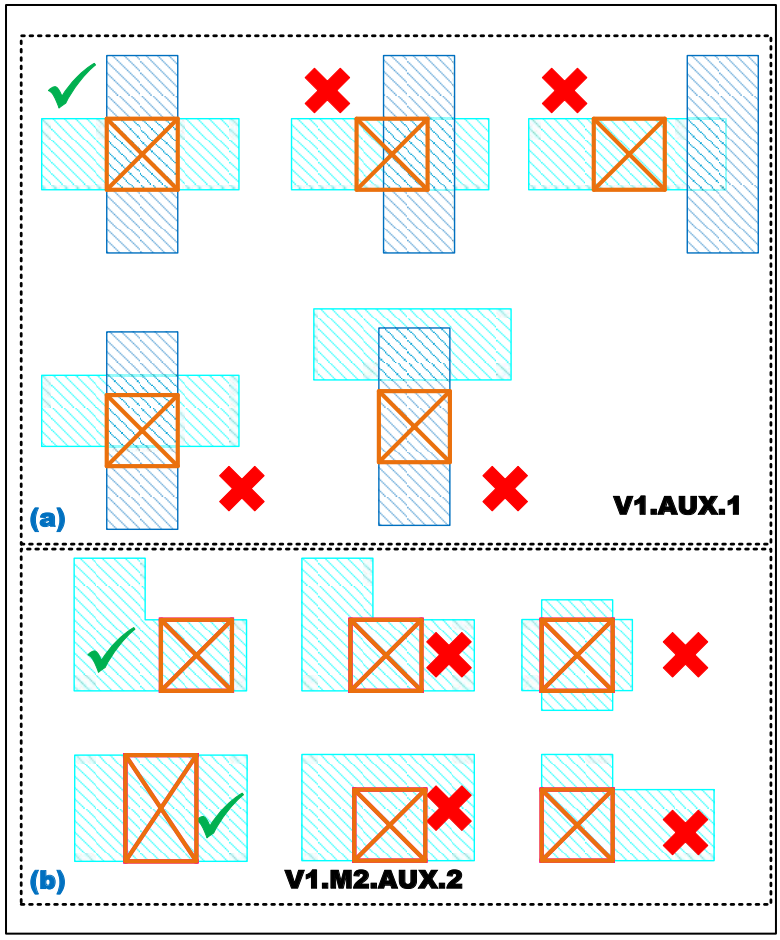

Fig. 3.13.2 Illustration of V1-V3 design rules (2 of 2; see Fig. 3.13.1).

3.14 M4-M5 Design Rules

Unless otherwise stated, assume that the rules listed in this section for M4 apply to M5 as well. However, the M5 design rule directions are perpendicular to those listed below, since M5 routing direction is vertical while that for M4 is horizontal.

Rule	Rule Type	Description	Operator	Values	Units	Notes
M4.W.1	Width	Minimum vertical width of M4	≥	24	nm	-
M4.W.2	Width	Maximum vertical width of M4	≤	480	nm	-
M4.W.3	Width	M4 vertical width may not be an even integer multiple of its minimum width.	-	-	-	-
M4.W.4	Width	M4 vertical width, resulting in the polygon spanning an even number of minimum width routing tracks vertically, is not allowed.	-	-	-	-
M4.W.5	Width	Minimum horizontal width of M4	≥	44	nm	-
M4.S.1	Spacing	Minimum vertical spacing between two M4 layer polygons' edges, regardless of the edge lengths and mask colors	≥	24	nm	-
M4.S.2	Spacing	Minimum horizontal spacing between two M4 layer polygons' edges, regardless of the edge lengths and mask colors	≥	40	nm	-
M4.S.3	Spacing	Minimum tip-to-tip spacing between two M4 layer polygons—that do not share a parallel run length—on adjacent tracks	≥	40	nm	-
M4.S.4	Spacing	Minimum tip-to-tip spacing between two M4 layer polygons—that share a parallel run length—on adjacent tracks	≥	40	nm	-
M4.S.5	Spacing	Minimum parallel run length of two M4 layer polygons on adjacent tracks	≥	44	nm	-

Table 3.14.1 M4-M5 design rules (1 of 2; see Table 3.14.2).

Rule	Rule Type	Description	Operator	Values	Units	Notes
M4.AUX.1	Auxiliary	M4 horizontal edges must be at a grid of	==	24	nm	-
M4.AUX.2	Auxiliary	Minimum width M4 tracks must lie along the horizontal routing tracks. These tracks are located at a spacing equal to: 2N x minimum metal width + offset from the origin, where N $\in$ Z-+.	-	-	-	1
M4.AUX.3	Auxiliary	M4 may not bend.	-	-	-	-
M4.AUX.4	Auxiliary	Outside edge of a wide M4 layer polygon may not touch a routing track edge.	-	-	-	-

Table 3.14.2 M4-M5 design rules (2 of 2; see Table 3.14.1).

NOTES

1. The metal grid offsets from X or Y axis are specified through the use of enviromental variables defined in the set_pdk_path.csh or .cshrc. The default offset value is 0 nm. To offset a particular grid by 'p' nm, specify the variable value as p*10. Thus, for an offset of 24 nm, the corresponding variable value is 240.

Note that currently, the rules only allow offset value for M4-M5 to be an integer multiple of 12 nm.

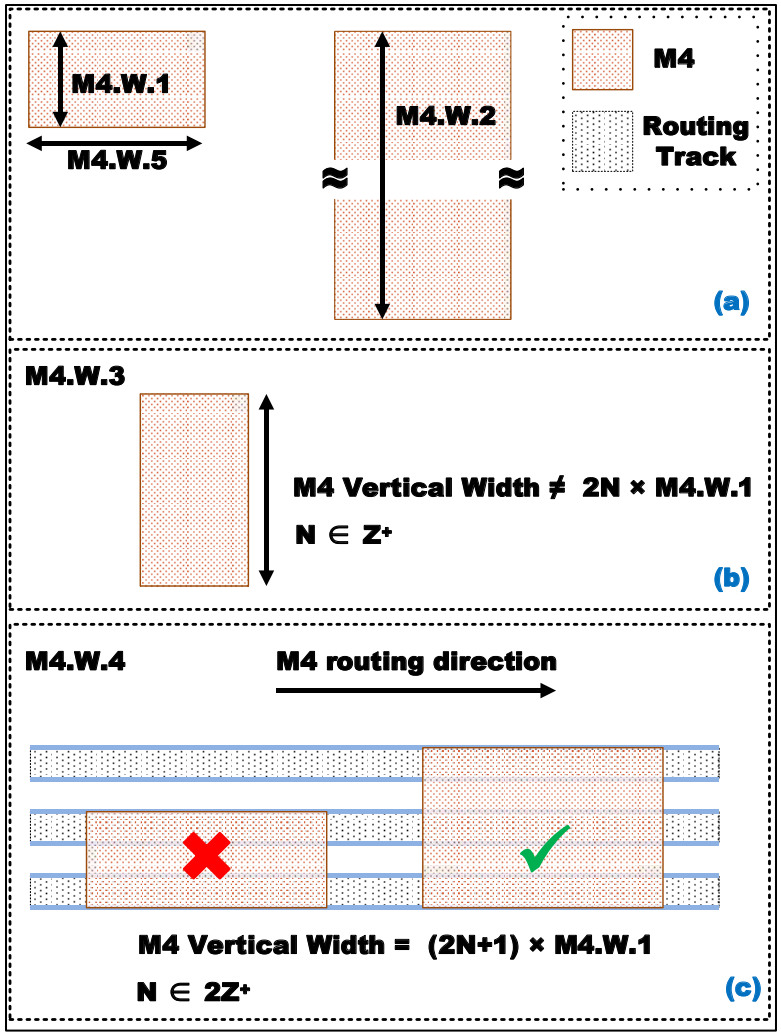

Fig. 3.14.1 Illustration of M4-M5 design rules (1 of 3; see Fig. 3.14.2 and Fig. 3.14.3).

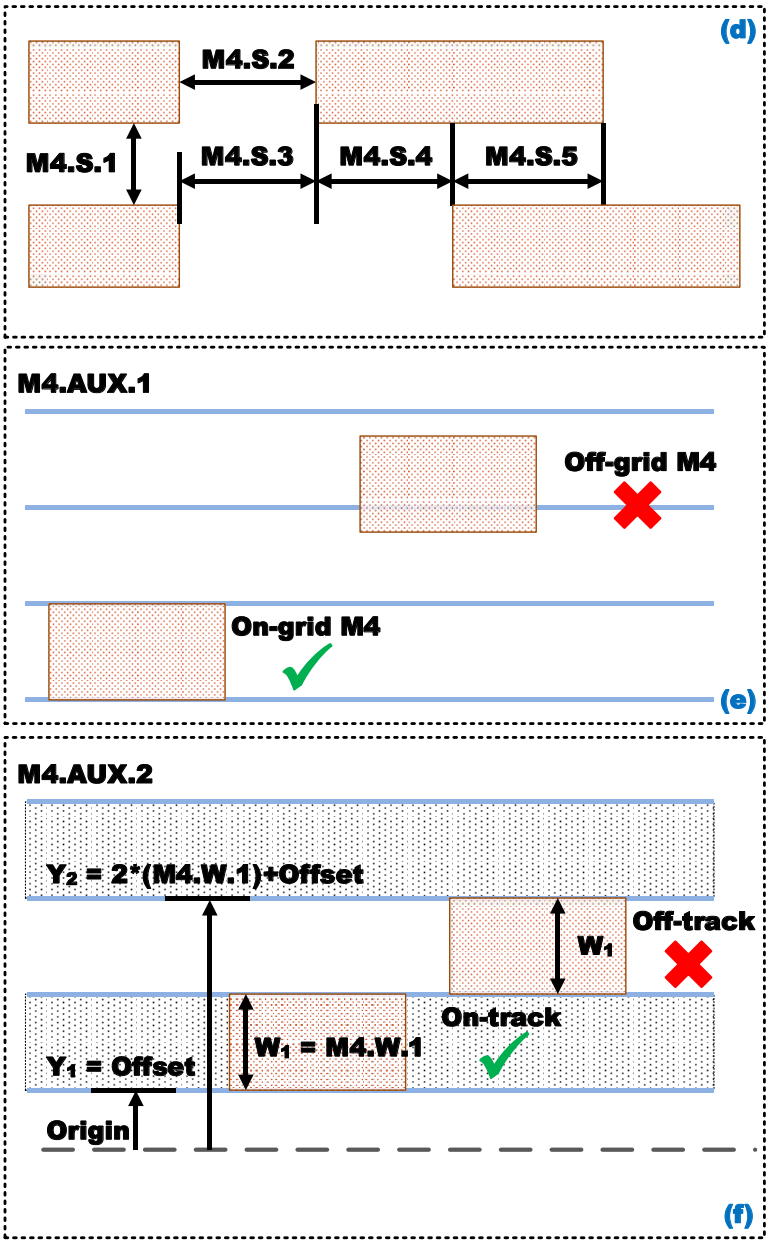

Fig. 3.14.2 Illustration of M4-M5 design rules (2 of 3; see Fig. 3.14.1 and Fig. 3.14.3).

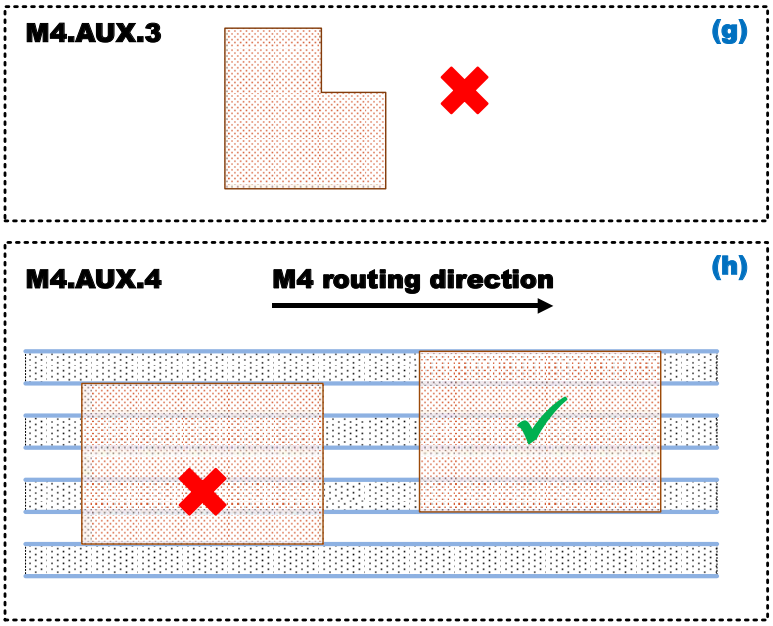

Fig. 3.14.3 Illustration of M4-M5 design rules (3 of 3; see Fig. 3.14.1 and Fig. 3.14.2).

3.15 V4-V5 Design Rules

Unless otherwise stated, assume that the rules listed in this section for V4—either for V4 alone or for V4 in conjunction with M4 or M5—apply to V5 as well, whether it is for V5 alone or for V5 in conjunction with M5 or M6.

These rules will be revised in the subsequent version of the design rule manual.

Rule	Rule Type	Description	Operator	Value	Units	Notes
V4.W.1	Width	Exact width of a V4 instance along the length of M5	==	24	nm	-
V4.S.1	Spacing	Minimum spacing between V4 instances on the same net	≥	33	nm	-
V4.S.2	Spacing	Minimum spacing between V4 instances on different nets	≥	33	nm	-
V4.S.3	Spacing	Minimum corner-to-corner spacing between two V4 instances	≥	33	nm	-
V4.M4.EN.1	Enclosure	Minimum enclosure of V4 by M4 on two opposite sides	≥	11	nm	-
V4.M5.EN.2	Enclosure	Minimum enclosure of V4 by M5 on at least two opposite sides	≥	11	nm	-
V4.AUX.1	Auxiliary	V4 must be inside M4 and M5	-	-	-	-
V4.M5.AUX.2	Auxiliary	V4 must exactly be the same width as M5 along the direction perpendicular to the M5 length	-	-	-	-

Table 3.15.1 V4-V5 design rules.

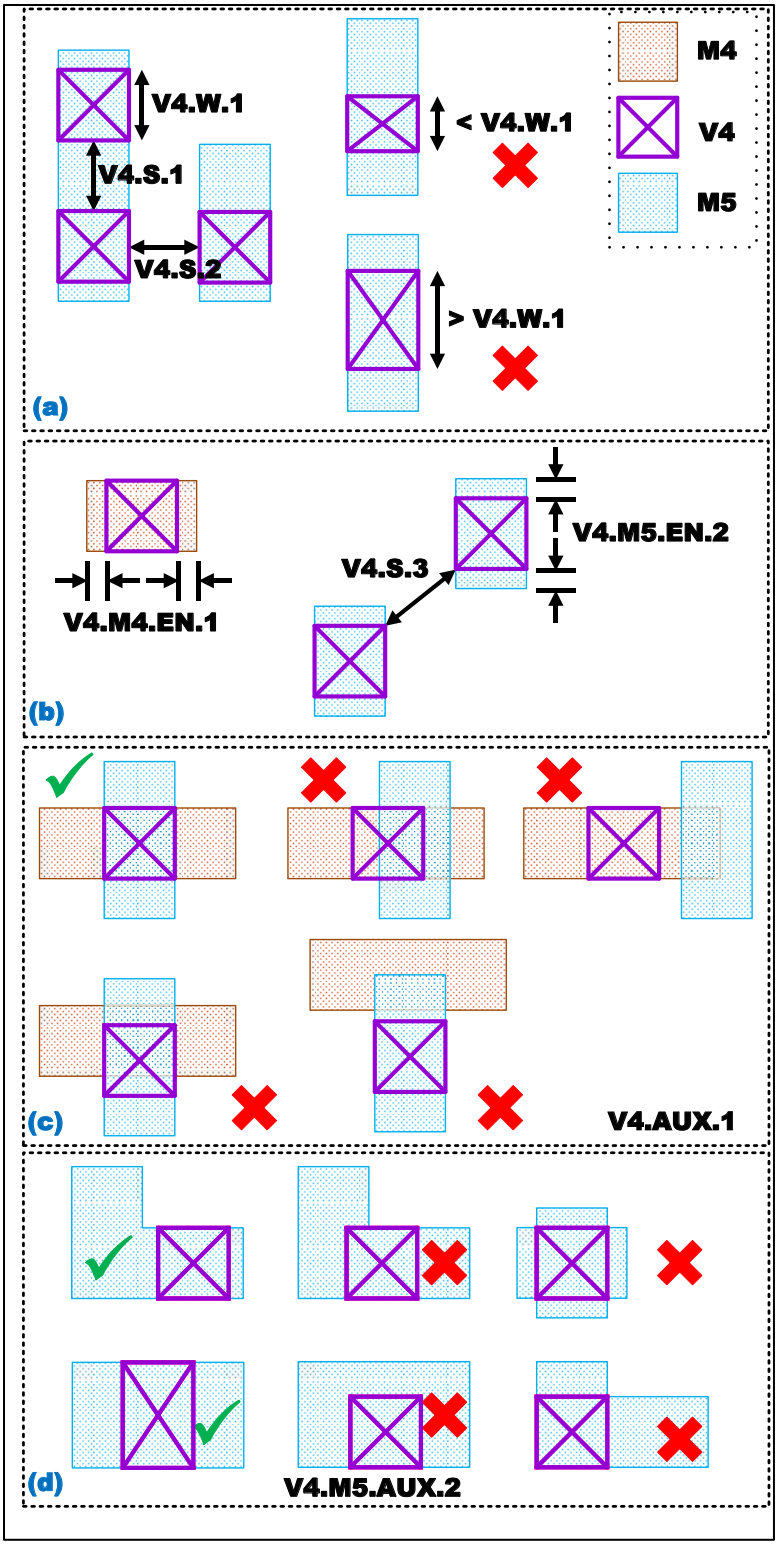

Fig. 3.15.1 Illustration of V4-V5 design rules.

3.16 M6-M7 Design Rules

Unless otherwise stated, assume that the rules listed in this section for M6 apply to M7 as well. However, the M7 design rule directions are perpendicular to those listed below, since M7 routing direction is vertical while that for M6 is horizontal.

Rule	Rule Type	Description	Operator	Values	Units	Notes
M6.W.1	Width	Minimum vertical width of M6	≥	32	nm	-
M6.W.2	Width	Maximum vertical width of M6	≤	640	nm	-
M6.W.3	Width	M6 vertical width may not be an even integer multiple of its minimum width.	-	-	-	-
M6.W.4	Width	M6 vertical width, resulting in the polygon spanning an even number of minimum width routing tracks vertically, is not allowed.	-	-	-	-
M6.W.5	Width	Minimum horizontal width of M6	≥	44	nm	-
M6.S.1	Spacing	Minimum vertical spacing between two M6 layer polygons' edges, regardless of the edge lengths and mask colors	≥	32	nm	-
M6.S.2	Spacing	Minimum horizontal spacing between two M6 layer polygons' edges, regardless of the edge lengths and mask colors	≥	40	nm	-
M6.S.3	Spacing	Minimum tip-to-tip spacing between two M6 layer polygons—that do not share a parallel run length—on adjacent tracks	≥	40	nm	-
M6.S.4	Spacing	Minimum tip-to-tip spacing between two M6 layer polygons—that share a parallel run length—on adjacent tracks	≥	40	nm	-
M6.S.5	Spacing	Minimum parallel run length of two M6 layer polygons on adjacent tracks	≥	44	nm	-

Table 3.16.1 M6-M7 design rules (1 of 2; see Table 3.16.2).

Rule	Rule Type	Description	Operator	Values	Units	Notes
M6.AUX.1	Auxiliary	M6 horizontal edges must be at a grid of	==	32	nm	-
M6.AUX.2	Auxiliary	Minimum width M6 tracks must lie along the horizontal routing tracks. These tracks are located at a spacing equal to: 2N x minimum metal width + offset from the origin, where N $\in$ Z-+.	-	-	-	1
M6.AUX.3	Auxiliary	M6 may not bend.	-	-	-	-
M6.AUX.4	Auxiliary	Outside edge of a wide M6 layer polygon may not touch a routing track edge.	-	-	-	-

Table 3.16.2 M6-M7 design rules (2 of 2; see Table 3.16.1).

NOTES

1. The metal grid offsets from X or Y axis are specified through the use of enviromental variables defined in the set_pdk_path.csh or .cshrc. The default offset value is 0 nm. To offset a particular grid by 'p' nm, specify the variable value as p*10. Thus, for an offset of 32 nm, the corresponding variable value is 320.

Note that currently, the rules only allow offset value for M6-M7 to be an integer multiple of 16 nm.

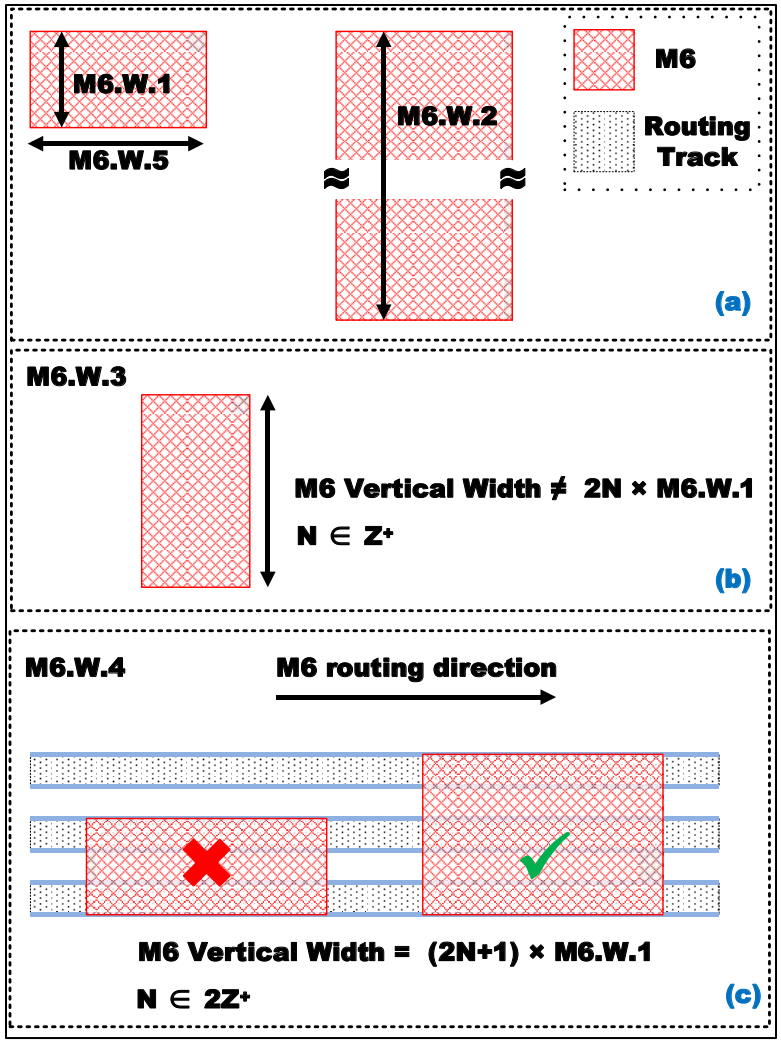

Fig. 3.16.1 Illustration of M6-M7 design rules (1 of 3; see Fig. 3.16.2 and Fig. 3.16.3).

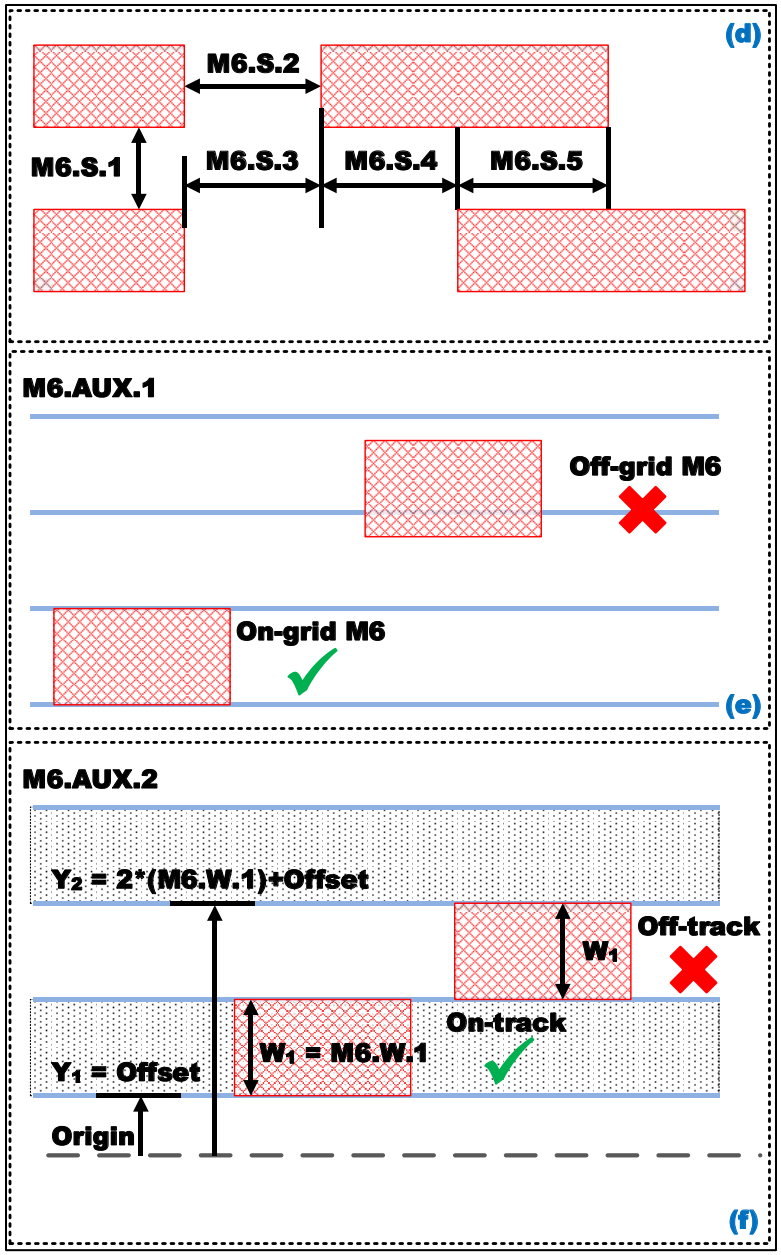

Fig. 3.16.2 Illustration of M6-M7 design rules (2 of 3; see Fig. 3.16.1 and Fig. 3.16.3).

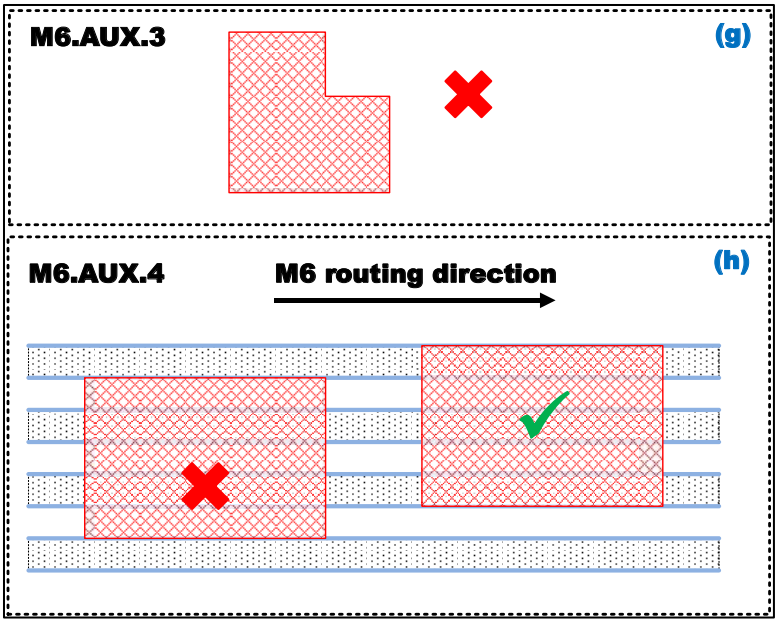

Fig. 3.16.3 Illustration of M6-M7 design rules (3 of 3; see Fig. 3.16.1 and Fig. 3.16.2).

3.17 V6-V7 Design Rules

Unless otherwise stated, assume that the rules listed in this section for V6—either for V6 alone or for V6 in conjunction with M6 or M7—apply to V7 as well, whether it is for V7 alone or for V7 in conjunction with M7 or M8.

These rules will be revised in the subsequent version of the design rule manual.

Rule	Rule Type	Description	Operator	Value	Units	Notes
V6.W.1	Width	Exact width of a V6 instance along the length of M5	==	32	nm	-
V6.S.1	Spacing	Minimum spacing between V6 instances on the same net	≥	45	nm	-
V6.S.2	Spacing	Minimum spacing between V6 instances on different nets	≥	45	nm	-
V6.S.3	Spacing	Minimum corner-to-corner spacing between two V6 instances	≥	45	nm	-
V6.M6.EN.1	Enclosure	Minimum enclosure of V6 by M6 on at least two opposite sides	≥	11	nm	-
V6.M7.EN.2	Enclosure	Minimum enclosure of V6 by M7 on two opposite sides	≥	11	nm	-
V6.AUX.1	Auxiliary	V6 must be inside M6 and M7	-	-	-	-
V6.M7.AUX.2	Auxiliary	V6 must exactly be the same width as M7 along the direction perpendicular to the M7 length	-	-	-	-

Table 3.17.1 V6-V7 design rules.

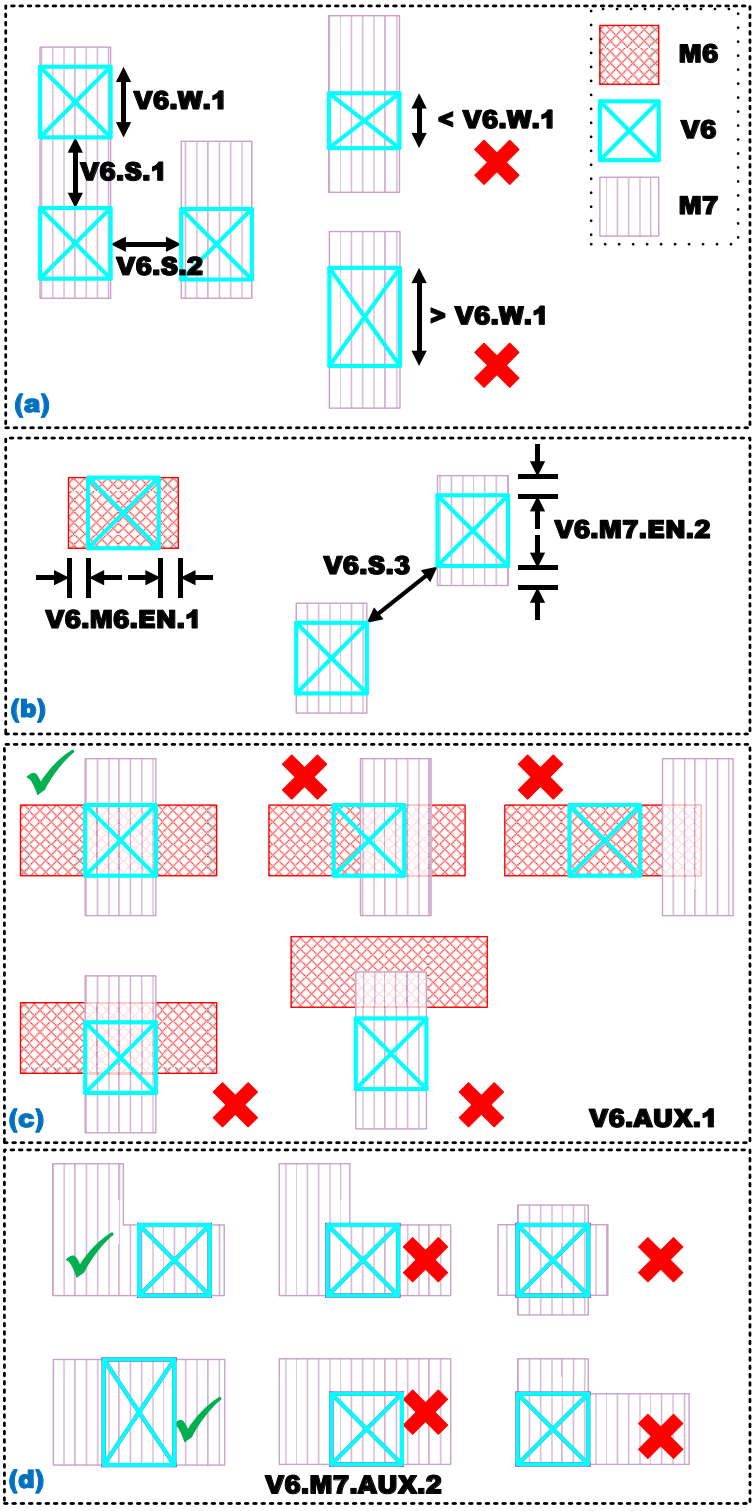

Fig. 3.17.1 Illustration of V6-V7 design rules.

3.18 M8-M9 Design Rules

Unless otherwise stated, assume that the rules listed in this section for M8, apply to M9 as well.

These rules will be revised in the subsequent version of the design rule manual.

Rule	Rule Type	Description	Operator	Value	Units	Notes
M8.W.1	Width	Minimum width of M8	≥	40	nm	-
M8.W.2	Width	Minimum width of M8, when its length >= 400 nm and < 1200 nm	≥	60	nm	-
M8.W.3	Width	Minimum width of M8, when its length >= 1200 nm and < 1800 nm	≥	80	nm	-
M8.W.4	Width	Minimum width of M8, when its length >= 1800 nm	≥	120	nm	-
M8.W.5	Width	Maximum width of M8	≥	2000	nm	-
M8.S.1	Spacing	Minimum (side-to-side) spacing between two M8 layer polygons' edges, when both edges are >= 80 nm	≥	40	nm	-
M8.S.2	Spacing	Minimum (tip-to-side) spacing between two M8 layer polygons' edges, when one of the edges is < 80 nm and the other is >= 80 nm	≥	43	nm	-
M8.S.3	Spacing	Minimum (tip-to-tip) spacing between two M8 layer polygons' edges, when both edges are < 80 nm	≥	46	nm	-
M8.S.4	Spacing	Minimum spacing between two M8 layer polygons' edges, when one of the edges is >= 60 nm and < 80 nm	≥	60	nm	-

Table 3.18.1 M8-M9 design rules (1 of 2; see Table 3.18.2).

Rule	Rule Type	Description	Operator	Value	Units	Notes
M8.S.5	Spacing	Minimum spacing between two M8 layer polygons' edges, when one of the edges is >= 80 nm and < 120 nm	≥	80	nm	-
M8.S.6	Spacing	Minimum spacing between two M8 layer polygons' edges, when one of the edges is >= 120 nm and < 500 nm	≥	120	nm	-
M8.S.7	Spacing	Minimum spacing between two M8 layer polygons' edges, when one of the edges is >= 500 nm and < 1000 nm	≥	500	nm	-
M8.S.8	Spacing	Minimum spacing between two M8 layer polygons' edges, when one of the edges is >= 1000 nm	≥	1000	nm	-
M8.A.1	Area	Minimum area of M8	≥	7520	nm-sq	-
M8.L.1	Length	Minimum feature length of M8	≥	40	nm	-

Table 3.18.2 M8-M9 design rules (2 of 2; see Table 3.18.1).

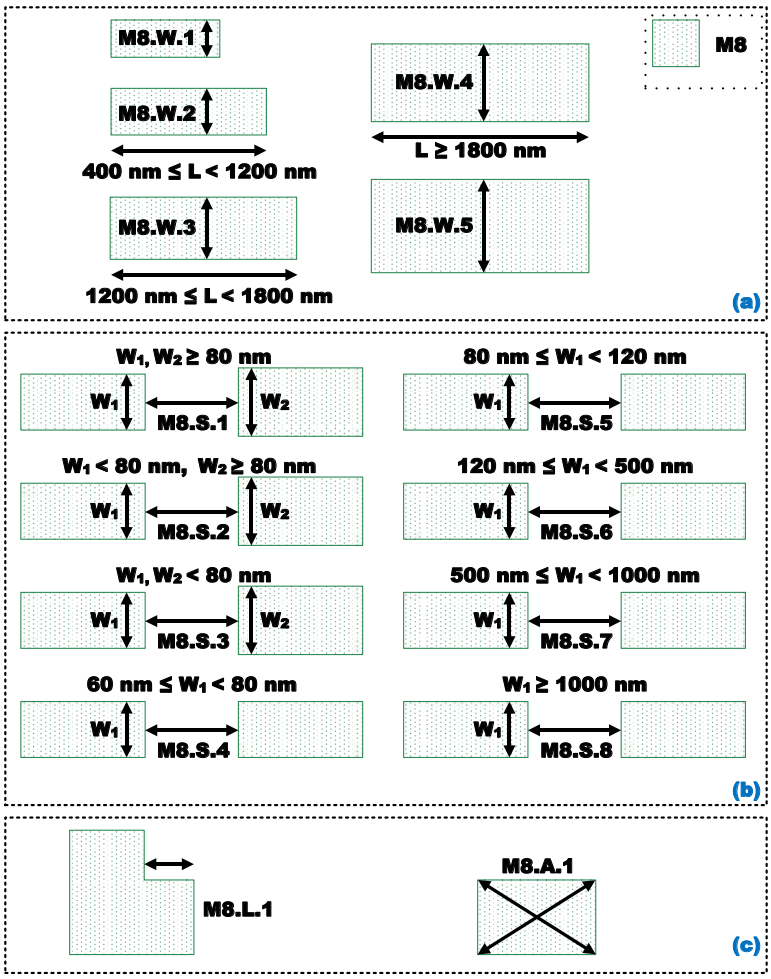

Fig. 3.18.1 Illustration of M8-M9 design rules.

3.19 V8-V9 Design Rules

Unless otherwise stated, assume that the rules listed in this section for V8—either for V8 alone or for V8 in conjunction with M8 or M9—apply to V9 as well, whether it is for V9 alone or for V9 in conjunction with M9 or PAD.

These rules will be revised in the subsequent version of the design rule manual.

Rule	Rule Type	Description	Operator	Value	Units	Notes
V8.W.1	Width	Exact width of a V8 instance	=	[40x40 | 40x120 | 120x40]	nm	-
V8.S.1	Spacing	Minimum spacing between two V8 instances	≥	57	nm	-
V8.S.2	Spacing	Minimum corner-to-corner spacing between V8 instances	≥	57	nm	-
V8.M8.EN.1	Enclosure	Minimum enclosure of V8 by M8 on at least two opposite sides	≥	20	nm	-
V8.M9.EN.2	Enclosure	Minimum enclosure of V8 by M9 on at least two opposite sides	≥	20	nm	-
V8.AUX.1	Auxiliary	V8 must be inside M8 and M9	-	-	-	-

Table 3.19.1 V8-V9 design rules.

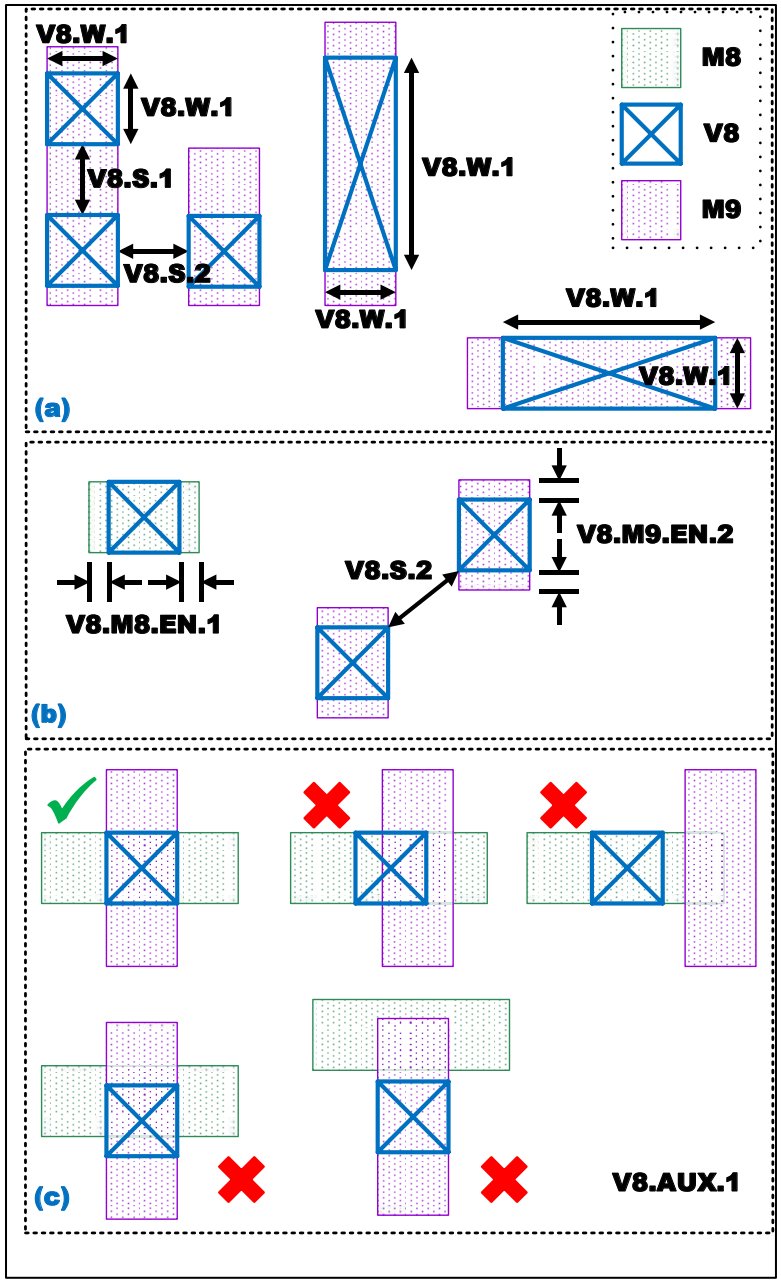

Fig. 3.19.1 Illustration of V8-V9 design rules.