

EECS Lab – Summer Training

Virtuoso / Layout & hspice

2023/08/22 Lab07

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洪侑廷 EECS Lab, NYCU

目錄

- Environment Setting
- Create New Library
- 7nm inv, dff LVS + DRC verification
- Display setting / 常用 Hotkey
- Layout DRC / LVS Flow
- Ring Oscillator 環形振盪器介紹
- 本次 lab 題目 Ring Oscillator 要求、通過條件
- 附件補充

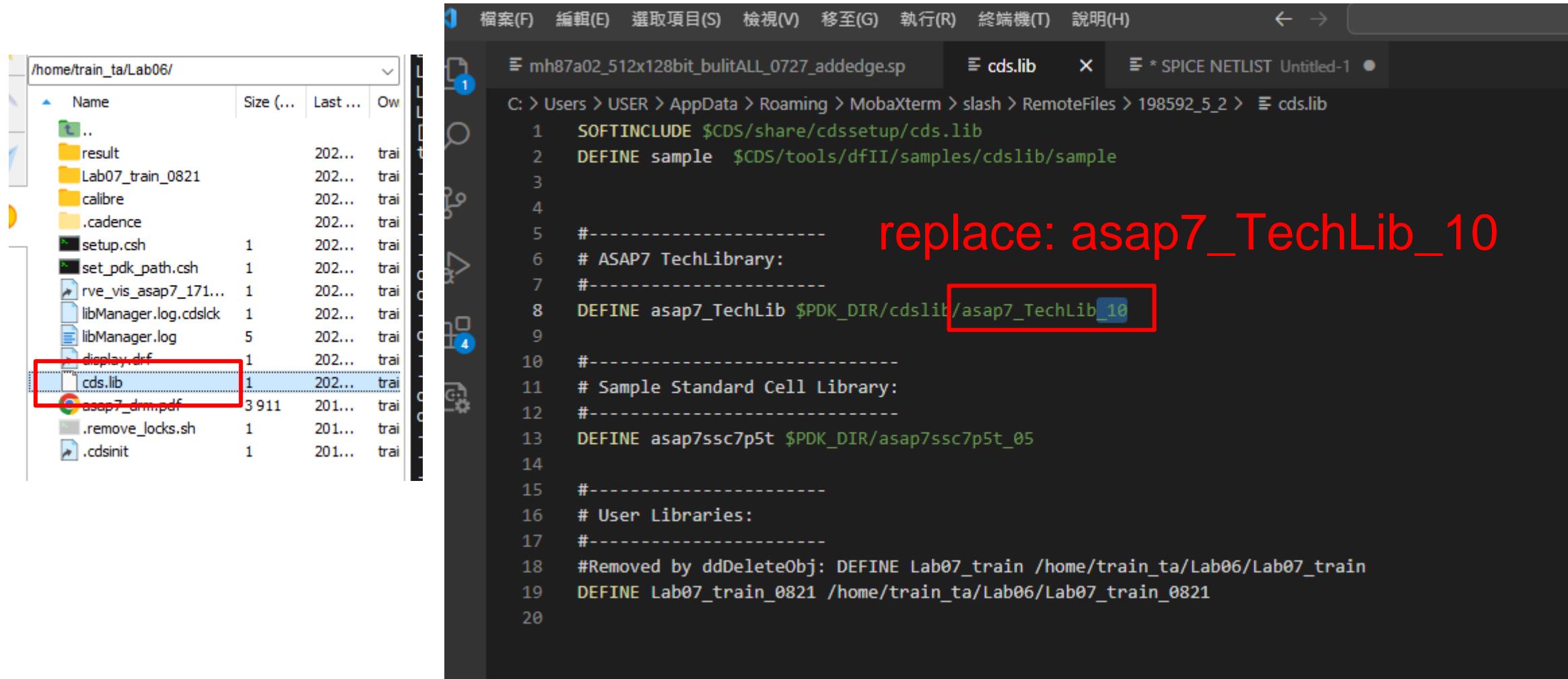
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Environment Setting - 1

- Please rename your Lab06 folder
- tar xvf ~train_ta/Lab07_2023.tar
- cd Lab06
- source setup.csh
 - (every time you log in to the server 細部大家可以開裡面指令看)
- virtuoso & (& 用於同時在背景執行)

Environment Setting - 2



The screenshot shows a terminal window with two panes. The left pane is a file browser displaying files in the directory `/home/train_ta/Lab06/`. The right pane is a text editor showing a SPICE netlist script.

File Browser (Left):

Name	Size ...	Last ...	Ow
...			
result	202...	trai	
Lab07_train_0821	202...	trai	
calibre	202...	trai	
.cadence	202...	trai	
setup.csh	1	202...	trai
set_pdk_path.csh	1	202...	trai
rve_vis_asap7_171...	1	202...	trai
libManager.log.cdsclk	1	202...	trai
libManager.log	5	202...	trai
display.drf	1	202...	trai
cds.lib	1	202...	trai
asap7_drcmp.pdf	3 911	201...	trai
.remove_locks.sh	1	201...	trai
.cdsinit	1	201...	trai

Text Editor (Right):

```
C: > Users > USER > AppData > Roaming > MobaXterm > slash > RemoteFiles > 198592_5_2 > cds.lib
1  SOFTINCLUDE $CDS/share/cdssetup/cds.lib
2  DEFINE sample $CDS/tools/dfII/samples/cdslib/sample
3
4
5  #-----
6  # ASAP7 TechLibrary:
7  #-----
8  DEFINE asap7_TechLib $PDK_DIR/cdslib/asap7_TechLib_10
9
10 #-----
11 # Sample Standard Cell Library:
12 #-----
13 DEFINE asap7ssc7p5t $PDK_DIR/asap7ssc7p5t_05
14
15 #-----
16 # User Libraries:
17 #-----
18 #Removed by ddDeleteObj: DEFINE Lab07_train /home/train_ta/Lab06/Lab07_train
19 DEFINE Lab07_train_0821 /home/train_ta/Lab06/Lab07_train_0821
20
```

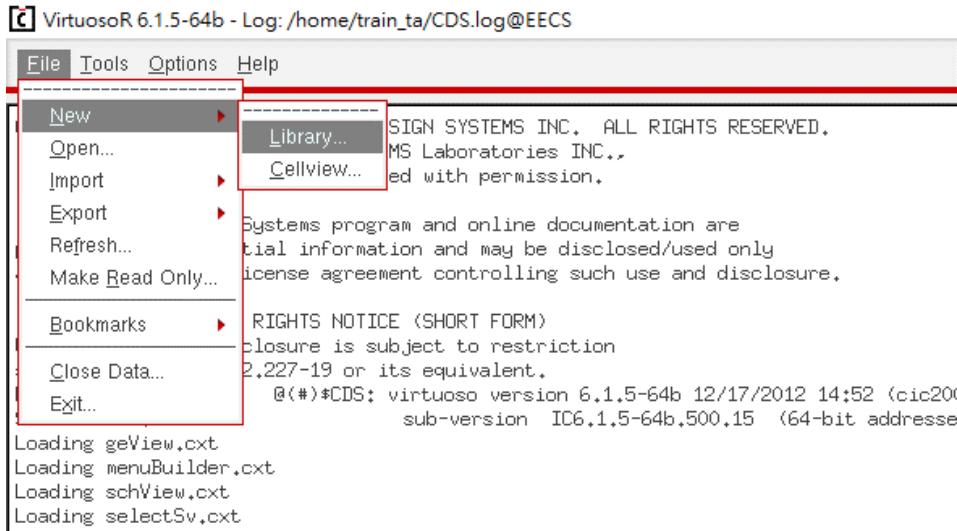
A red box highlights the line `DEFINE asap7_TechLib $PDK_DIR/cdslib/asap7_TechLib_10`. A red box also highlights the file `cds.lib` in the file browser. The text `replace: asap7_TechLib_10` is overlaid in red in the center of the terminal window.

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Create New Library

1.



2.



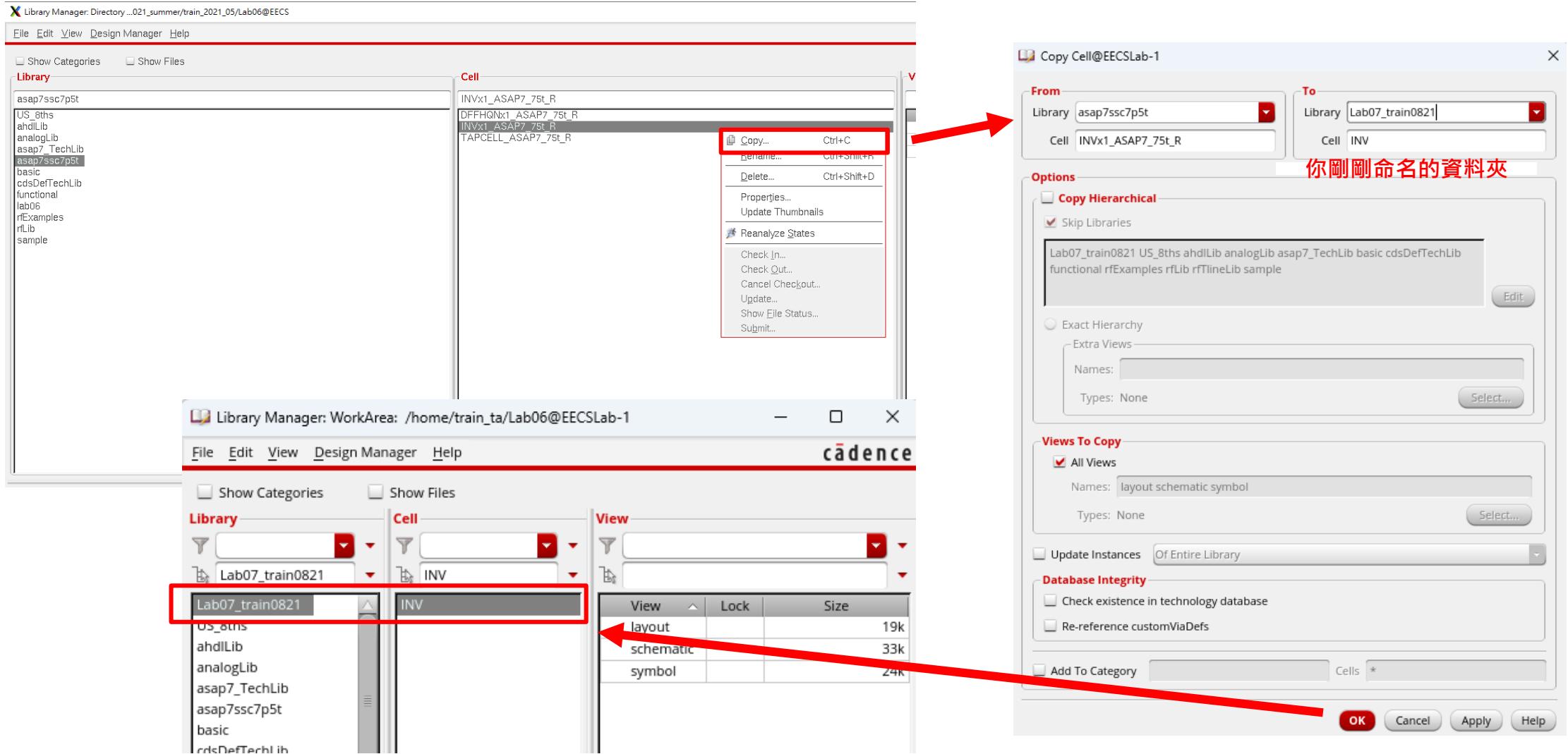
3.



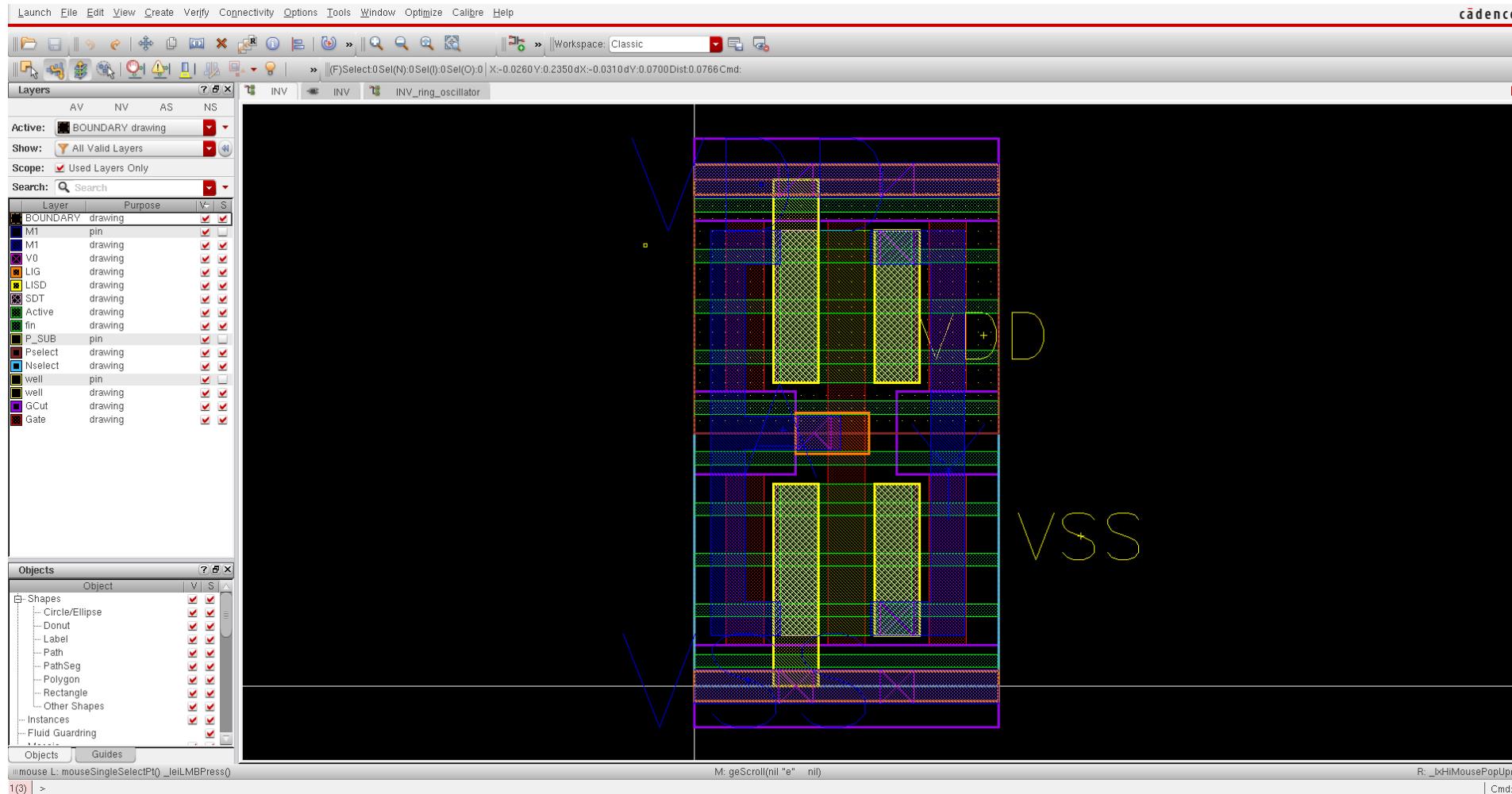
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LVS + DRC : Copy standard cell



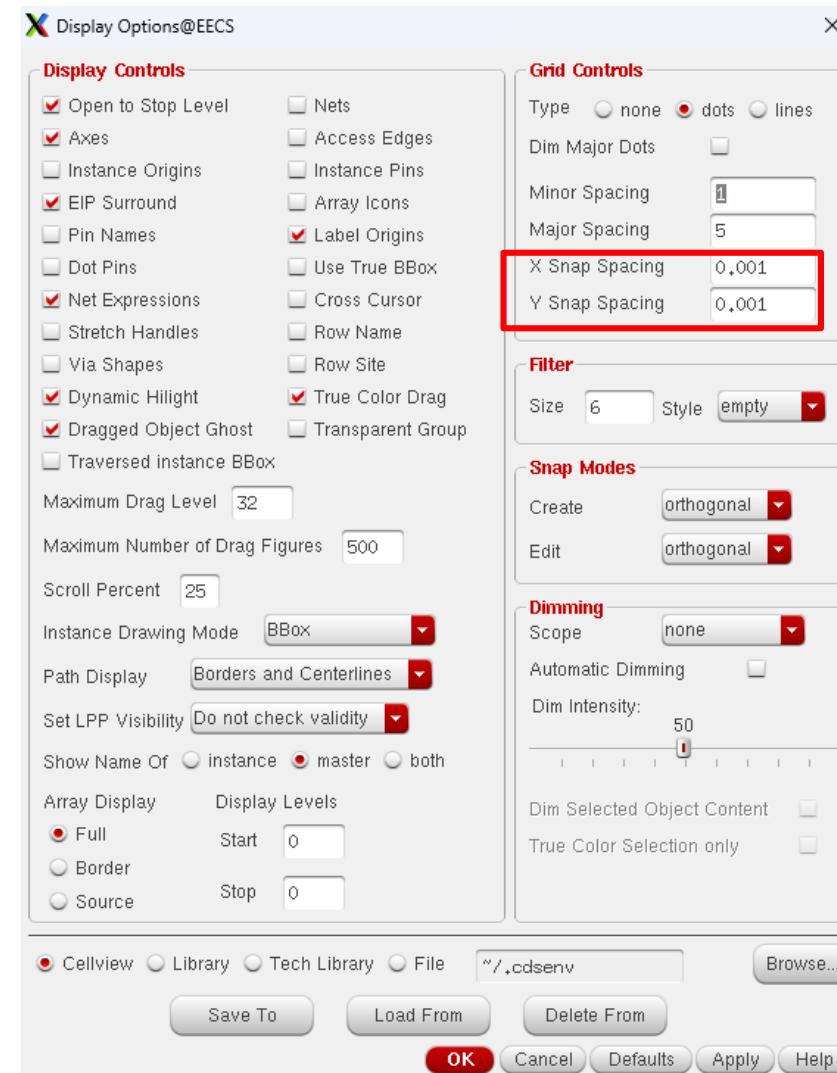
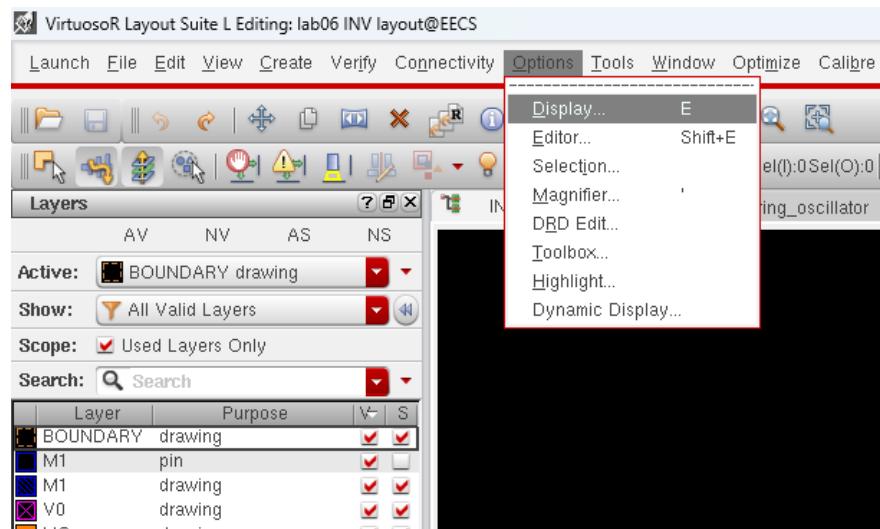
開啟 layout



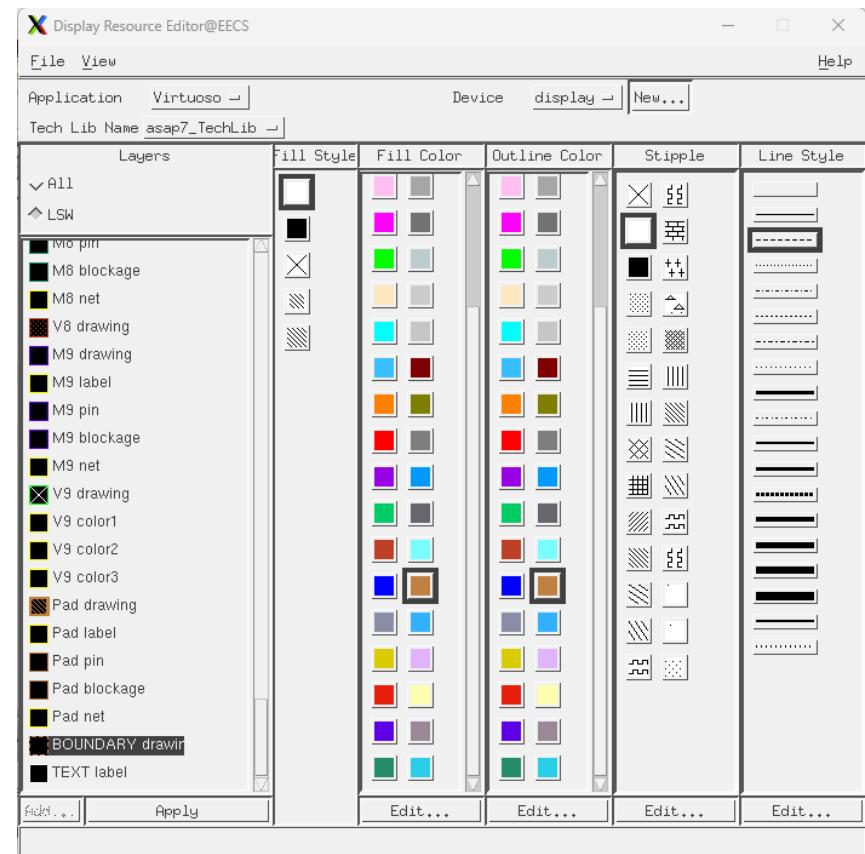
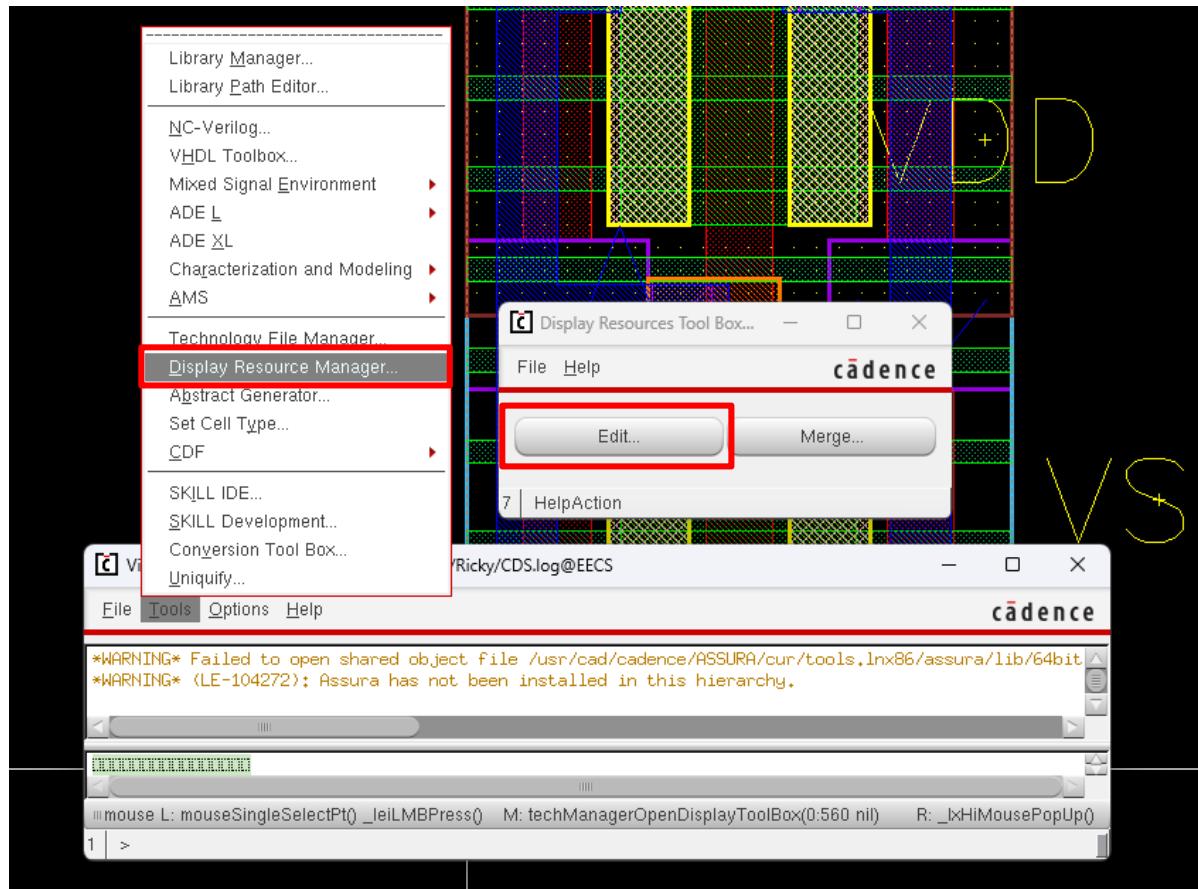
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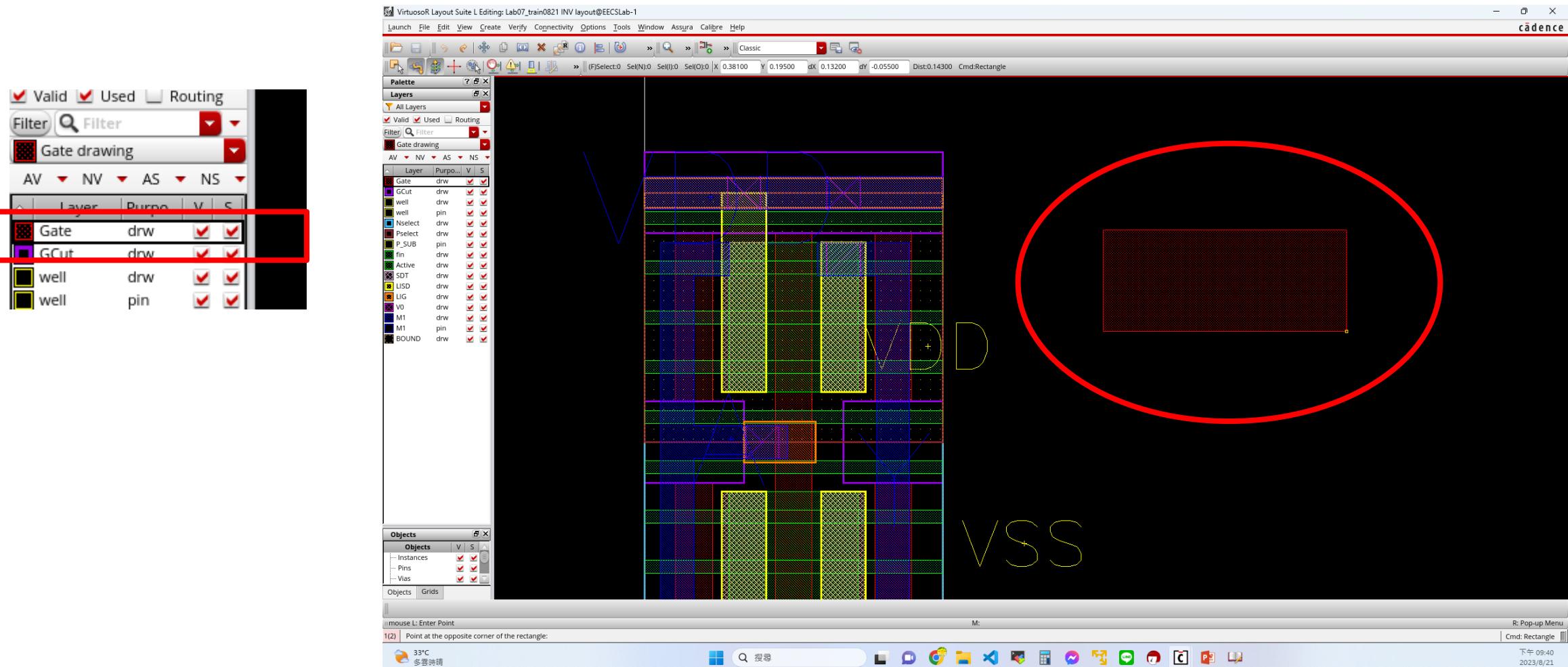
Display - Grid controls



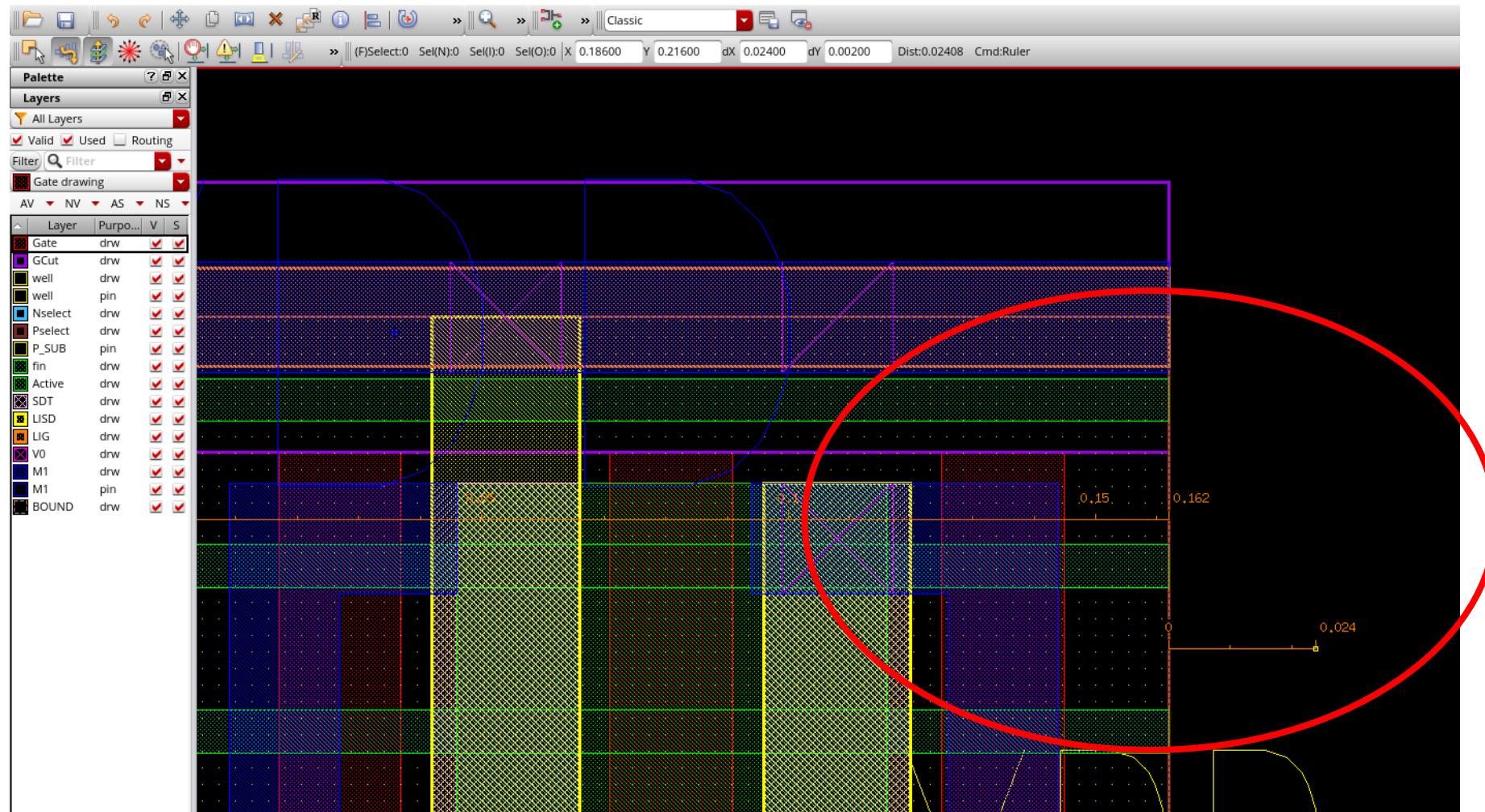
Display - 更改塗層顏色



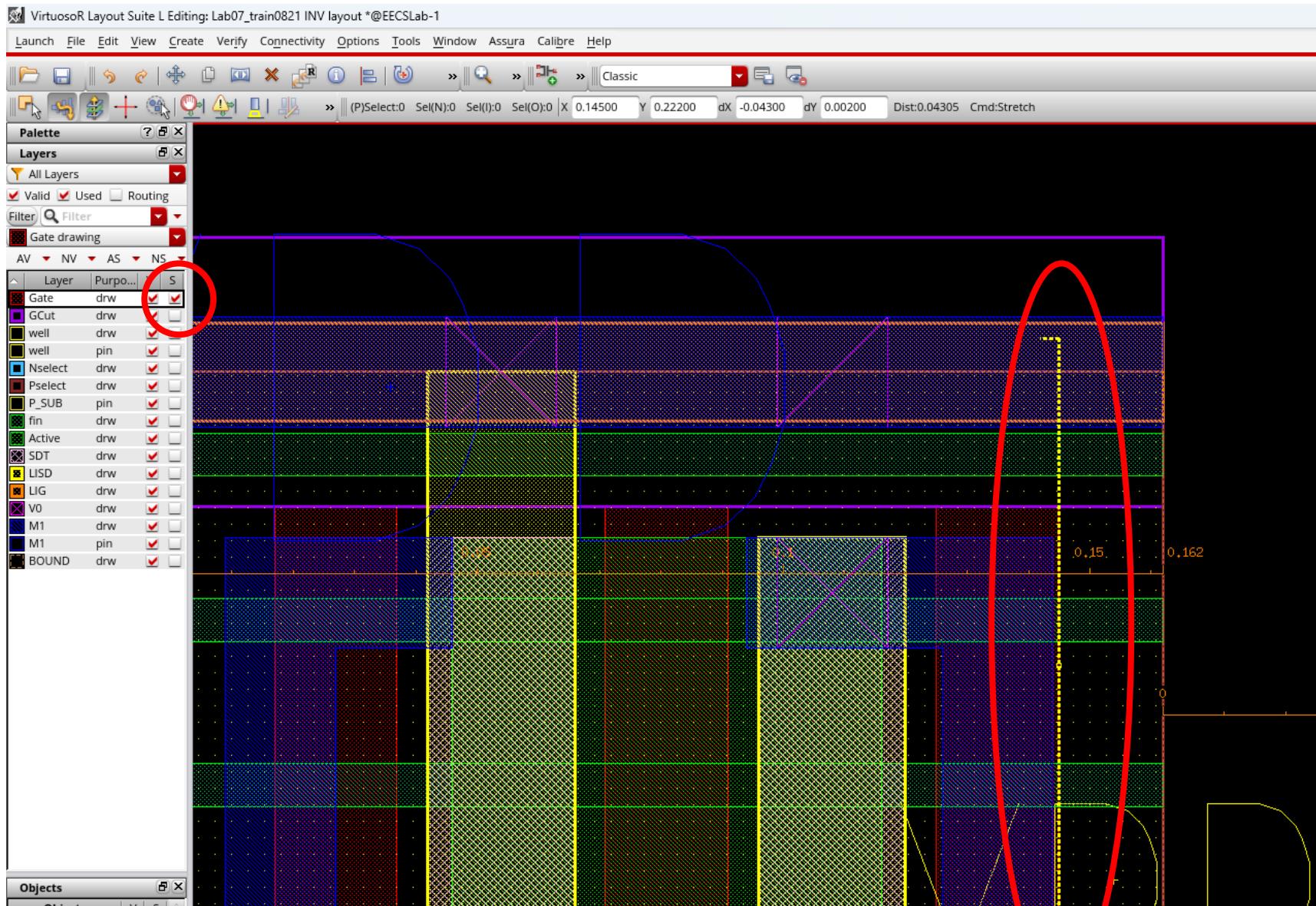
常用 Hotkey – 拉圖層方塊 (R)



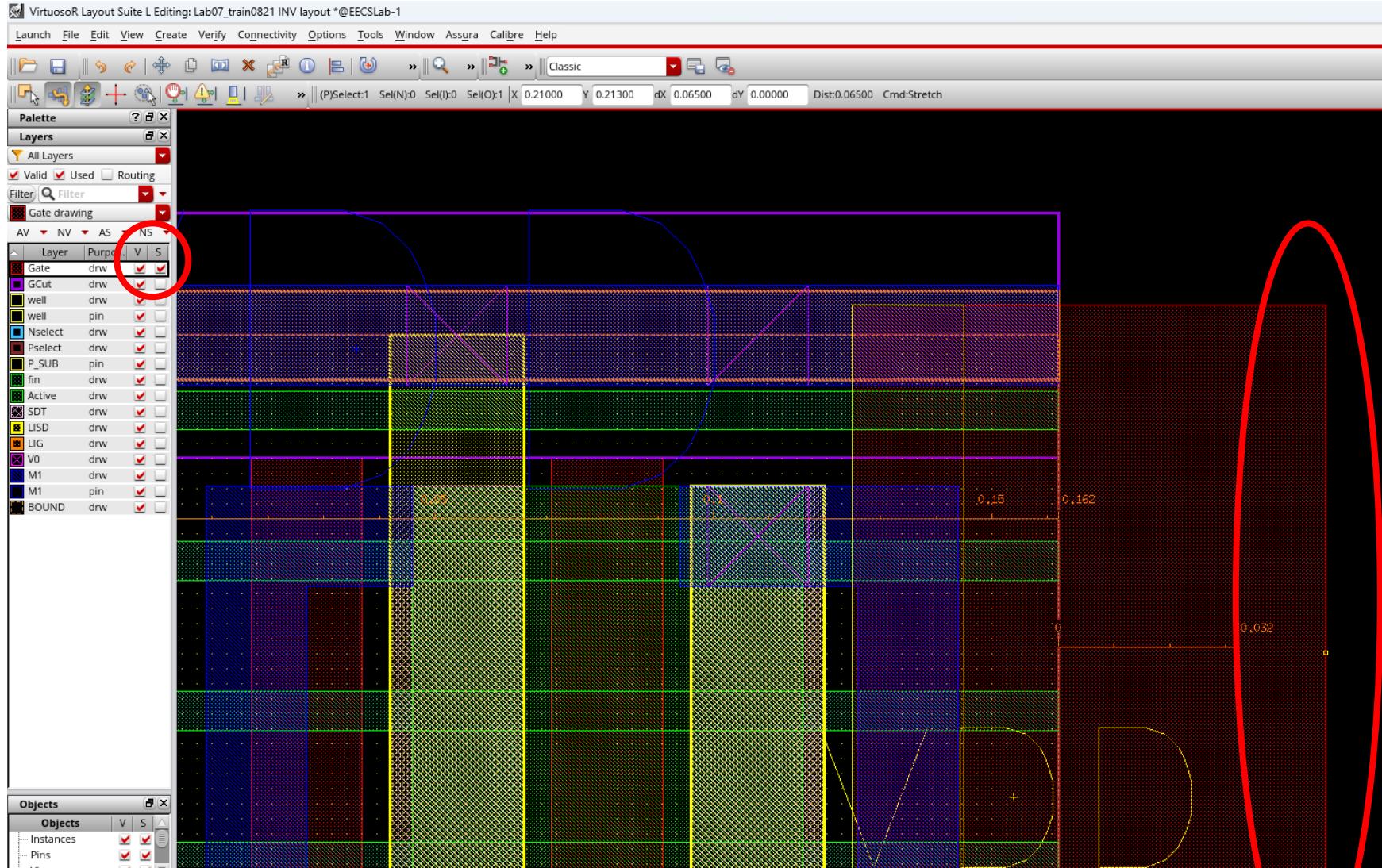
常用 Hotkey – 測量 & 清除測量 (K & shift+K)



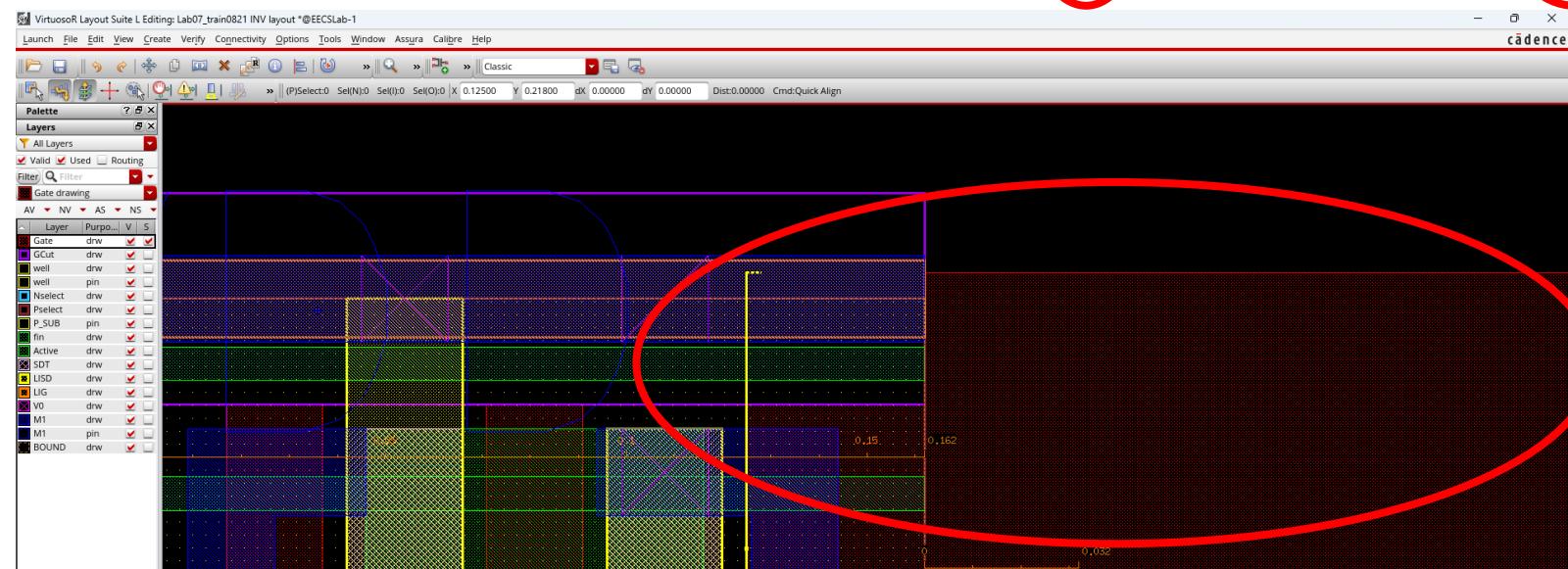
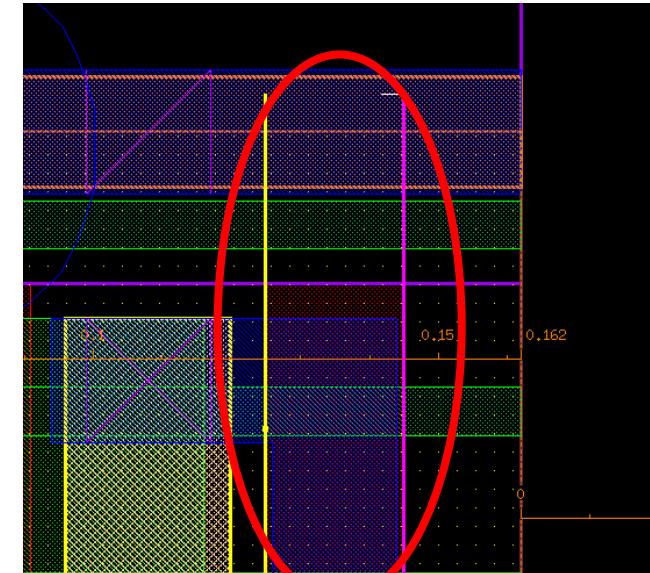
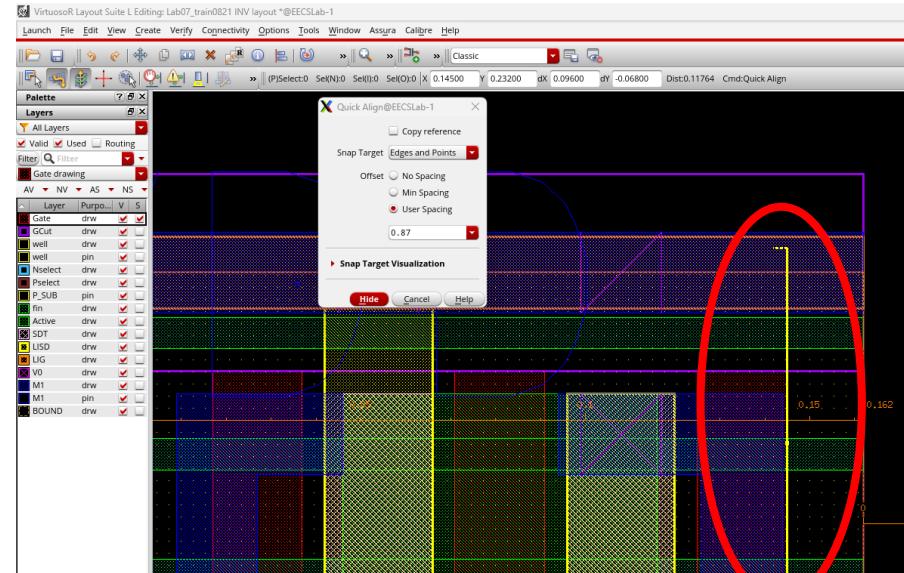
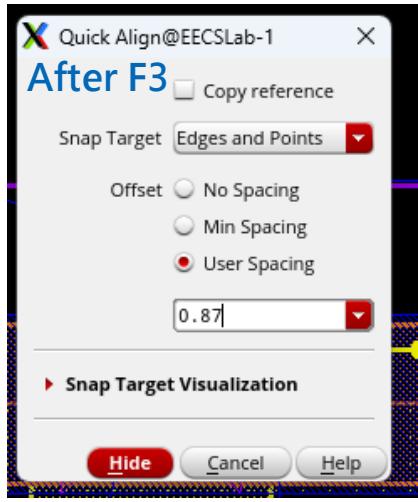
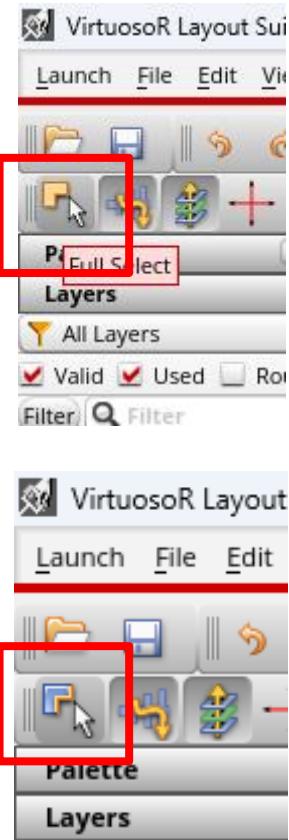
常用 Hotkey – 拉伸 (S)



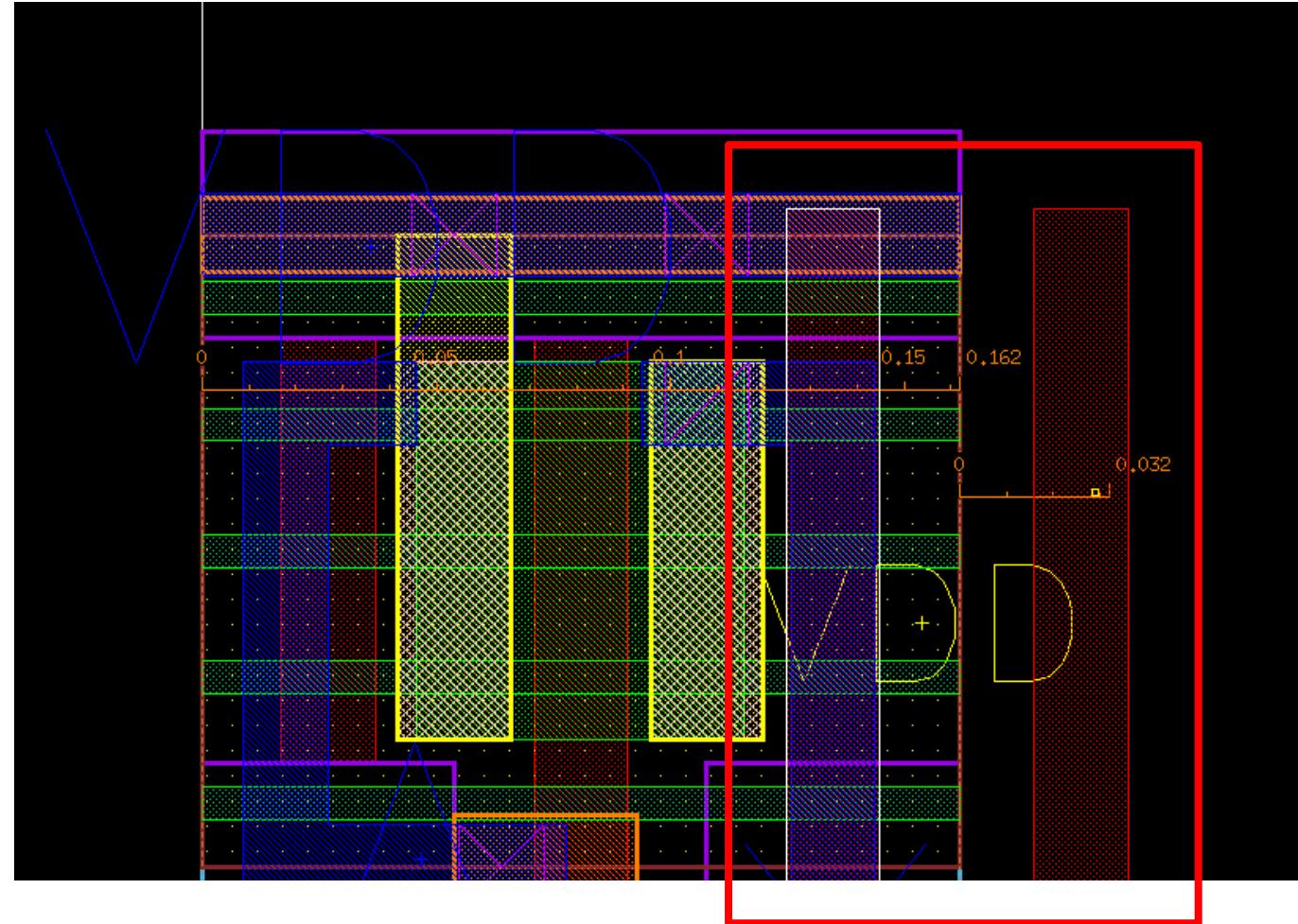
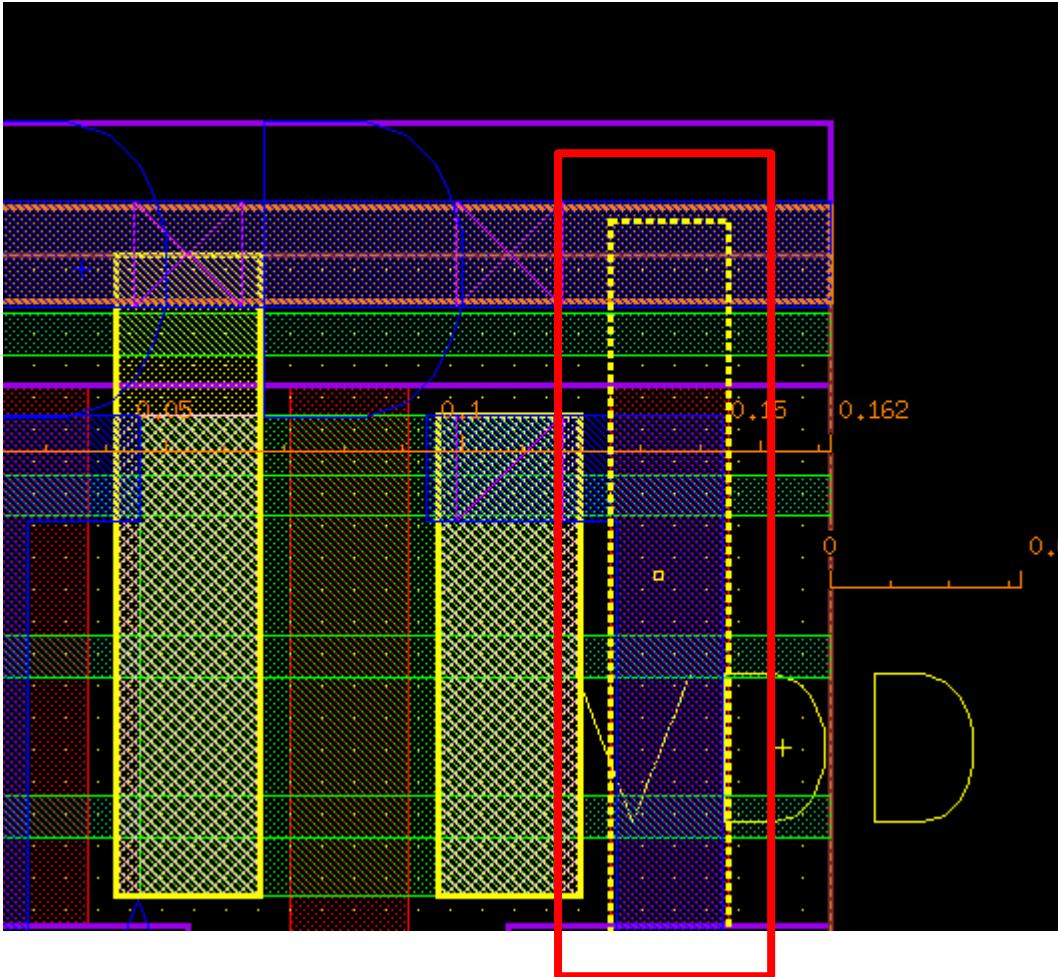
常用 Hotkey – 拉伸 (S)



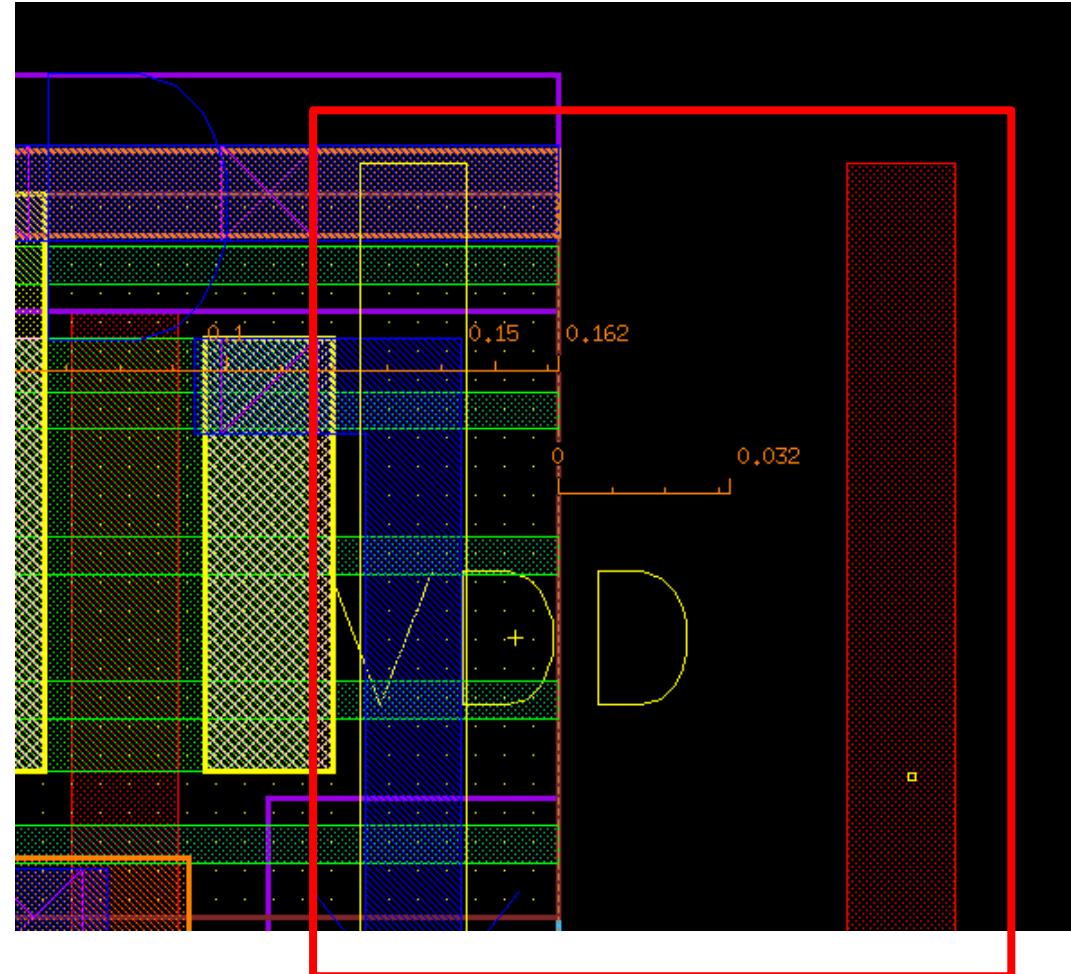
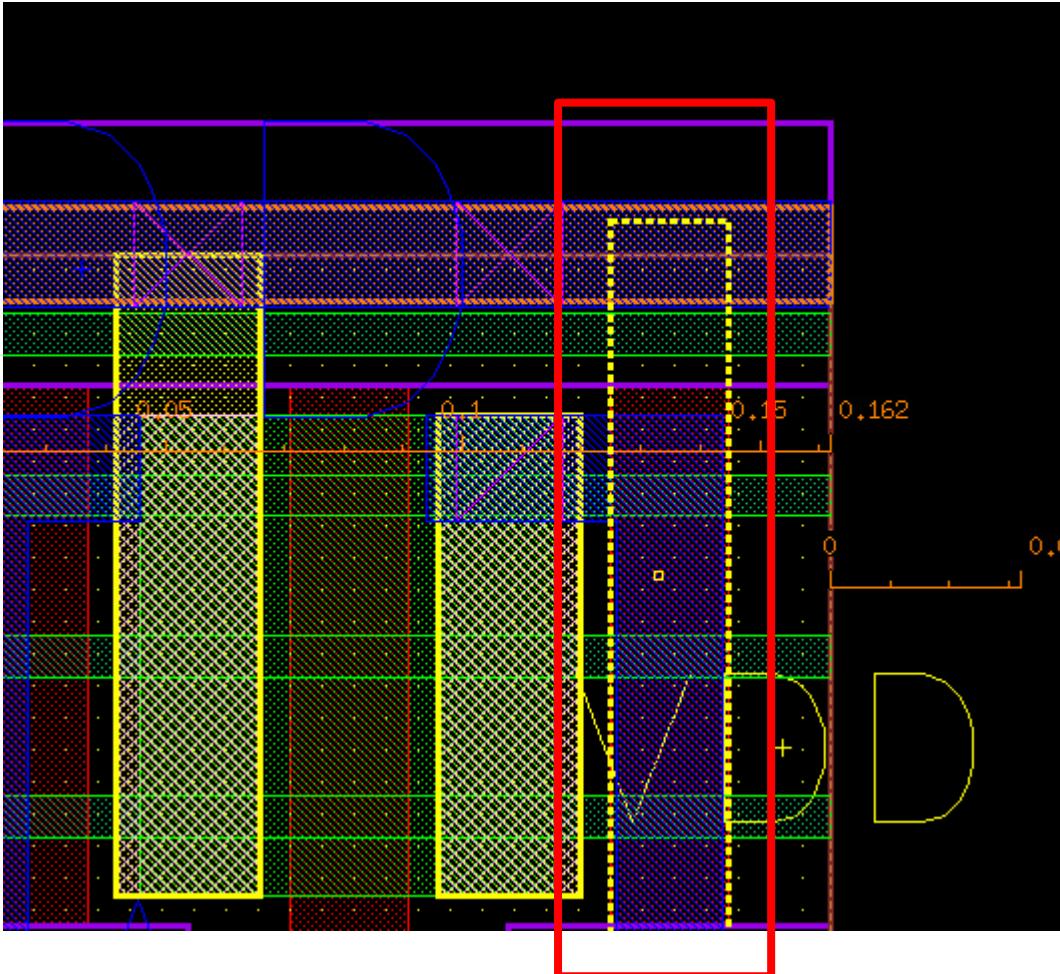
常用 Hotkey - 對齊 (A + F3)



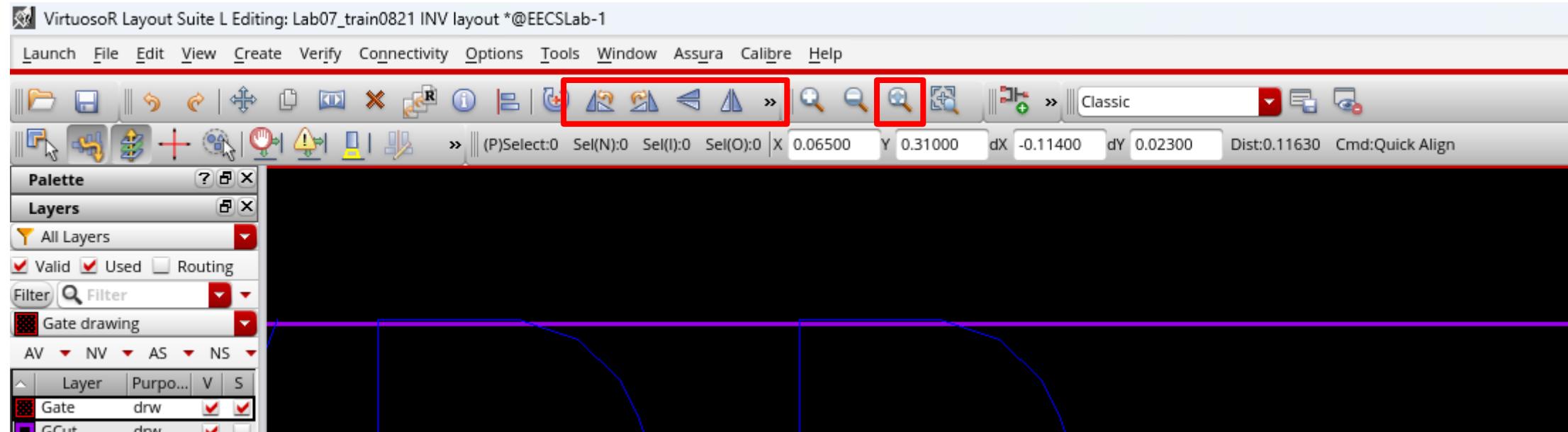
常用 Hotkey – 複製 (C)



常用 Hotkey – 移動 (M)



常用 Hotkey – 旋轉、全視角、esc=取消動作



esc=取消動作

Virtuoso Hotkey

C: Copy

F: 顯示全圖

K: 尺規

M: 移動

Q: 元件內部屬性

S: 圖形延伸或縮小

Shift+K: 消除尺規

Ctrl+Z: 放大

Delete: 刪除

I: 呼叫元件

L: 打I/O與vdd, gnd塊

O: 呼叫 Contact塊

R: 劃長方形

U: Undo

Shift+Z: 縮小

esc: 取消動作

UNIX Hotkey

ls :list files and directories

mkdir : make a directory

cd directory : change to named directory

cd (空白) ; **cd ~** : change to home directory

cd .. :change to parent directory

pwd : display the path of the directory

cp file1 file2 : copy file1 and call it file2

mv file1 file2 : move or rename file1 to file2

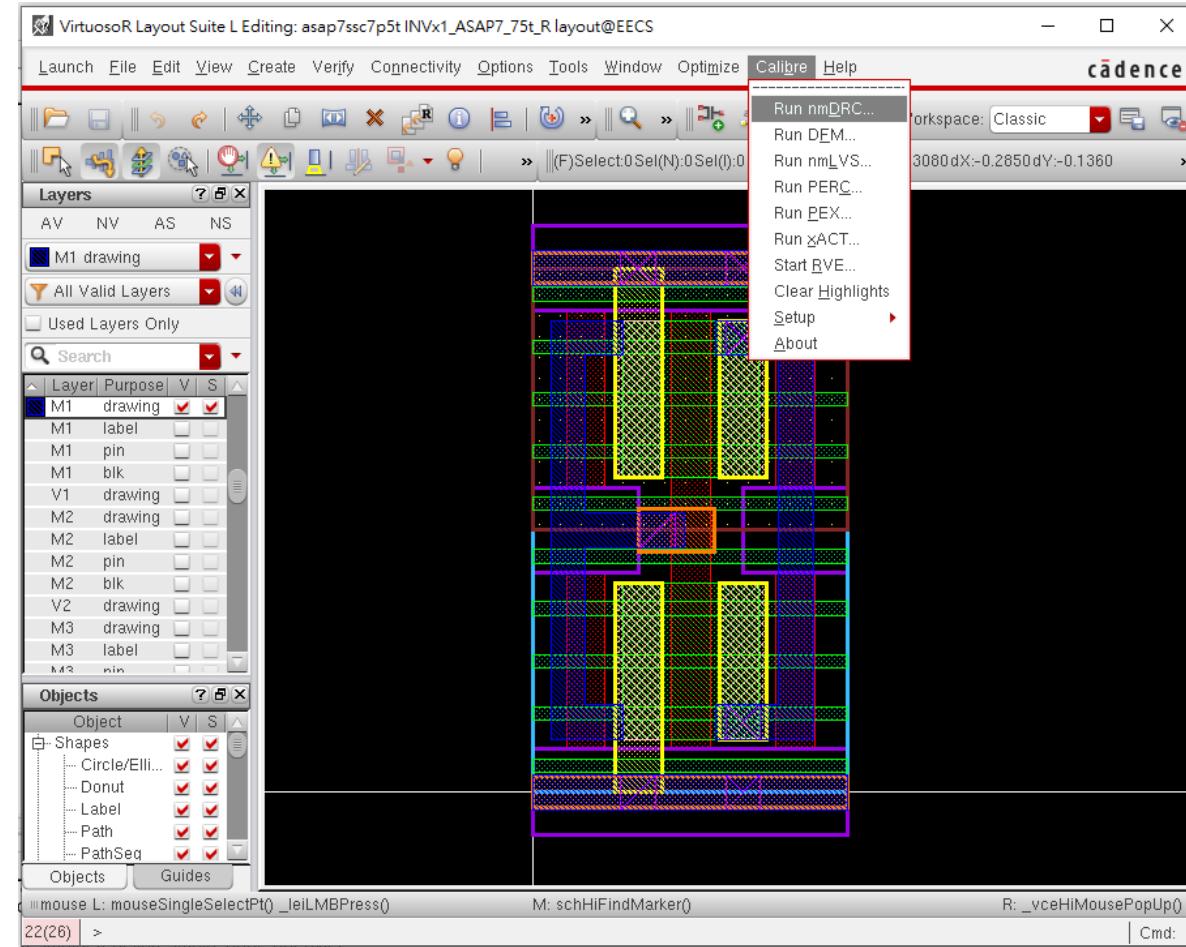
rm file : remove a file

cat file : display a file

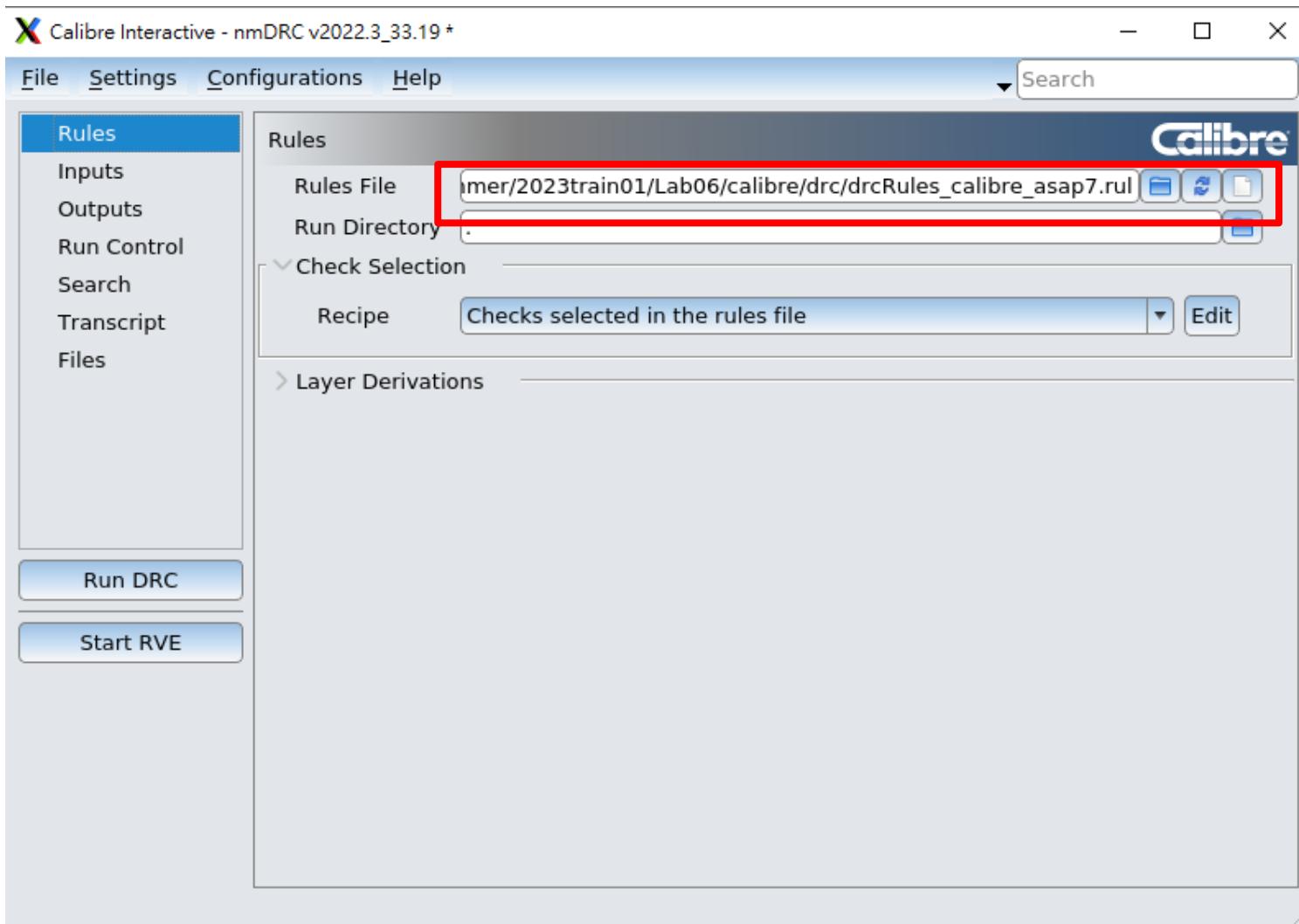
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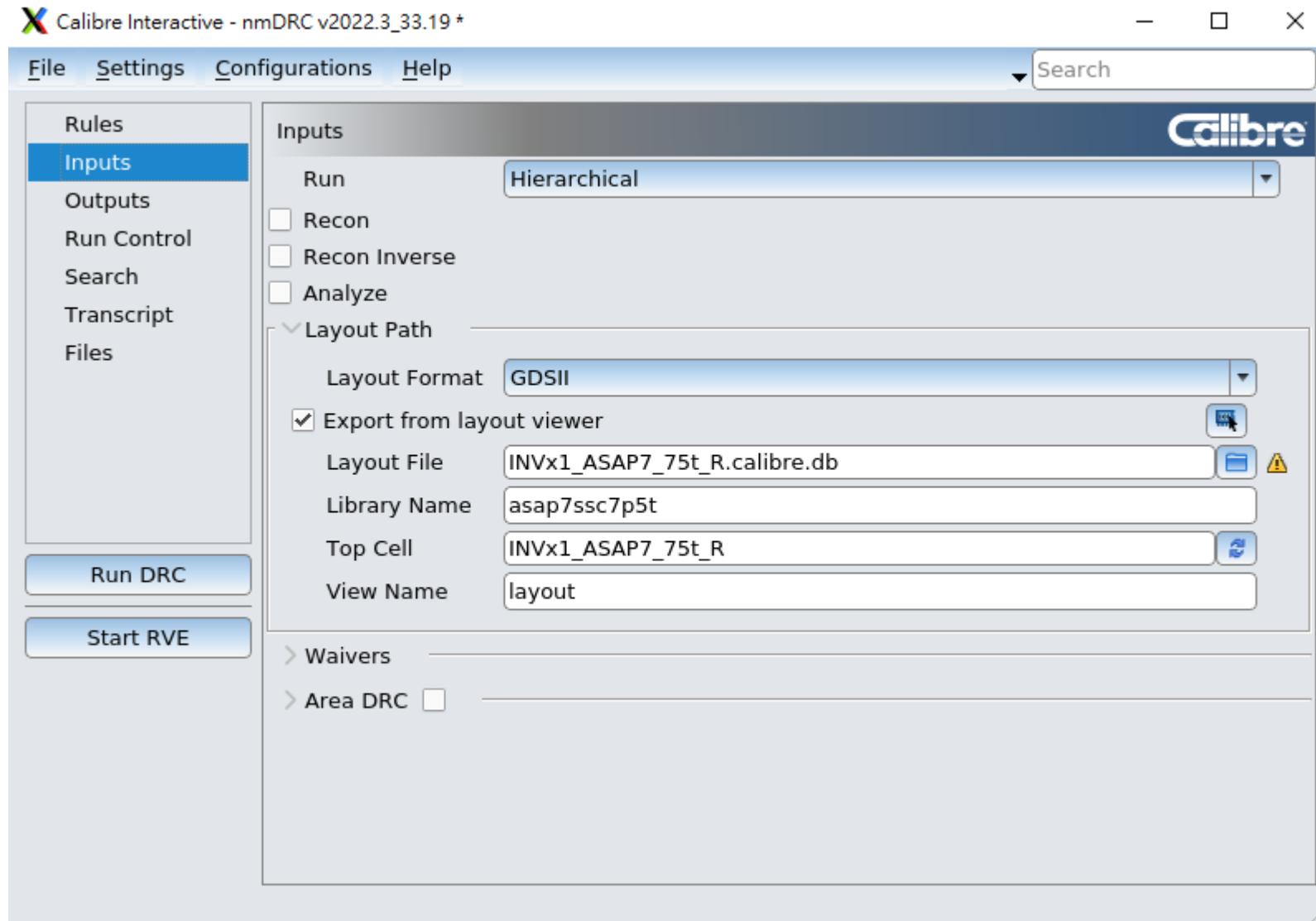
Run DRC



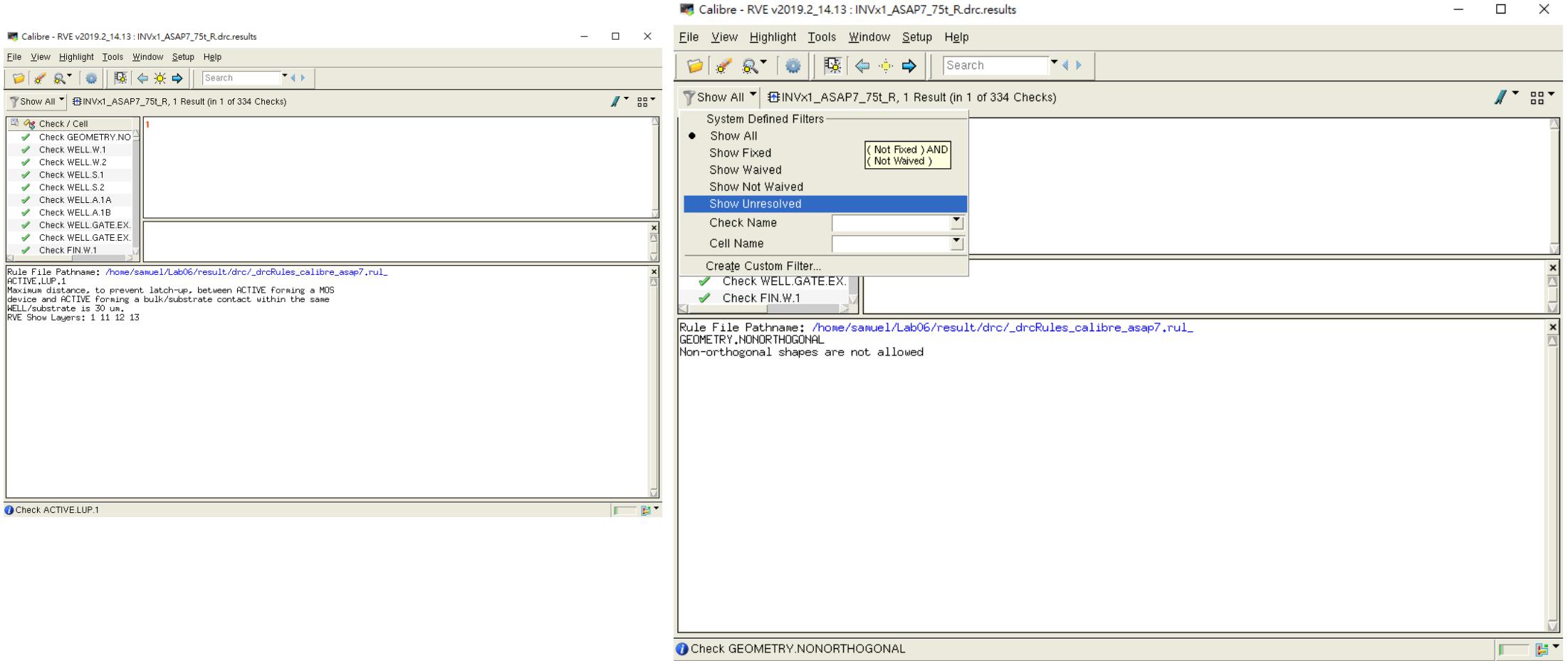
Run DRC



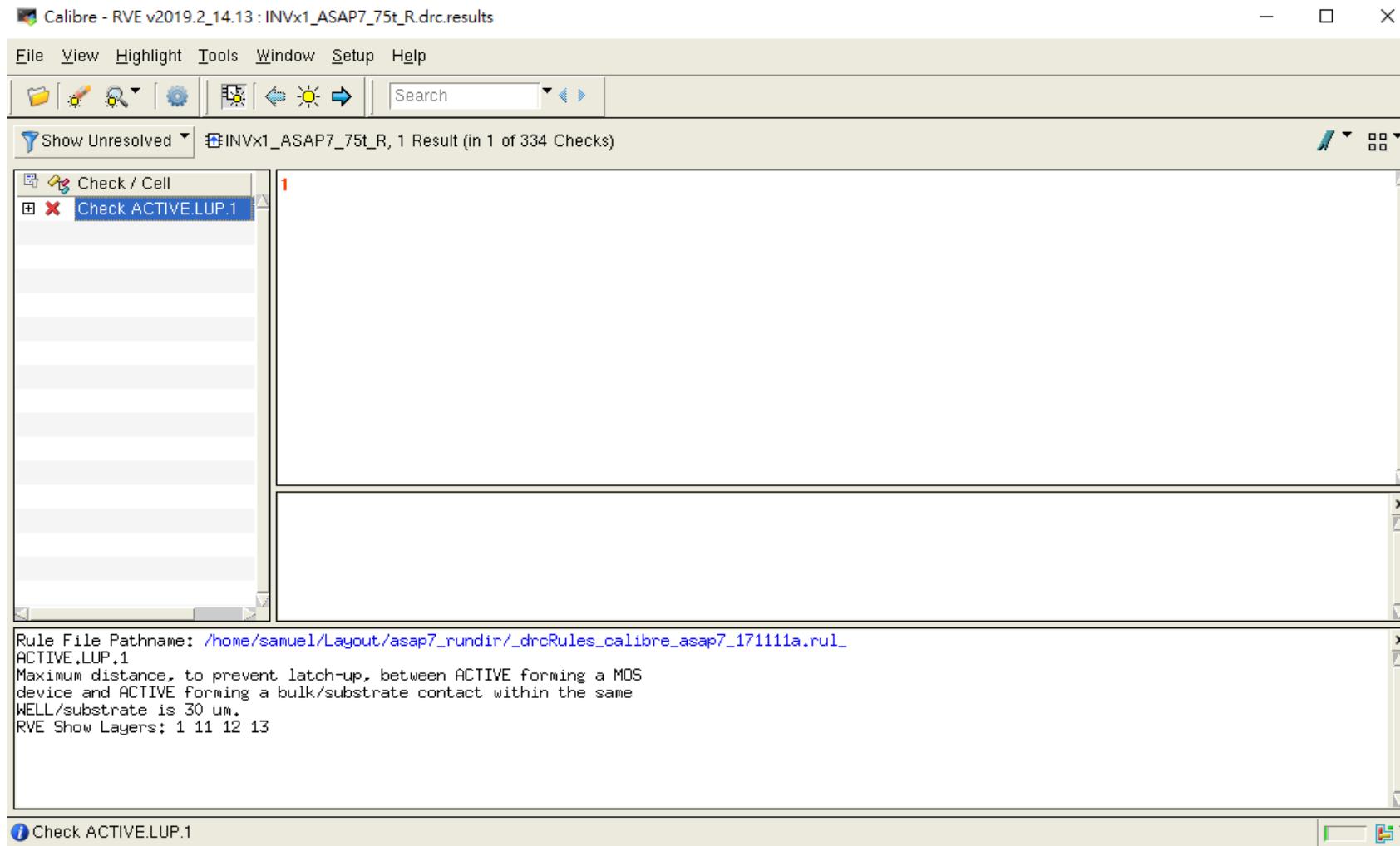
Run DRC



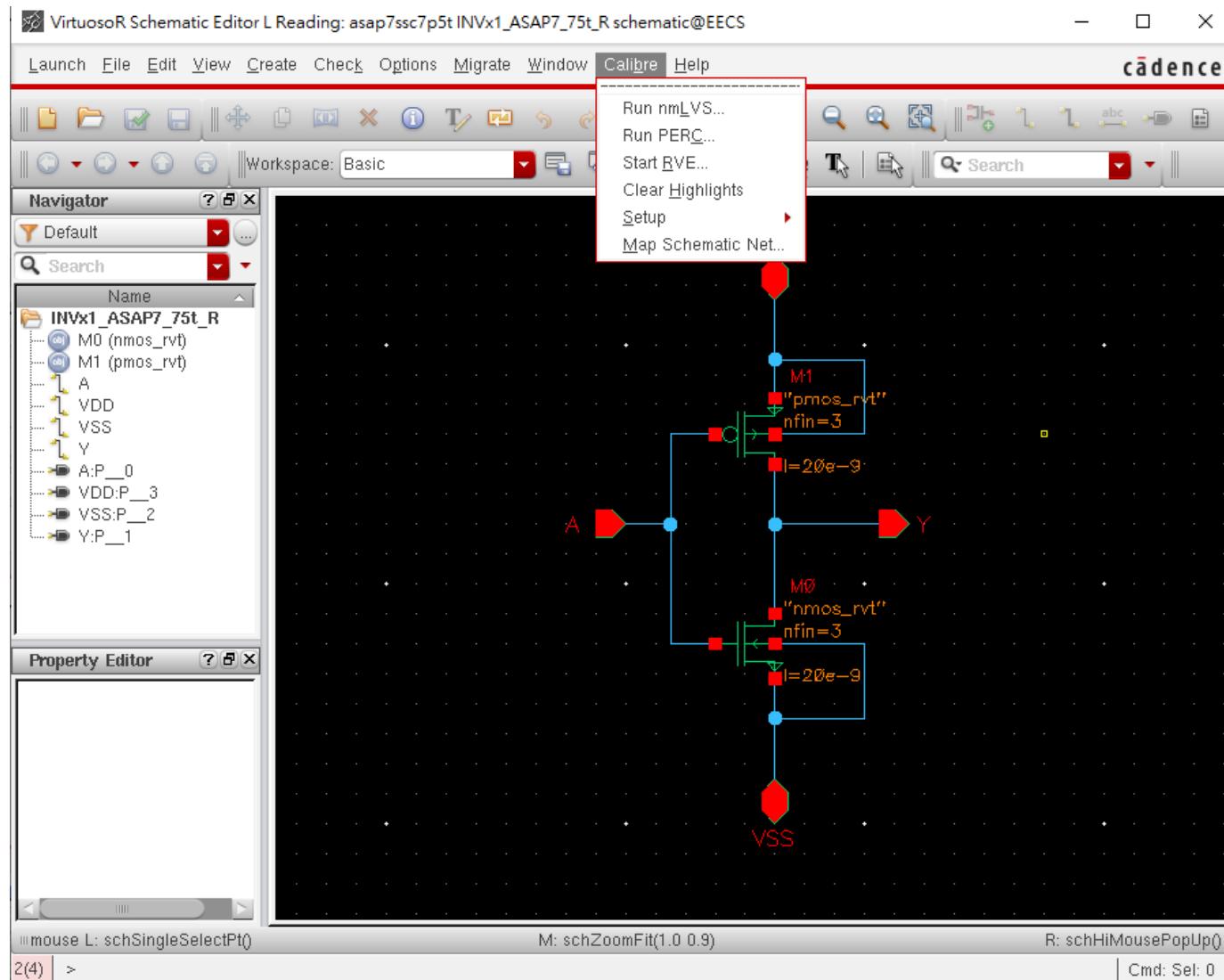
DRC 預期結果



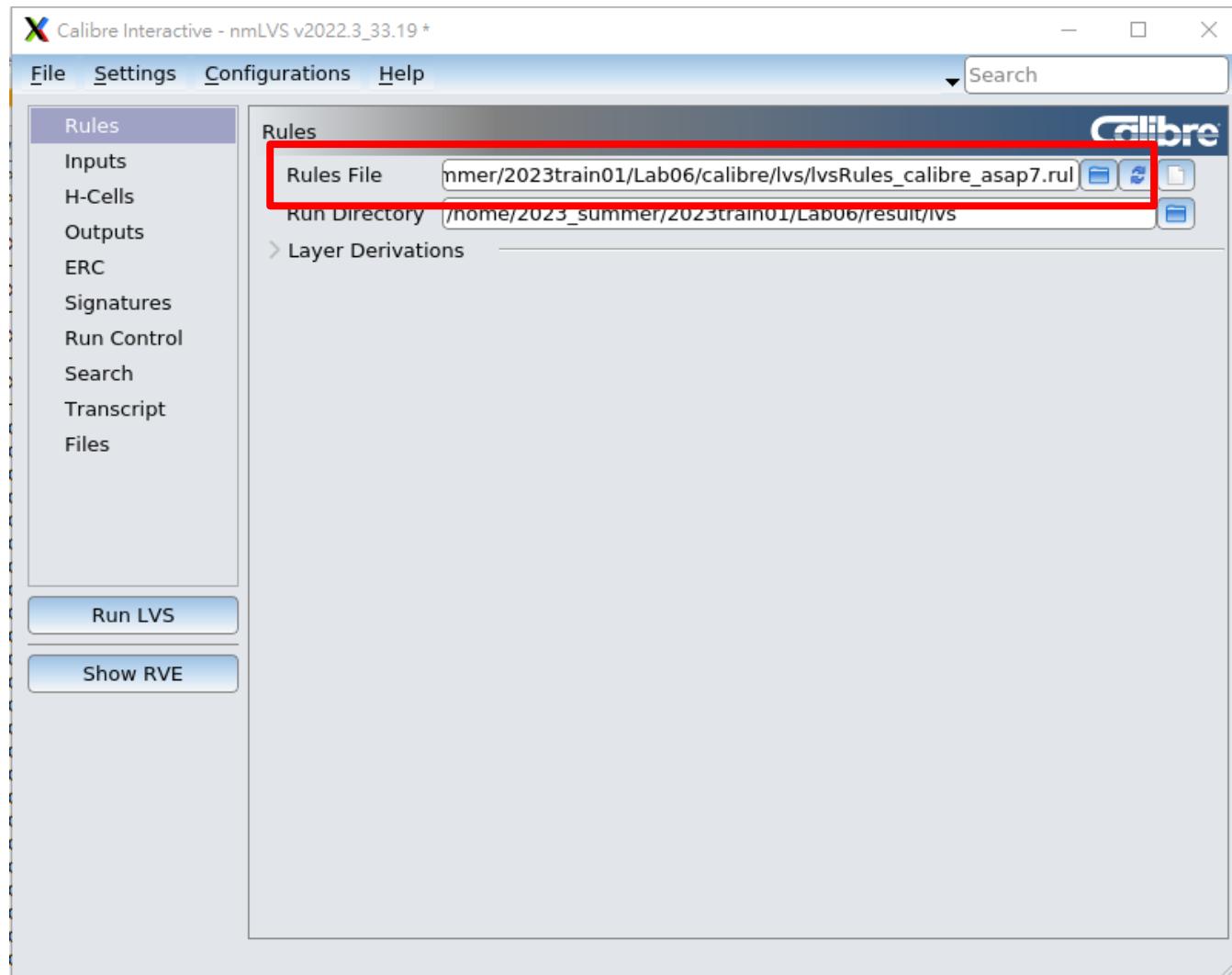
可忽略的錯誤



Run LVS

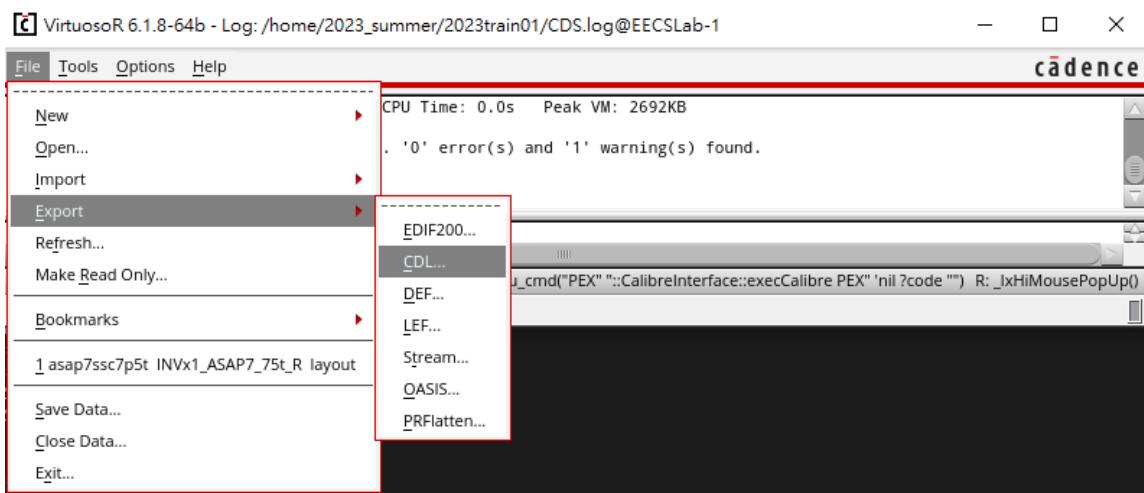


Run LVS – rule setting

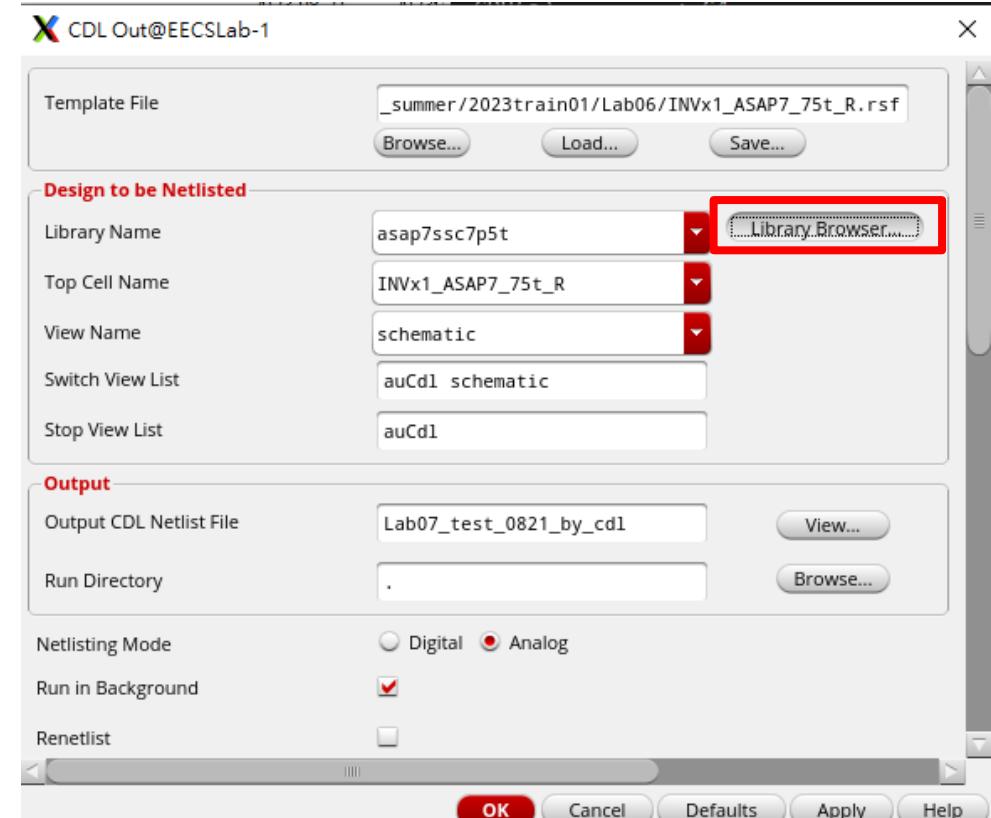


Run LVS – translate sp file by CDL - 1

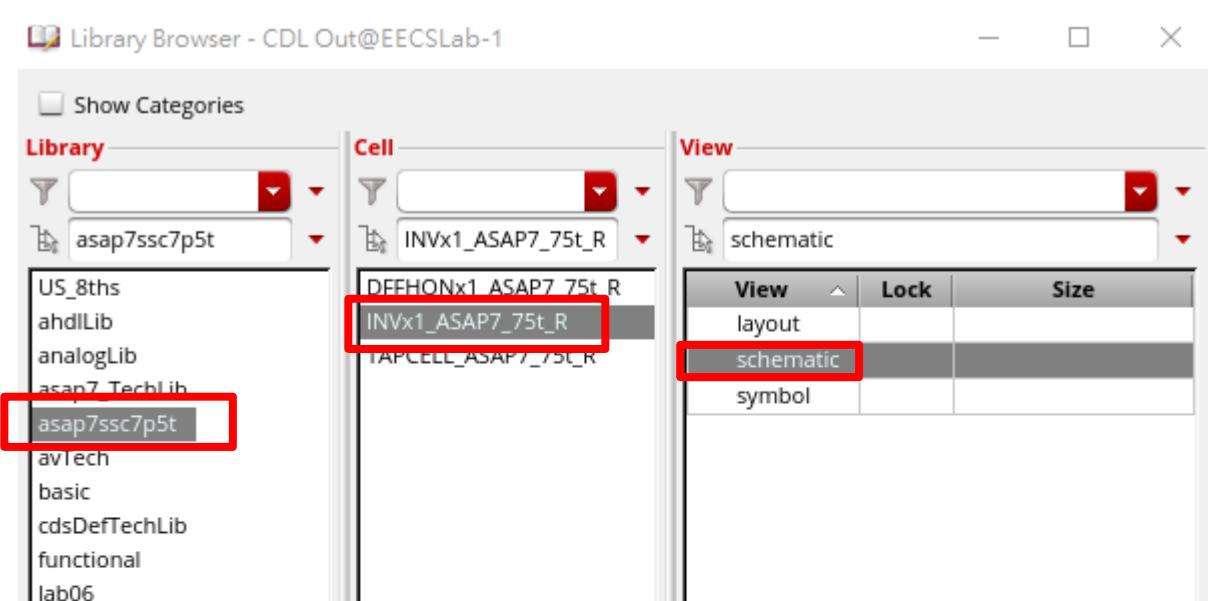
1.



2.



3.



Run LVS – translate sp file by CDL - 2

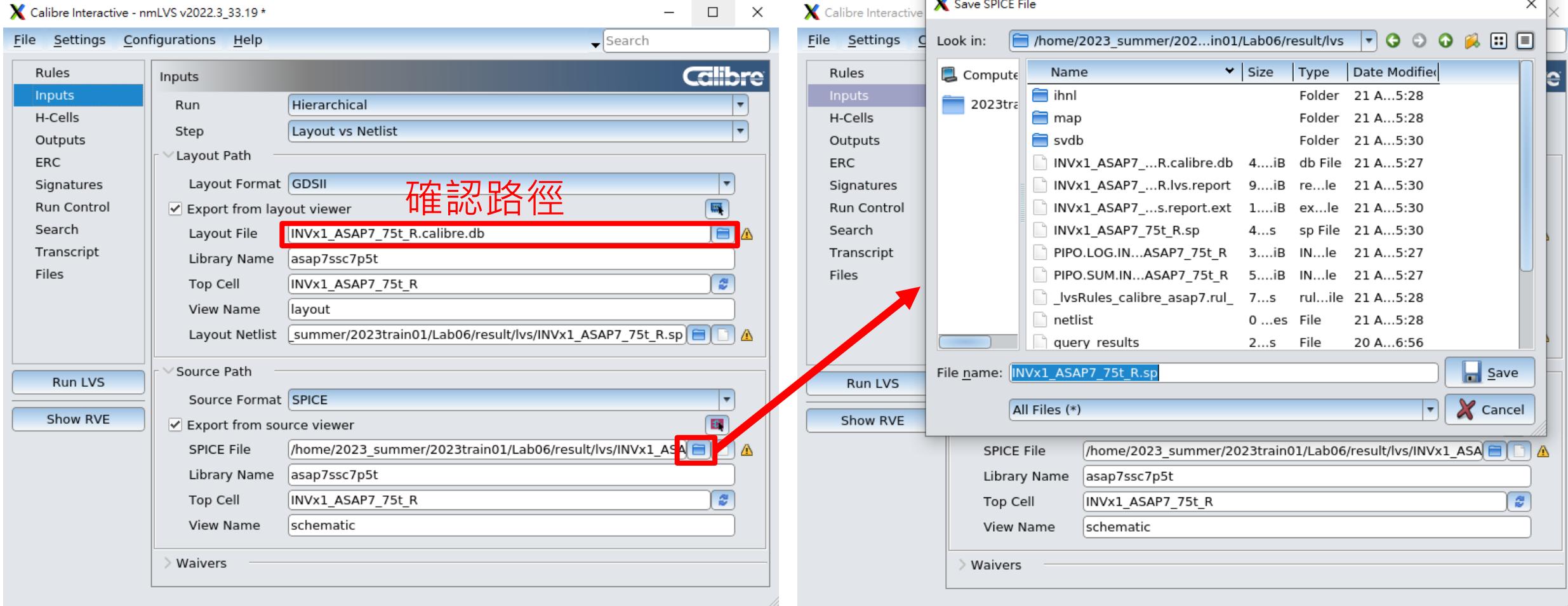
4.

The screenshot shows two windows from the Cadence VirtuosoR 6.1.8-64b interface. The top window is a terminal session titled 'c ./Lab07_test_0821_by_cdl@EECSLab-1'. It displays a netlist header and a portion of an SPICE-like script. A red box highlights the following code:

```
.SUBCKT INVx1_ASAP7_75t_R A VDD VSS Y
.*PININFO A:I Y:O VDD:B VSS:B
MM0 Y A VSS VSS nmos_rvt w=81.0n l=20n nfin=3
MM1 Y A VDD VDD pmos_rvt w=81.0n l=20n nfin=3
.ENDS
```

A modal dialog box titled 'Analysis Job Succeeded@EECSLab-1' is overlaid on the terminal window, indicating that a job started at 'Aug 21 20:30:34 2023' has succeeded. The bottom window is also titled 'c VirtuosoR 6.1.8-64b - Log: /home/2023_summer/2023train01/CDS.log@EECSLab-1'. It shows log messages related to initializing the simulation environment and the status of the CDL Out translation process.

Run LVS



Run LVS debug

```
lab06_cdl_outputnetlist.sp X
C: > Users > USER > AppData > Roaming > MobaXterm > slash > RemoteFiles > 39584
1 ****
2 * auCdl Netlist:
3 *
4 * Library Name: lab06
5 * Top Cell Name: INV
6 * View Name: schematic
7 * Netlisted on: Aug 1 19:47:24 2023
8 ****
9
10 *.BIPOLAR
11 *.RESI = 2000
12 *.RESVAL
13 *.CAPVAL
14 *.DIOPERI
15 *.DIOAREA
16 *.EQUATION
17 *.SCALE METER
18 *.MEGA
19 .PARAM
20
21
22
23 ****
24 * Library Name: lab06
25 * Cell Name: INV
26 * View Name: schematic
27 ****
28
29 .SUBCKT INV A VDD VSS Y
30 *.PININFO A:I Y:O VDD:B VSS:B
31 MM0 Y A VSS VSS nmos_rvt w=81.0n l=20n nfin=3
32 MM1 Y A VDD VDD pmos_rvt w=81.0n l=20n nfin=3
33 .ENDS
34
35
```

By CDL

```
lab06_cdl_outputnetlist.sp X
C: > Users > USER > AppData > Roaming > MobaXterm > slash > RemoteFiles > 39584
1 ****
2 * auCdl Netlist:
3 *
4 * Library Name: lab06
5 * Top Cell Name: INV
6 * View Name: schematic
7 * Netlisted on: Aug 1 19:47:24 2023
8 ****
9
10 *.BIPOLAR
11 *.RESI = 2000
12 *.RESVAL
13 *.CAPVAL
14 *.DIOPERI
15 *.DIOAREA
16 *.EQUATION
17 *.SCALE METER
18 *.MEGA
19 .PARAM
20
21
22
23 ****
24 * Library Name: lab06
25 * Cell Name: INV
26 * View Name: schematic
27 ****
28
29 .SUBCKT INV VSS VDD A Y 9 10
30 *.PININFO A:I Y:O VDD:B VSS:B
31 MM0 Y A VSS 9 nmos_rvt w=81.0n l=20n nfin=3
32 MM1 Y A VDD 10 pmos_rvt w=81.0n l=20n nfin=3
33 .ENDS
34
35
```

After debug
by yourself

Run LVS - result

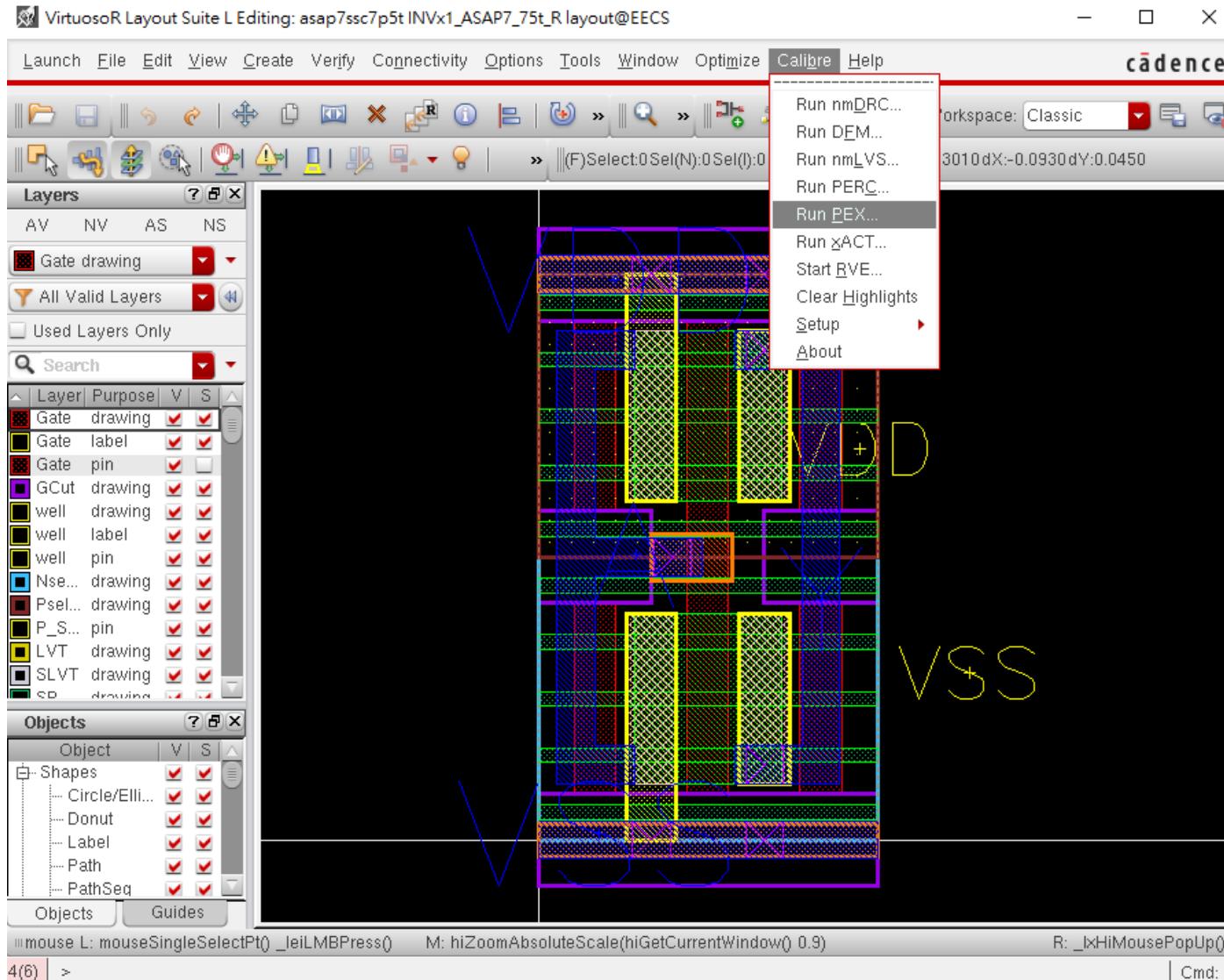
```
LVS Report File - INV.lvs.report
File Edit Options Windows

#####
##          C A L I B R E      S Y S T E M      ##
##          L V S      R E P O R T      ##
##          #####
REPORT FILE NAME:           INV.lvs.report
LAYOUT NAME:                /home/2022_fall/Ricky/Lab06/INV.sp ('INV')
SOURCE NAME:                /home/2022_fall/Ricky/Lab06/lab06_cdl_outputnetlist.sp ('INV')
RULE FILE:                  /home/2022_fall/Ricky/Lab06/_lvsRules_calibre_asap7.rul_
RULE FILE TITLE:            LVS Rule File for ASAP7 PDK
CREATION TIME:              Tue Aug  1 20:11:31 2023
CURRENT DIRECTORY:          /home/2022_fall/Ricky/Lab06
USER NAME:                  Ricky
CALIBRE VERSION:            v2019.2_14.13   Tue Apr 9 20:09:15 PDT 2019

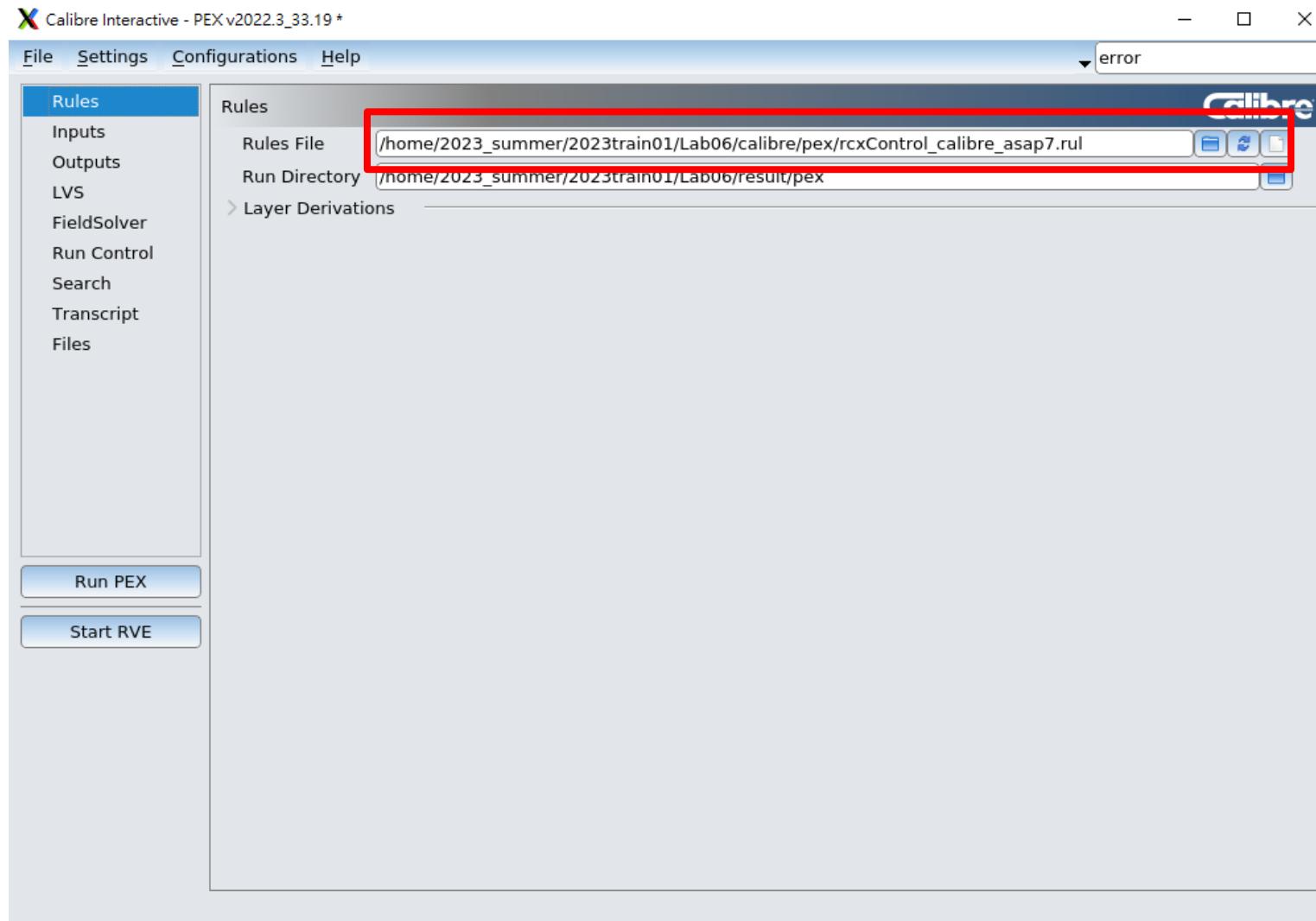
OVERALL COMPARISON RESULTS

      #
      #      #####
      #      #      #
      #      #      #      *
      #      #      #      -
      #      #      #      \_/
      #
      #####
```

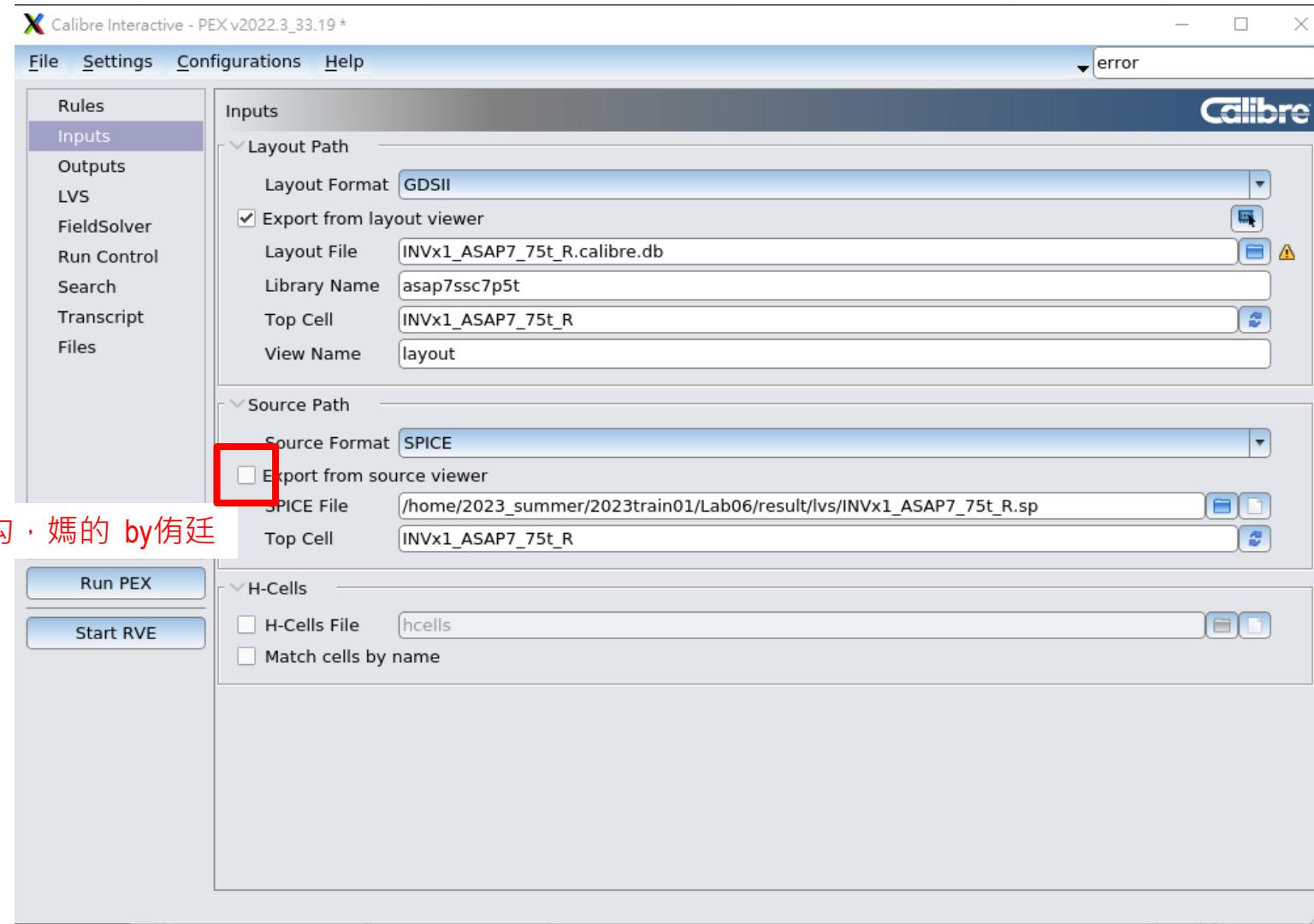
Post layout Simulation



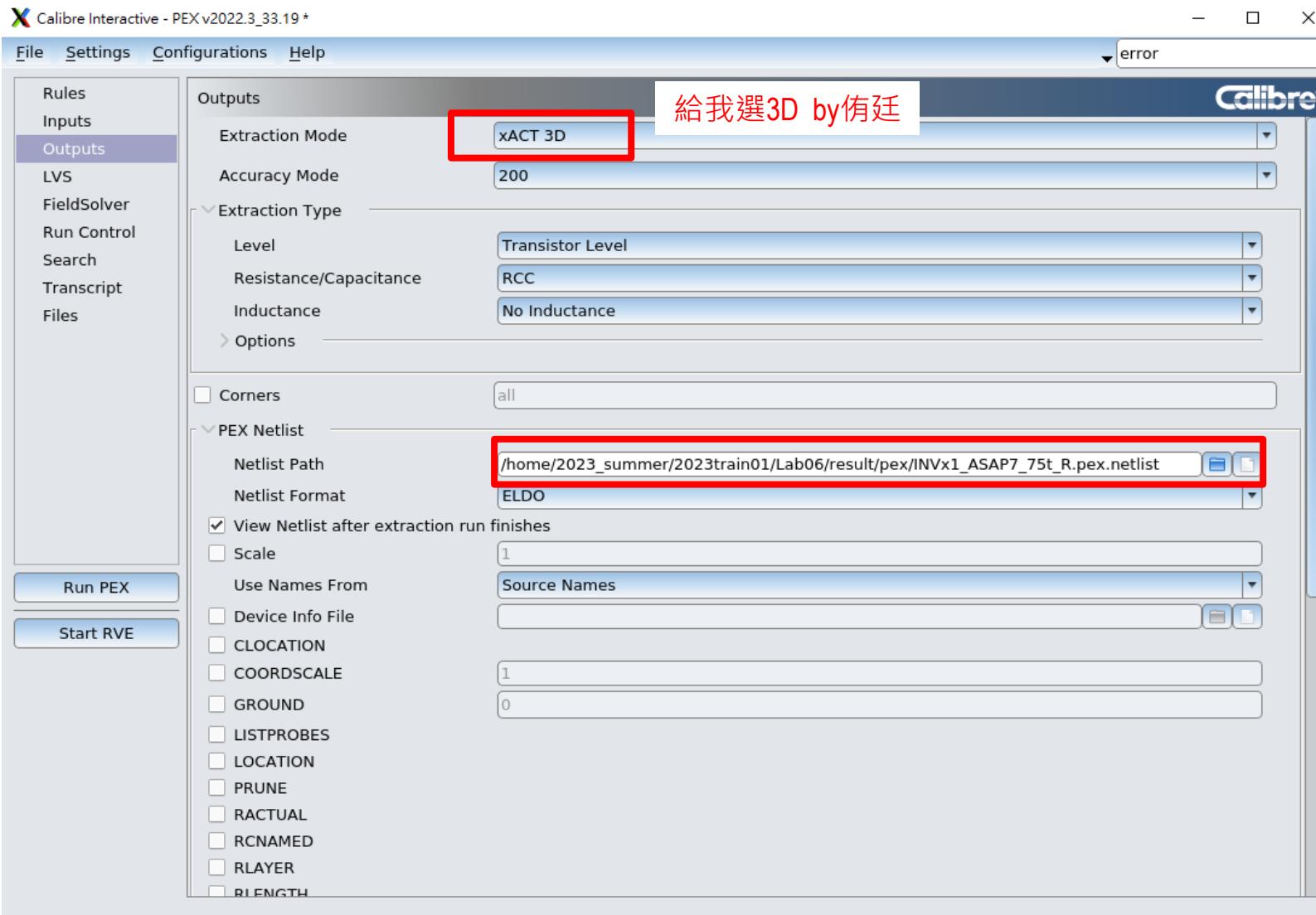
Post layout Simulation – setting



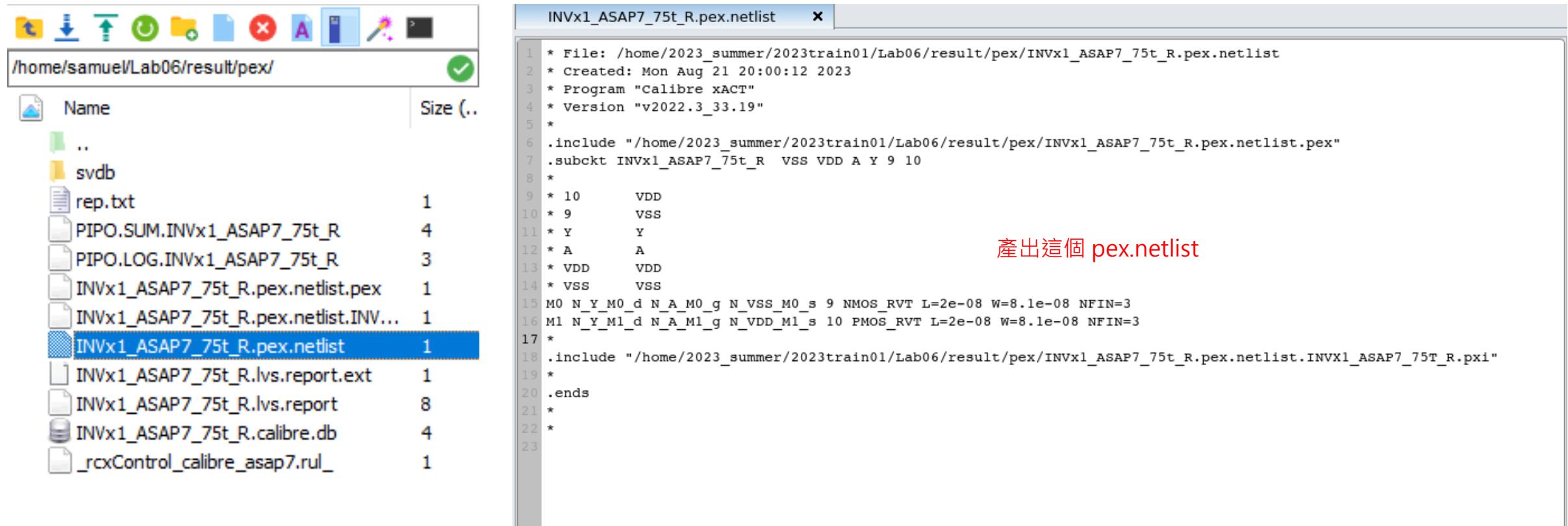
Post layout Simulation – setting points 1



Post layout Simulation – setting points 2



Check PEX output result



The image shows a terminal window and a text editor side-by-side.

The terminal window on the left displays a file list in a directory:

```
/home/samuel/Lab06/result/pex/
```

Name	Size ..
..	
svdb	
rep.txt	1
PIPO.SUM.INVx1_ASAP7_75t_R	4
PIPO.LOG.INVx1_ASAP7_75t_R	3
INVx1_ASAP7_75t_R.pex.netlist.pex	1
INVx1_ASAP7_75t_R.pex.netlist.INV...	1
INVx1_ASAP7_75t_R.pex.netlist	1
INVx1_ASAP7_75t_R.lvs.report.ext	1
INVx1_ASAP7_75t_R.lvs.report	8
INVx1_ASAP7_75t_R.calibre.db	4
_rcxControl_calibre_asap7.rul_	1

The text editor on the right shows the content of the selected file:

```
INVx1_ASAP7_75t_R.pex.netlist x  
1 * File: /home/2023_summer/2023train01/Lab06/result/pex/INVx1_ASAP7_75t_R.pex.netlist  
2 * Created: Mon Aug 21 20:00:12 2023  
3 * Program "Calibre xACT"  
4 * Version "v2022.3_33.19"  
5 *  
6 .include "/home/2023_summer/2023train01/Lab06/result/pex/INVx1_ASAP7_75t_R.pex.netlist.pex"  
7 .subckt INVx1_ASAP7_75t_R VSS VDD A Y 9 10  
8 *  
9 * 10 VDD  
10 * 9 VSS  
11 * Y Y  
12 * A A  
13 * VDD VDD  
14 * VSS VSS  
15 M0 N_Y_M0_d N_A_M0_g N_VSS_M0_s 9 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3  
16 M1 N_Y_M1_d N_A_M1_g N_VDD_M1_s 10 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3  
17 *  
18 .include "/home/2023_summer/2023train01/Lab06/result/pex/INVx1_ASAP7_75t_R.pex.netlist.INVx1_ASAP7_75T_R.pxi"  
19 *  
20 .ends  
21 *  
22 *  
23 *
```

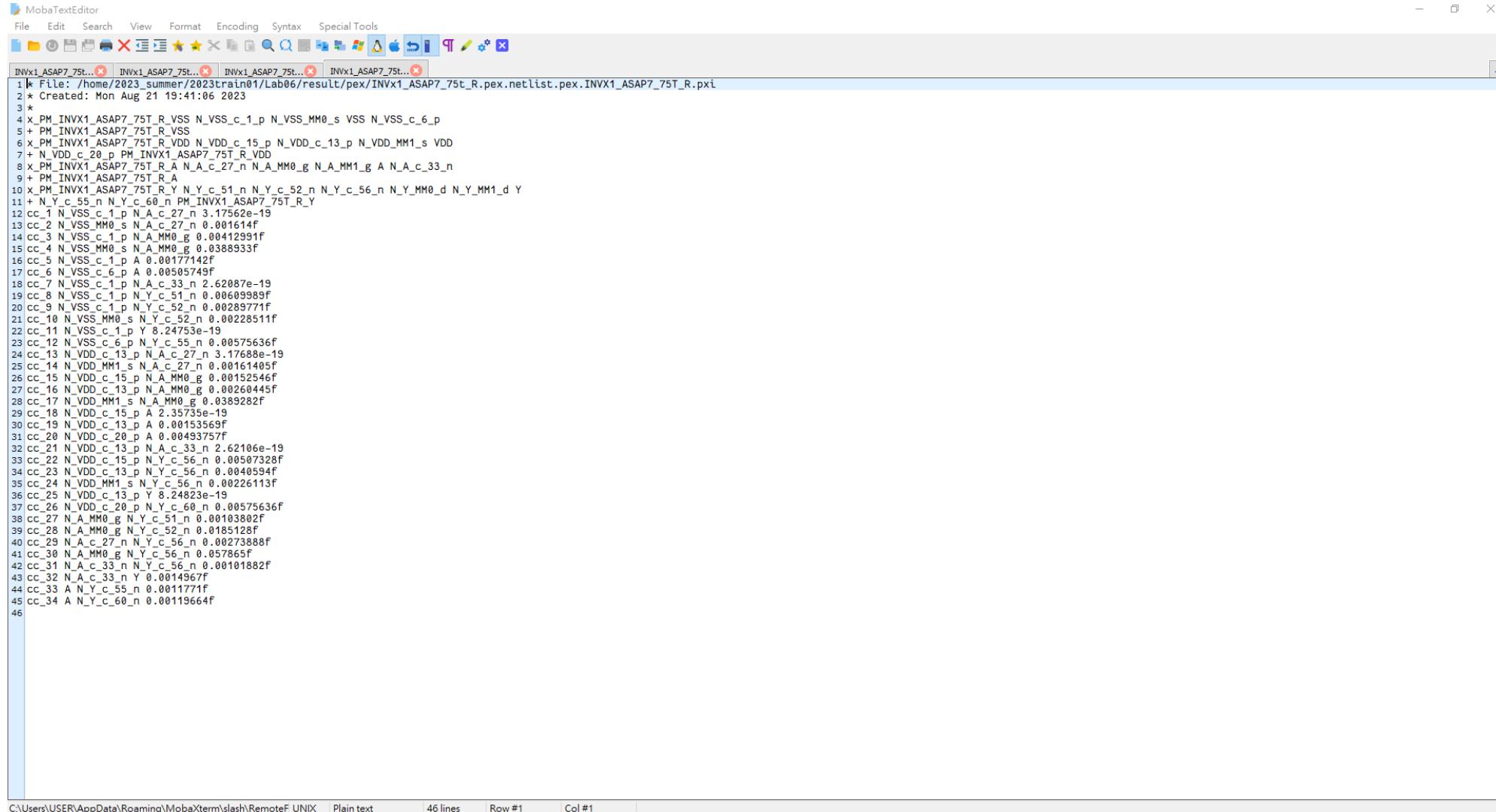
A red annotation "產出這個 pex.netlist" is placed next to the file name in the terminal list.

PEX output result add setting

```
* Created: Thu Aug 29 00:41:00 2019
* Program "Calibre xRC"
* Version "v2019.2_14.13"
*
.global vdd vss
.include '/home/train_ta/asap7PDK_r1p5/models/hspice/7nm_SS.pm'
.include "/home/samuel/Lab06/result/pex/INVx1_ASAP7_75t_R.pex.netlist.pex"
.subckt INVx1_ASAP7_75t_R VSS VDD A Y 9 10
*
* 10    VDD
* 9 VSS
* Y Y
* A A
* VDD    VDD
* VSS    VSS
M0 Y A VSS 9 NMOS RVT L=2e-08 W=8.1e-08 NFIN=3
M1 Y A VDD 10 PMOS RVT L=2e-08 W=8.1e-08 NFIN=3
*
.include "/home/samuel/Lab06/result/pex/INVx1_ASAP7_75t_R.pex.netlist.INVX1_ASAP7_75T_R.pxi"
*
.ends
*
*
xinverter VSS VDD A Y vss vdd INVx1_ASAP7_75t_R
vvdd vdd 0 0.7v
Vvss vss 0 0v
VA A 0 PULSE ( 0V 0.7V 1ns 0.1ns 0.1ns 10ns 20.2ns)
.tran 0.05ns 60ns
****|option ctrl****
.op
.option post
.options probe           *with I/V in .lis
.probe v(*) i(*)         *with cap value in .lis
.option captab            *with cap value in .lis
.end
```

加入製程設定檔案

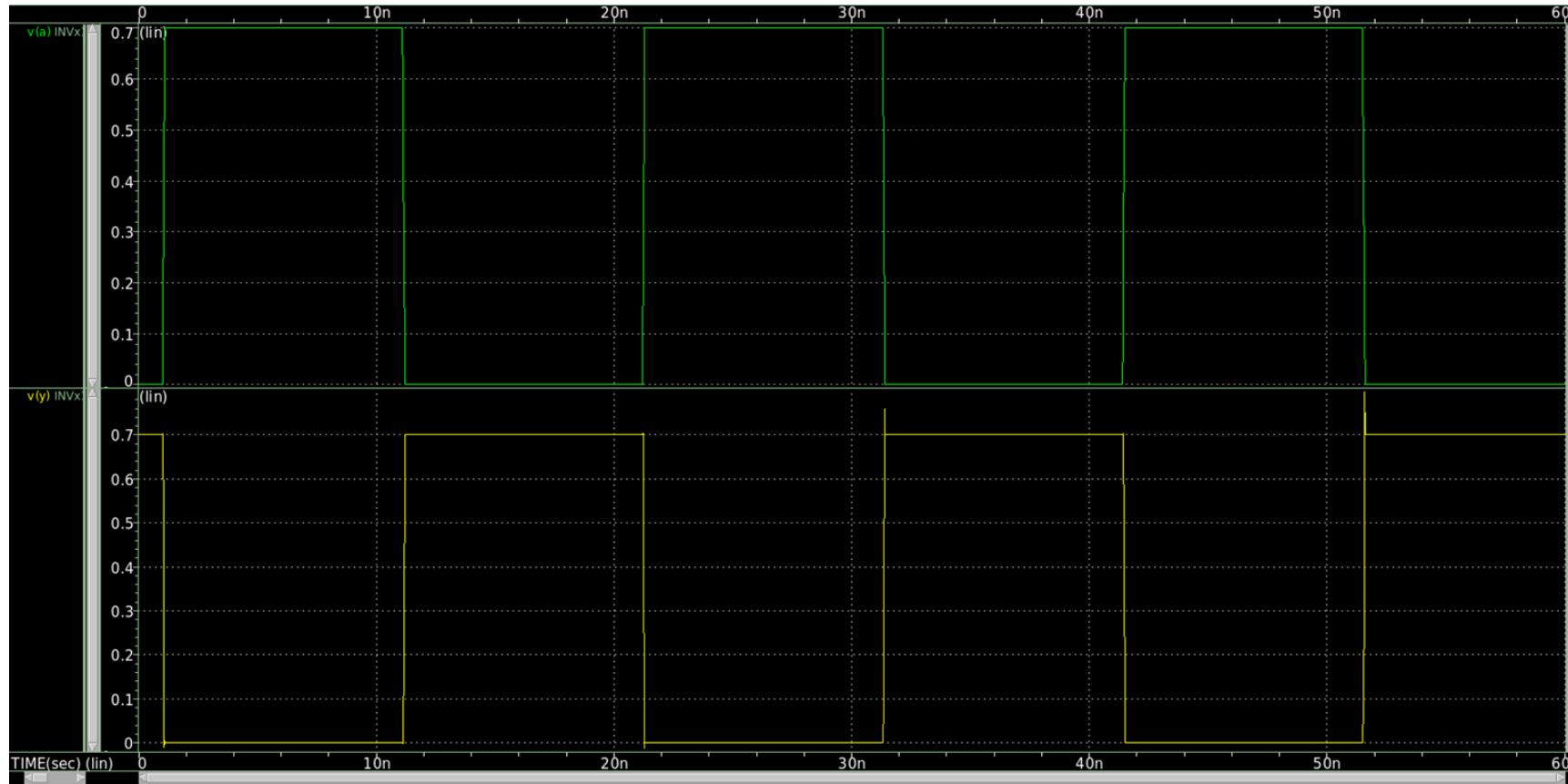
PEX RC information - result



The screenshot shows a window titled "MobaTextEditor" displaying a text file with the following details:

- File: /home/2023_summer/2023train01/Lab06/result/pex/INVx1_ASAP7_75t_R.pex.netlist.pex.INVx1_ASAP7_75T_R.pkl
- Created: Mon Aug 21 19:41:06 2023
- Content: A large block of text representing PEX RC information, starting with line 1 and ending at line 46. The text includes various component names like X_PM_INVX1_ASAP7_75T_R_VSS, connection types (p, n), and values (e.g., 0.001614f, 0.00412991f).

Post layout Simulation - waveview



Post layout Simulation - report

The image shows two windows side-by-side. On the left is the "Calibre Interactive - PEX v2019.2_14.13" window, which contains a transcript of the simulation process. On the right is the "PEX Netlist File - INVx1_ASAP7_75t_R.pex.netlist" window, which displays the generated netlist file.

Calibre Interactive - PEX v2019.2_14.13 Transcript:

```
// liability or otherwise, in no event shall Mentor Graphics
// liability exceed the amount paid for the product giving rise
// to the claim.
//
INFO: Map for layout placement hierarchy takes 1.6440e-02 Mbytes.
INFO: Net summary reporting completed.

--- NET SUMMARY REPORTING ENDING TIME - Thu Aug 29 00:31:39 2019
--- TOTAL CPU TIME = 0 REAL TIME = 0 LVHEAP = 3/9/268 MALLOC = 108/:

=====
CALIBRE xRC WARNING / ERROR Summary
-----
xRC Warnings = 2
xRC Errors = 0
=====

--- CALIBRE xRC::FORMATTER COMPLETED - Thu Aug 29 00:31:39 2019
--- TOTAL CPU TIME = 0 REAL TIME = 1 LVHEAP = 3/9/268 MALLOC = 108/:
```

PEX Netlist File - INVx1_ASAP7_75t_R.pex.netlist:

```
* File: INVx1_ASAP7_75t_R.pex.netlist
* Created: Thu Aug 29 00:31:37 2019
* Program "Calibre xRC"
* Version "v2019.2_14.13"
*
.inclu "INVx1_ASAP7_75t_R.pex.netlist.pex"
.subckt INVx1_ASAP7_75t_R VSS VDD A Y 9 10
*
* 10 VDD
* 9 VSS
* Y Y
* A A
* VDD VDD
* VSS VSS
M0 N_Y_M0_d N_A_M0_g N_VSS_M0_s 9 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
M1 N_Y_M1_d N_A_M1_g N_VDD_M1_s 10 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
*
.inclu "INVx1_ASAP7_75t_R.pex.netlist.INVx1_ASAP7_75T_R.pxi"
*
.ends
*
*
```

Reference

- http://venividiki.ee.virginia.edu/mediawiki/index.php/FinFET_ASAP7_CellLayout

目錄

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- 7nm inv, dff LVS + DRC verification
- Display setting / 常用 Hotkey
- Layout DRC / LVS Flow
- Ring Oscillator 環形振盪器介紹
- 本次 lab 題目 Ring Oscillator 要求、通過條件
- 附件補充

Ring Oscillator 環形振盪器

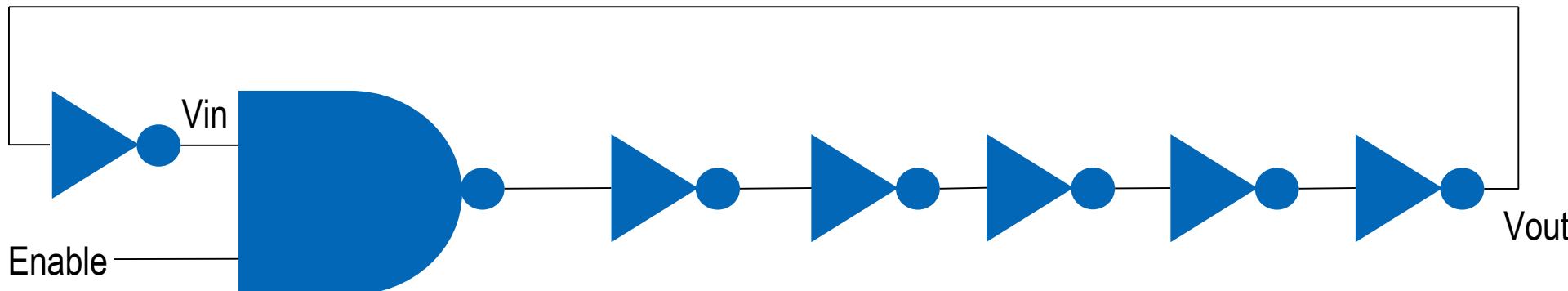
- 由 inverters組成，連接成一個閉環，產生持續的振盪、生成頻率，而頻率主要取決於每個反向器的延遲。
 - 因此可以通過改變反向器的特性與數量來調節頻率。
-
- 用於頻率參考：在某些情境下，可用作頻率參考源，特別是在缺乏其他穩定時鐘源時。
 - 用於電壓控制振蕩器 (VCO)：與電壓控制元件結合使用時，可用作VCO，通過控制電壓調節頻率。
 - 用於快速啟動時鐘：用於一些低功耗模式，因簡單的結構和快速的啟動時間。

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本次 lab 題目 Ring Oscillator

- >7 stages ring oscillator
- M1 for local connection(Vertical or Horizontal)
- M2 for power rail (only horizontal)
- M3 for power rail (only vertical)
- Block diagram as below:



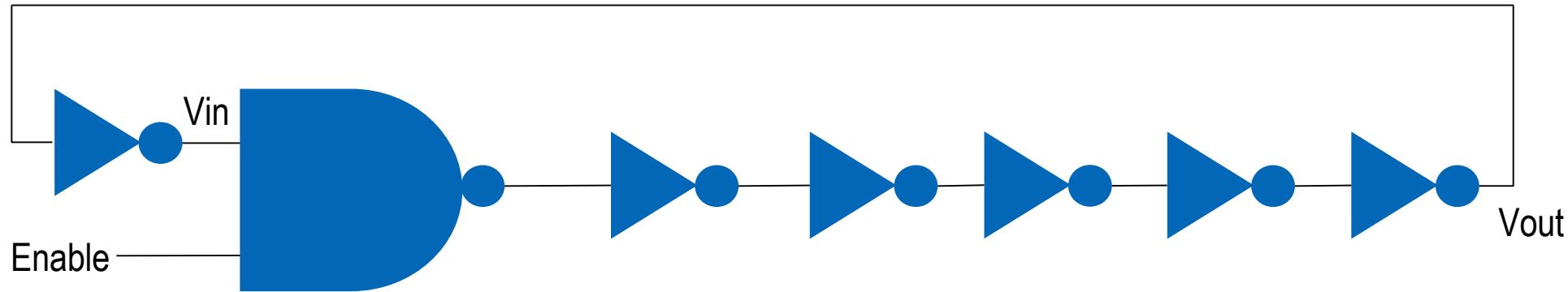
NAND SP檔 提示

```
.SUBCKT nand2 VSS VDD enable vin Y
M2  Y  enable  VDD 13 pmos_rvt L=2e-08 W=8.1e-08 nfin=3
M3  Y  vin      VDD 13 pmos_rvt L=2e-08 W=8.1e-08 nfin=3
M0  Y  enable  net 15 nmos_rvt L=2e-08 W=8.1e-08 nfin=3
M1  net vin    VSS 15 nmos_rvt L=2e-08 W=8.1e-08 nfin=3
.ENDS
```

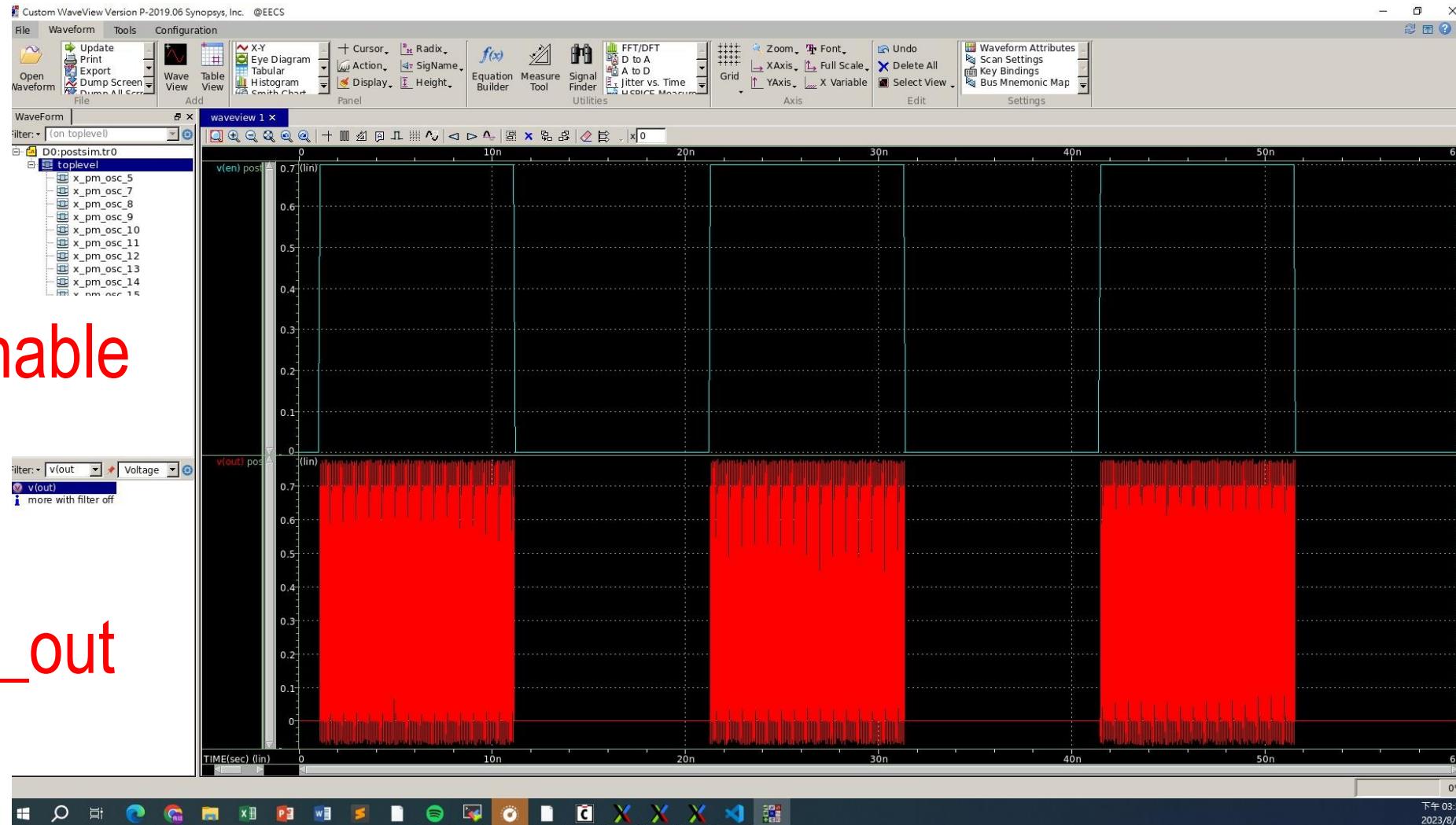
本次 lab 題目 Ring Oscillator

- Design function:

Enable=1,Vout=clock signal; Enable=0,Vout=0



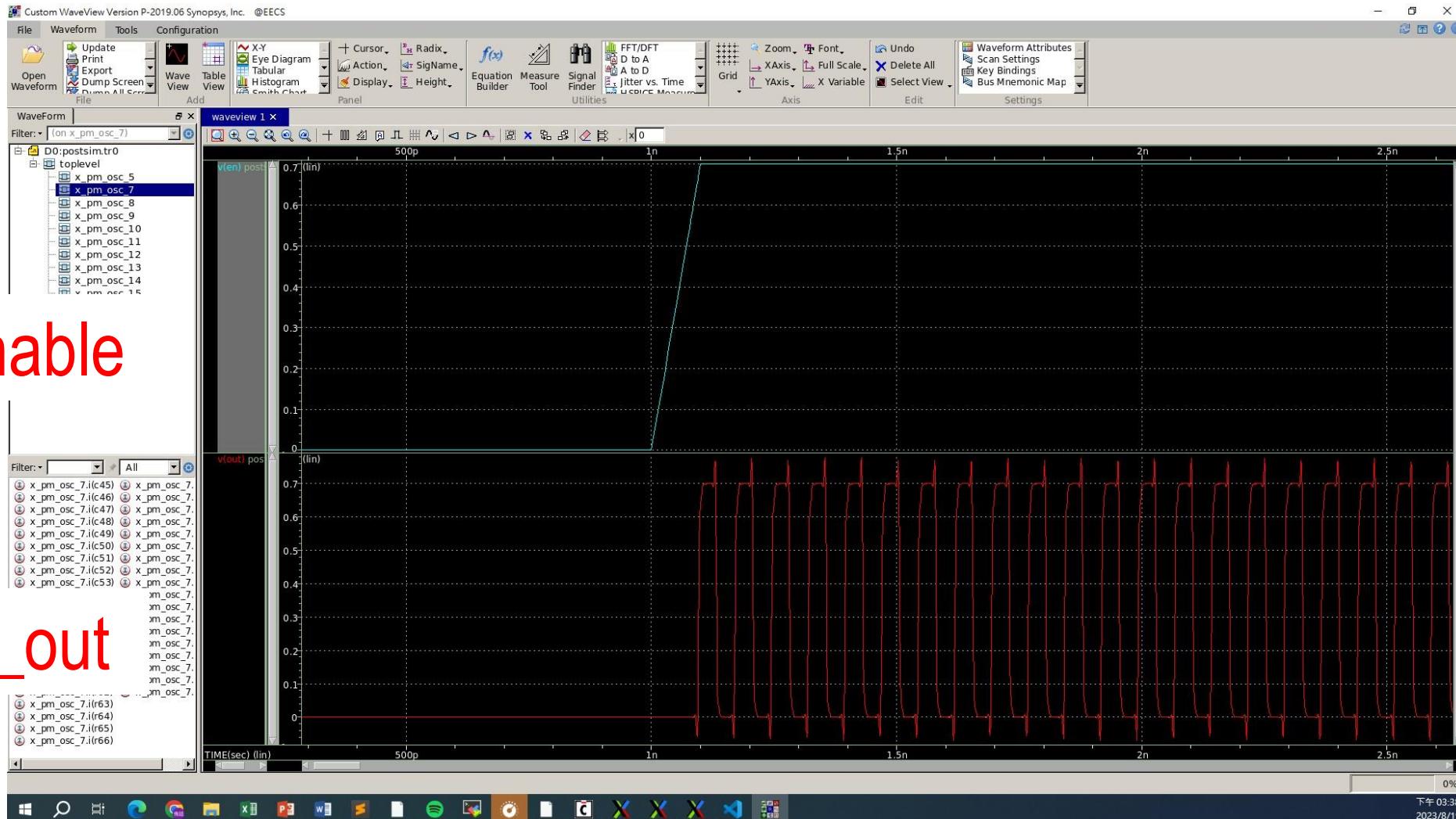
預期輸出波型 - 以10個inv為例_1



V_enable

V_out

預期輸出波型 - 以10個inv為例_2



預期 PEX 抽出 RC 資訊

```
osc.pex.netlist.pex ✘
1 * File: osc.pex.netlist.pex
2 * Created: Sat Aug 19 15:22:00 2023
3 * Program "Calibre xACT"
4 * Version "v2019.2_14.13"
5 * Nominal Temperature: 25C
6 * Circuit Temperature: 27C
7 *
8 .subckt PM_OSC_VSS 1 6 11 14 16 21 24 26 31 34 36 41 44 46 51 54 56
9 + 153 155 160 167 169 172 177 196
10 c146 196 0 0.0884248f
11 c147 177 0 0.00216735f
12 c148 172 0 0.00203959f
13 c149 169 0 0.00205688f
14 c150 167 0 0.00205688f
15 c151 160 0 0.00212338f
16 c152 155 0 0.00224212f
17 c153 153 0 0.00458482f
18 c154 111 0 0.0110036f
19 c155 108 0 0.101003f
20 c156 56 0 0.0153569f
21 c157 54 0 0.038094f
22 c158 46 0 0.0352241f
23 c159 44 0 0.0373541f
24 c160 36 0 0.0352973f
25 c161 34 0 0.0373541f
26 c162 26 0 0.0352973f
27 c163 24 0 0.0373369f
28 c164 16 0 0.0352973f
29 c165 14 0 0.037152f
30 c166 6 0 0.0352973f
31 c167 1 0 0.0355913f
32 r168 196 252 13.2616
33 r169 196 197 90.9117
34 r170 193 242 13.2616
35 r171 193 197 286.721
36 r172 193 194 90.9117
37 r173 190 232 13.2616
38 r174 190 194 286.721
39 r175 190 191 90.9117
40 r176 186 222 13.2616
41 r177 186 187 90.9117
```

```
osc.pex.netlist ✘
C: > Users > USER > AppData > Roaming > MobaXterm > slash > RemoteFiles > 656172_2_6 > osc.pex.netlist
1 * File: osc.pex.netlist
2 * Created: Sat Aug 19 15:22:00 2023
3 * Program "Calibre xACT"
4 * Version "v2019.2_14.13"
5 *
6 .include "osc.pex.netlist.pex"
7 .subckt osc VSS VDD VIN ENABLE VOUT
8 *
9 * VOUT VOUT
10 * ENABLE ENABLE
11 * VIN VIN
12 * VDD VDD
13 * VSS VSS
14 M0 N_15_M0_d N_VIN_M0_g N_VSS_M0_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
15 M1 N_5_M1_d N_ENABLE_M1_g N_15_M1_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
16 M2 N_VSS_M2_d N_VOUT_M2_g N_VIN_M2_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
17 M3 N_7_M3_d N_5_M3_g N_VSS_M3_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
18 M4 N_VSS_M4_d N_8_M4_g N_VOUT_M4_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
19 M5 N_9_M5_d N_7_M5_g N_VSS_M5_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
20 M6 N_VSS_M6_d N_10_M6_g N_8_M6_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
21 M7 N_11_M7_d N_9_M7_g N_VSS_M7_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
22 M8 N_VSS_M8_d N_12_M8_g N_10_M8_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
23 M9 N_13_M9_d N_11_M9_g N_VSS_M9_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
24 M10 N_VSS_M10_d N_14_M10_g N_12_M10_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
25 M11 N_14_M11_d N_13_M11_g N_VSS_M11_s 75 NMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
26 M12 N_VDD_M12_d N_VIN_M12_g N_5_M12_s 76 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
27 M13 N_5_M13_d N_ENABLE_M13_g N_VDD_M13_s 76 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
28 M14 N_VDD_M14_d N_VOUT_M14_g N_VIN_M14_s 77 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
29 M15 N_7_M15_d N_5_M15_g N_VDD_M15_s 76 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
30 M16 N_VDD_M16_d N_8_M16_g N_VOUT_M16_s 77 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
31 M17 N_9_M17_d N_7_M17_g N_VDD_M17_s 76 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
32 M18 N_VDD_M18_d N_10_M18_g N_8_M18_s 77 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
33 M19 N_11_M19_d N_9_M19_g N_VDD_M19_s 76 PMOS_RVT L=2e-08 W=8.1e-08 NFIN=3
```

Lab07 通過條件

Check Rule Flow

1. Check DRC with no error
2. Check LVS with no error
3. Check PEX with no error

4. Measure the length of your layout design
(Remember to place the circuit become rectangle)

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附件補充 DRC Rule File M5-7 Offset Issue

Rule	Rule Type	Description	Operator	Values	Units	Notes
M4.AUX.1	Auxiliary	M4 horizontal edges must be at a grid of	==	24	nm	-
M4.AUX.2	Auxiliary	Minimum width M4 tracks must lie along the horizontal routing tracks. These tracks are located at a spacing equal to: $2N \times$ minimum metal width + offset from the origin, where $N \in \mathbb{Z}^+$.	-	-	-	1
M4.AUX.3	Auxiliary	M4 may not bend.	-	-	-	-
M4.AUX.4	Auxiliary	Outside edge of a wide M4 layer polygon may not touch a routing track edge.	-	-	-	-

Table 3.14.2 M4-M5 design rules (2 of 2; see Table 3.14.1).

NOTES

1. The metal grid offsets from X or Y axis are specified through the use of environmental variables defined in the `set_pdk_path.csh` or `.cshrc`. The default offset value is 0 nm. To offset a particular grid by p nm, specify the variable value as $p*10$. Thus, for an offset of 24 nm, the corresponding variable value is 240.

Note that currently, the rules only allow offset value for M4-M5 to be an integer multiple of 12 nm.



```
824 VARIABLE VAR_M4_YOFFSET 0 /*ENVIRONMENT*/
825 VARIABLE VAR_M4_1X_DBU 240
826 M4_OFFGRID = OFFGRID M4 1 VAR_M4_1X_DBU OFFSET 0 VAR_M4_YOFFSET
827 M4_OFFGRIDR = DFM COPY M4_OFFGRID REGION
828 VARIABLE VAR_M4_1X (VAR_M4_1X_DBU/10000)
829 VARIABLE VAR_M4_1X_DECOMP_GRID (2*(1+1)*VAR_M4_1X_DBU)
830 VARIABLE VAR_M4_1X_OFFSET_GRIDA (1*(VAR_M4_1X_DBU/2))
831 VARIABLE VAR_M4_1X_OFFSET_GRIDB (((1.5*1)+1)*VAR_M4_1X_DBU)
832 VARIABLE VAR_M4_1X_OFFSET_GRIDA_TOT (VAR_M4_1X_OFFSET_GRIDA + VAR_M4_YOFFSET)
833 VARIABLE VAR_M4_1X_OFFSET_GRIDB_TOT (VAR_M4_1X_OFFSET_GRIDB + VAR_M4_YOFFSET)
```

附件補充 更換Technology Library

