

# FPGA Introduce

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# Outline

- ❖ EGO1
- ❖ 元件及腳位對應
- ❖ Vivado 2018.2

# Outline

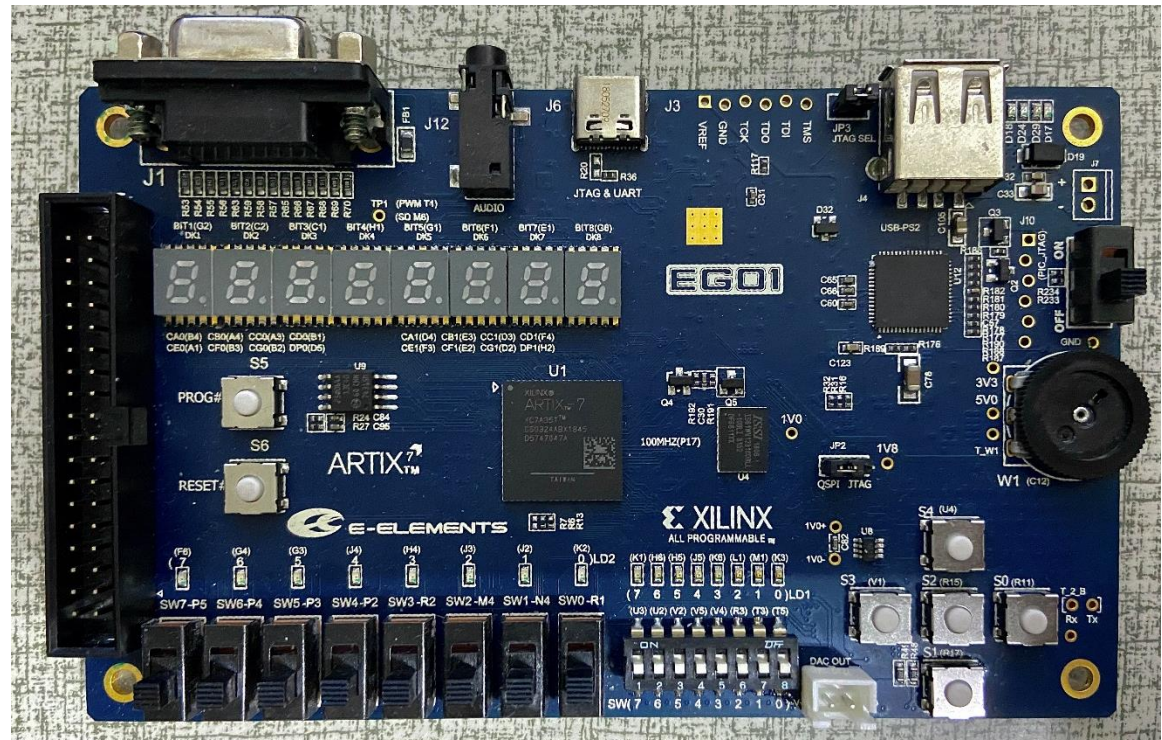
- ❖ EGO1
- ❖ 元件及腳位對應
- ❖ Vivado 2018.2

# EGO1

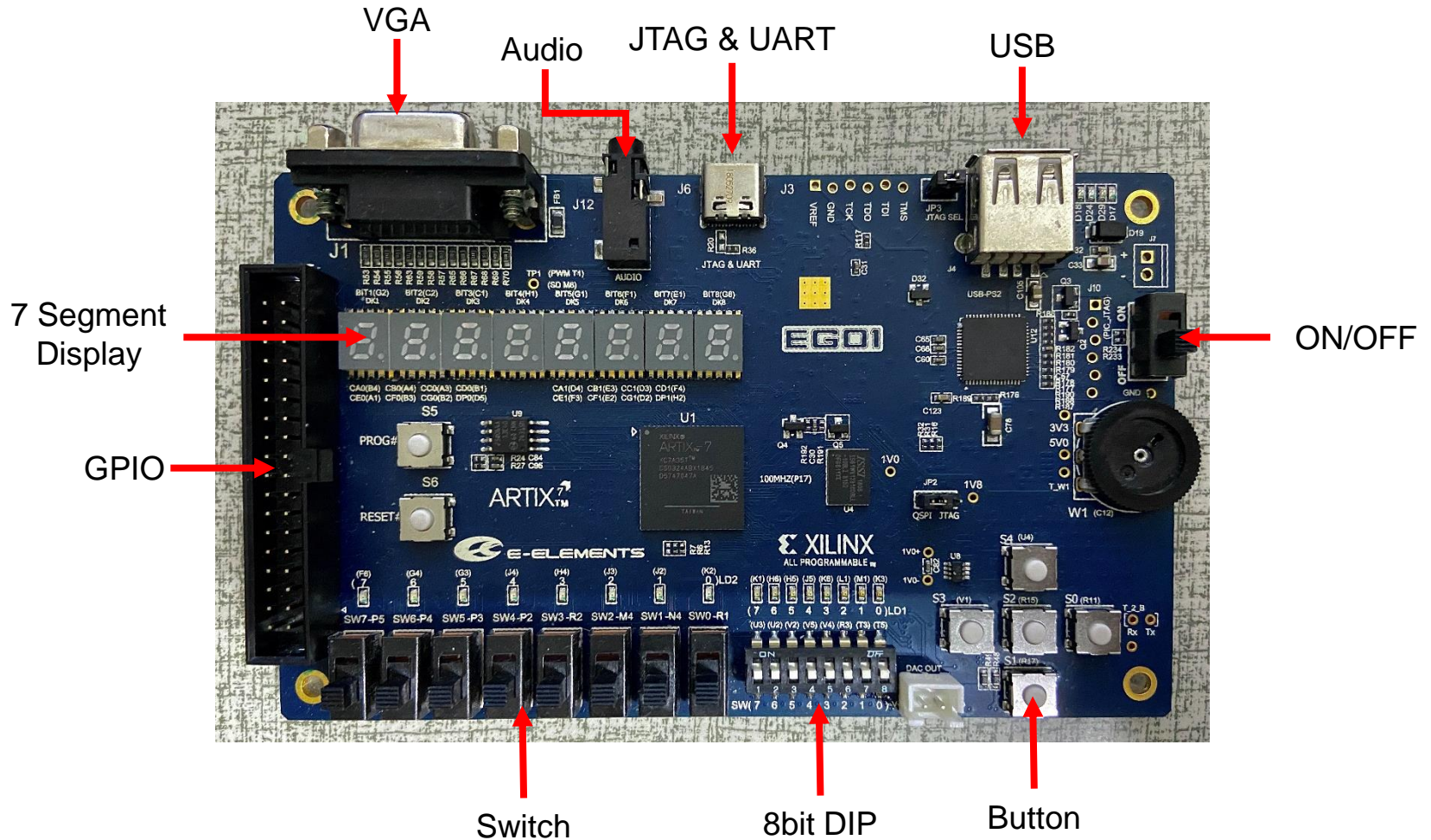


國立中興大學  
National Chung Hsing University

- ❖ EGO1是依元素科技基於 Xilinx Artix-7 FPGA研發的可攜式數模混和基礎教學平台。EGO-XA7配備的FPGA具有大容量高性能等特點，能實現較複雜的數位邏輯設計。



# EGO1





# EGO1



## EGO1 User Manual

	Part Number	XC7A12T	XC7A15T	XC7A25T	XC7A35T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280
	Slices	2,000	2,600	3,650	5,200
	CLB Flip-Flops	16,000	20,800	29,200	41,600
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50
	Total Block RAM (Kb)	720	900	1,620	1,800
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5
I/O Resources	Maximum Single-Ended I/O	150	250	150	250
	Maximum Differential I/O Pairs	72	120	72	120
Embedded Hard IP Resources	DSP Slices	40	45	80	90
	PCIe® Gen2 <sup>(1)</sup>	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate) <sup>(2)</sup>	2	4	4	4
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L

# Outline

- ❖ EGO1
- ❖ 元件及腳位對應
- ❖ Vivado 2018.2

# 元件及腳位對應

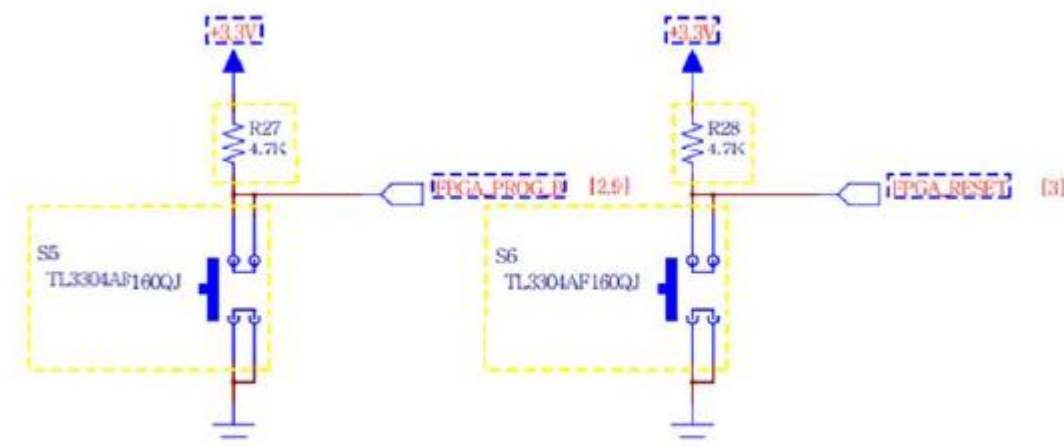
- ❖ EGO-XA7 搭載一個100MHz的時鐘晶片，輸出的時鐘訊號直接與FPGA全域時鐘輸入接腳(P17)相連。

名稱	電路圖訊號	FPGA IO PIN
時鐘接腳	SYS_CLK	P17



# 元件及腳位對應

- ❖ 專用按鍵
- ❖ PROG：擦除FPGA配置
- ❖ RESET：邏輯重置

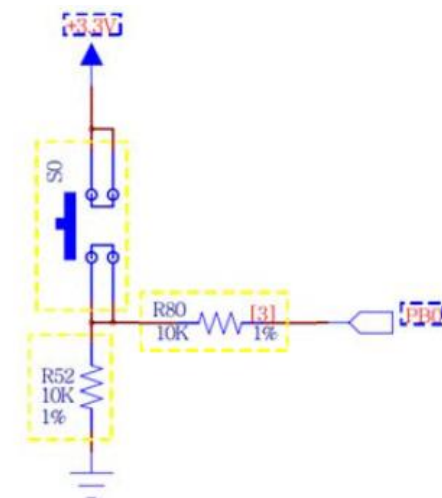


名稱	電路圖訊號	FPGA IO PIN
重置接腳	FPGA_RESET	P15

# 元件及腳位對應

- ❖ 通用按鍵(S0 ~ S4)
- ❖ 預設為低電位，按鍵按下時輸出高電位

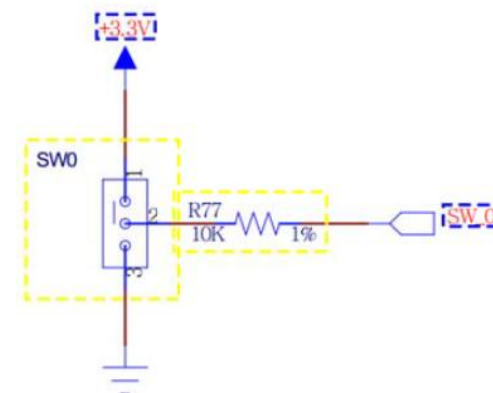
名稱	電路圖訊號	FPGA IO PIN
S0	PB0	R11
S1	PB1	R17
S2	PB2	R15
S3	PB3	V1
S4	PB4	U4



# 元件及腳位對應

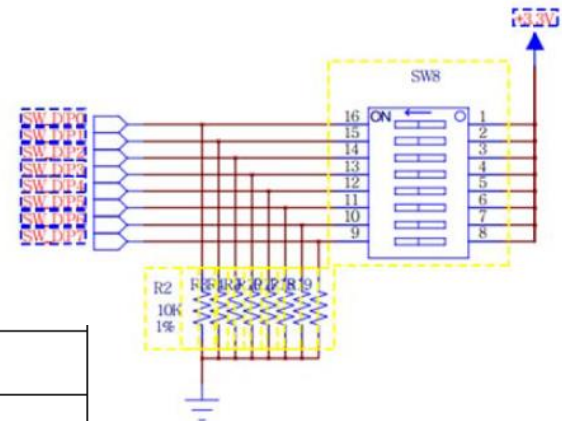
- ❖ 開關(Switch)
- ❖ 預設為低電位，**向上撥動**輸出**高電位**

名稱	電路圖訊號	FPGA IO PIN
SW0	SW_0	P5
SW1	SW_1	P4
SW2	SW_2	P3
SW3	SW_3	P2
SW4	SW_4	R2
SW5	SW_5	M4
SW6	SW_6	N4
SW7	SW_7	R1



# 元件及腳位對應

- ❖ 8bit 指撥開關(DIP Switch)
- ❖ 預設為低電位，**向上撥動**輸出**高電位**



SW8	SW_DIP0	U3
	SW_DIP1	U2
	SW_DIP2	V2
	SW_DIP3	V5
	SW_DIP4	V4
	SW_DIP5	R3
	SW_DIP6	T3
	SW_DIP7	T5

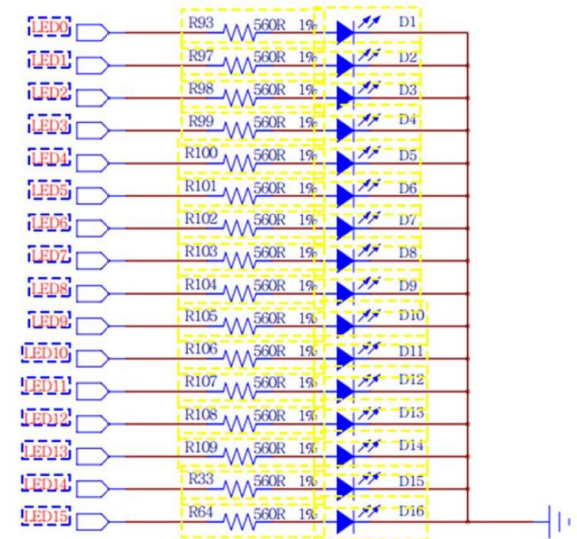


# 元件及腳位對應

- ❖ LED燈
- ❖ 輸出高電位時被點亮

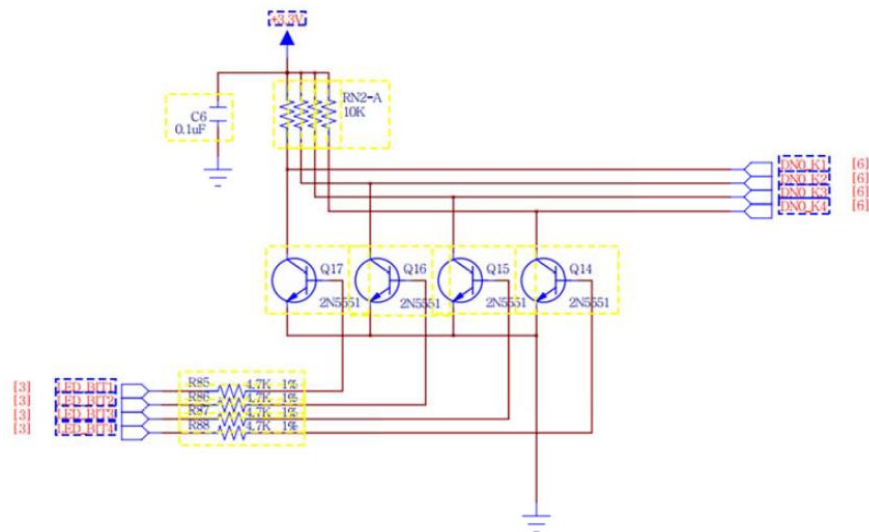
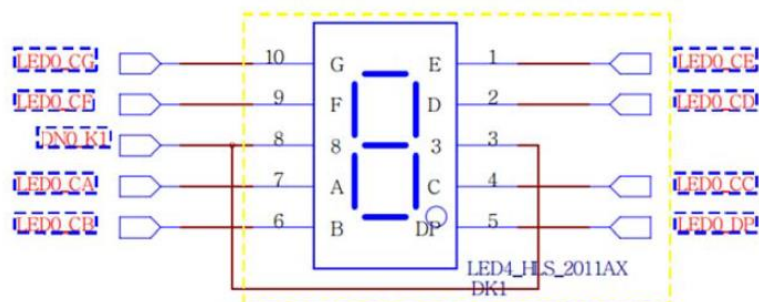
名稱	電路圖訊號	FPGA IO PIN	顏色
D0	LED0	F6	Green
D1	LED1	G4	Green
D2	LED2	G3	Green
D3	LED3	J4	Green
D4	LED4	H4	Green

D5	LED5	J3	Green
D6	LED6	J2	Green
D7	LED7	K2	Green
D8	LED8	K1	Green
D9	LED9	H6	Green
D10	LED10	H5	Green
D11	LED11	J5	Green
D12	LED12	K6	Green
D13	LED13	L1	Green
D14	LED14	M1	Green
D15	LED15	K3	Green



# 元件及腳位對應

- ❖ 七段顯示器(7 Segment Display)
- ❖ 顯示器為**共陰極**顯示器，即公共極輸入低電位。
- ❖ 操控多顯示器需**片選信號**及**段選信號**。片選信號及段選信號須皆為**高電位**，顯示器上對應位置才可以被點亮。





# 元件及腳位對應

## ❖ 七段顯示器(7 Segment Display)

段選信號

名稱	電路圖訊號	FPGA IO PIN
A0	LED0_CA	B4
B0	LED0_CB	A4
C0	LED0_CC	A3
D0	LED0_CD	B1
E0	LED0_CE	A1
F0	LED0_CF	B3
G0	LED0_CG	B2
DP0	LED0_DP	D5
A1	LED1_CA	D4
B1	LED1_CB	E3
C1	LED1_CC	D3
D1	LED1_CD	F4
E1	LED1_CE	F3
F1	LED1_CF	E2
G1	LED1_CG	D2
DP1	LED1_DP	H2

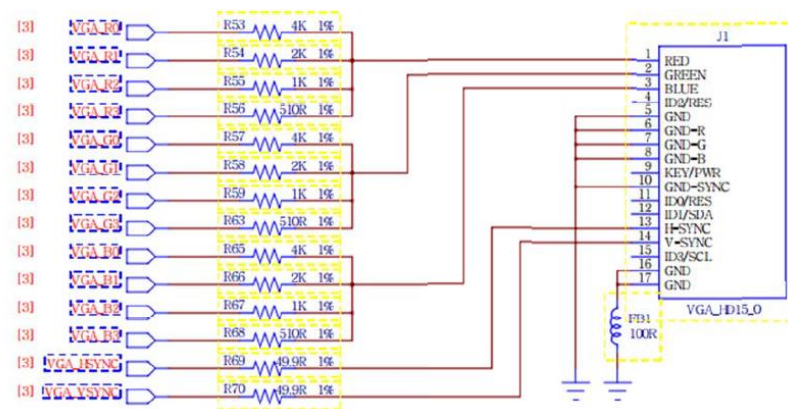
片選信號

DN0_K1	LED_BIT1	G2
DN0_K2	LED_BIT2	C2
DN0_K3	LED_BIT3	C1
DN0_K4	LED_BIT4	H1
DN1_K1	LED_BIT5	G1
DN1_K2	LED_BIT6	F1
DN1_K3	LED_BIT7	E1
DN1_K4	LED_BIT8	G6

# 元件及腳位對應

- ❖ VGA介面
- ❖ EGO-XA7上的VGA介面通過14位元信號線與FPGA連接，紅、綠、藍三個顏色信號各占4位，另外還包括水平同步和垂直同步信號。

名稱	電路圖訊號	FPGA IO PIN
RED	VGA_R0	F5
	VGA_R1	C6
	VGA_R2	C5
	VGA_R3	B7
GREEN	VGA_G0	B6
	VGA_G1	A6
	VGA_G2	A5
	VGA_G3	D8
BLUE	VGA_B0	C7
	VGA_B1	E6
	VGA_B2	E5
	VGA_B3	E7
H-SYNC	VGA_HSYNC	D7
V-SYNC	VGA_VSYNC	C4



# 元件及腳位對應

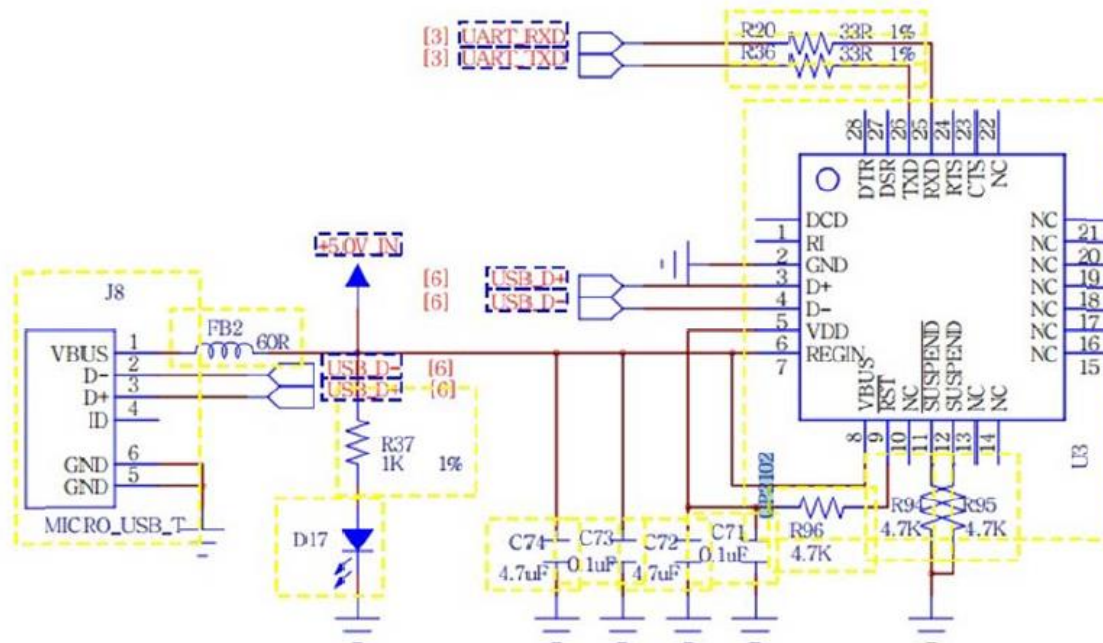
## ❖ UART

- ❖ 全稱為通用非同步收發器，是實現設備之間低速資料通信的標準協議。“**非同步**”指不需要額外的時鐘線進行資料的同步傳輸，雙方約定在**同一個頻率**下收發資料，此介面只需要兩條信號線(RXD、TXD)就可以完成資料的相互通信，接收盒發送可以同時進行，也就是全雙工。
- ❖ 收發的過程，在發送器閒置時間，資料線處於邏輯1狀態，當有資料要傳輸時，首先使資料線狀態為**0**，之後是**8個資料位元**、一位元**校驗位**、一位元**停止位**，停止位用於標示一幀的結束，接收過程亦類似。



# 元件及腳位對應

## ❖ UART

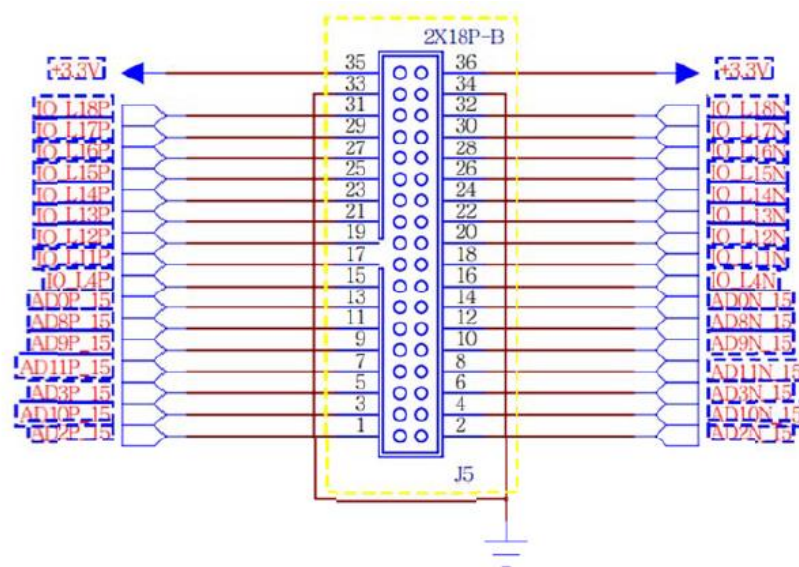


CP2102 標號	電路圖訊號	FPGA IO PIN
25	UART_RX	T4 (FPGA 串列埠發送)
26	UART_TX	N5 (FPGA 串列埠接收)

# 元件及腳位對應

## ❖ GPIO (32雙向I/O)

2x18 標號	電路圖訊號	FPGA IO PIN
1	AD2P_15	B16
2	AD2N_15	A15
3	AD10P_15	A13
4	AD10N_15	B18
5	AD3P_15	F13
6	AD3N_15	B13
7	AD11P_15	D14
8	AD11N_15	B11
9	AD9P_15	E15
10	AD9N_15	D15
11	AD8P_15	H16
12	AD8N_15	F15
13	AD0P_15	H14
14	AD0N_15	E17
15	IO_L4P	K13
16	IO_L4N	H17
17	IO_L11P	B17
18	IO_L11N	A16
19	IO_L12P	A14
20	IO_L12N	A18
21	IO_L13P	F14
22	IO_L13N	B14
23	IO_L14P	C14
24	IO_L14N	A11
25	IO_L15P	E16
26	IO_L15N	C15
27	IO_L16P	G16



28	IO_L16N	F16
29	IO_L17P	G14
30	IO_L17N	D17
31	IO_L18P	J13
32	IO_L18N	G17

# Outline

- ❖ EGO1
- ❖ 元件及腳位對應
- ❖ Vivado 2018.2



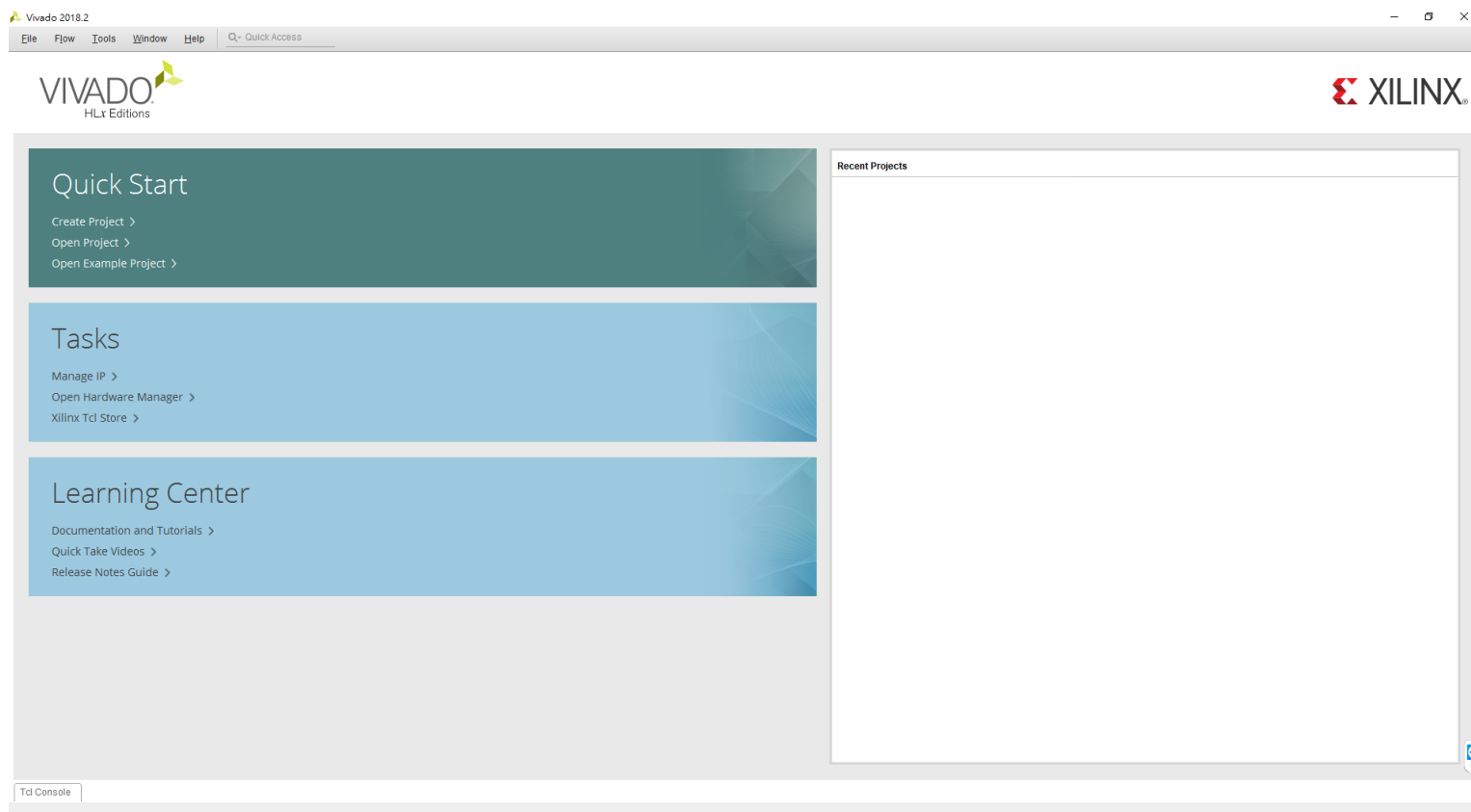
# Vivado 2018.2

- ❖ 專案不能有中文路徑、不能以數字開頭
- ❖ 程式碼加入註解 ( /\*...\*/ or //... )
- ❖ 在D槽以自己的學號創建新資料夾，之後全部上課資料都放裡面，避免公共電腦過於混亂

**不要Copy同學的程式碼**  
**!!!**

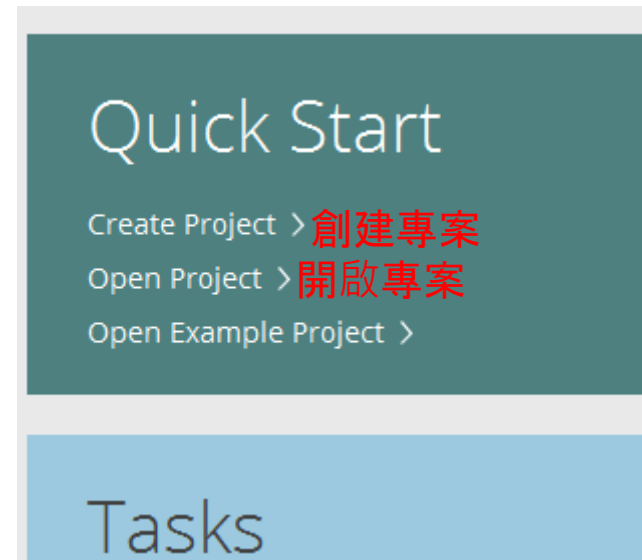
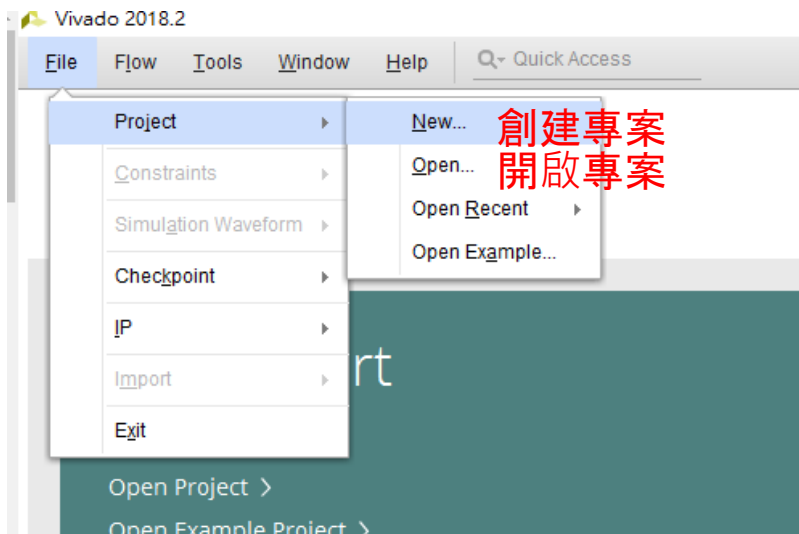
# Vivado 2018.2

## ❖ 開啟 Vivado 2018.2



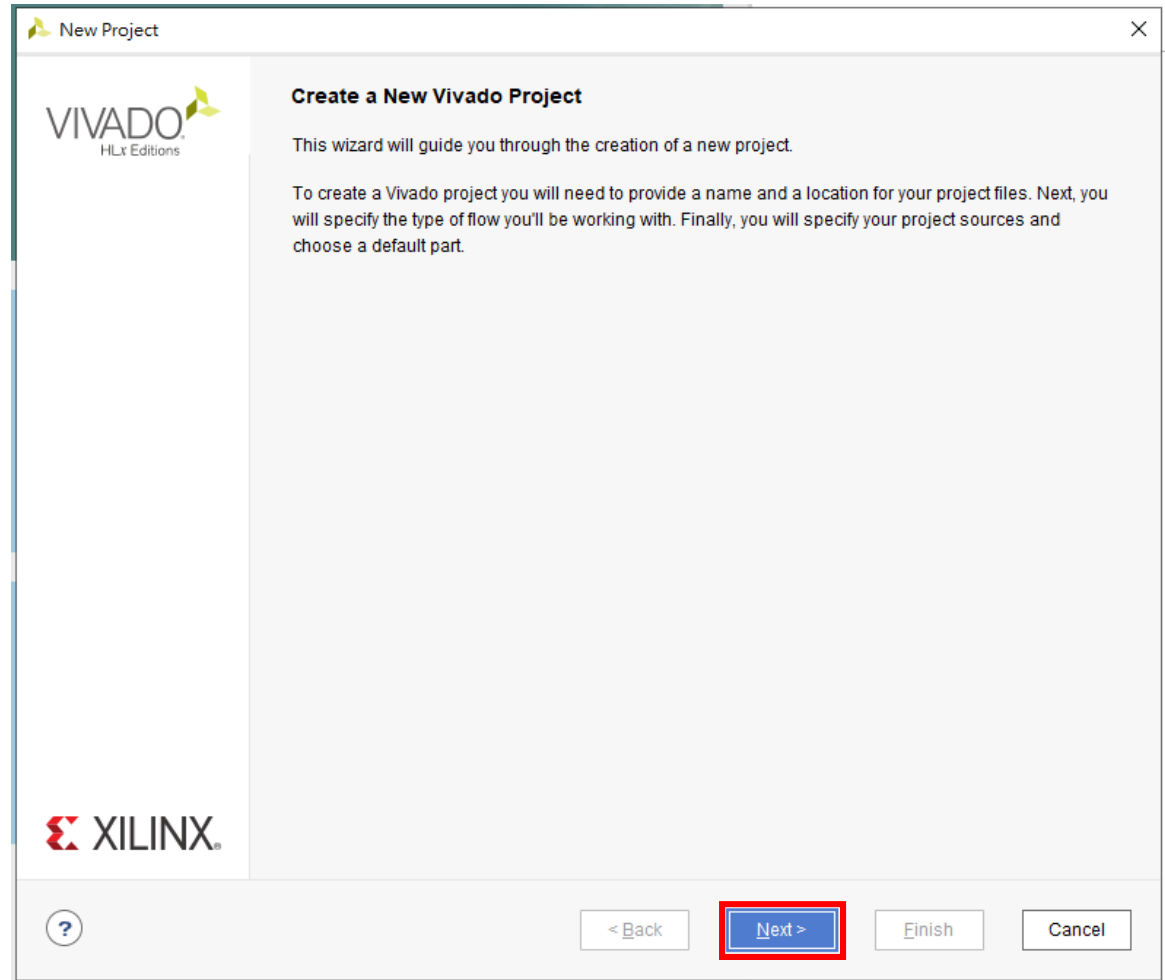
# Vivado 2018.2

## ❖ 創建專案 / 開啟專案



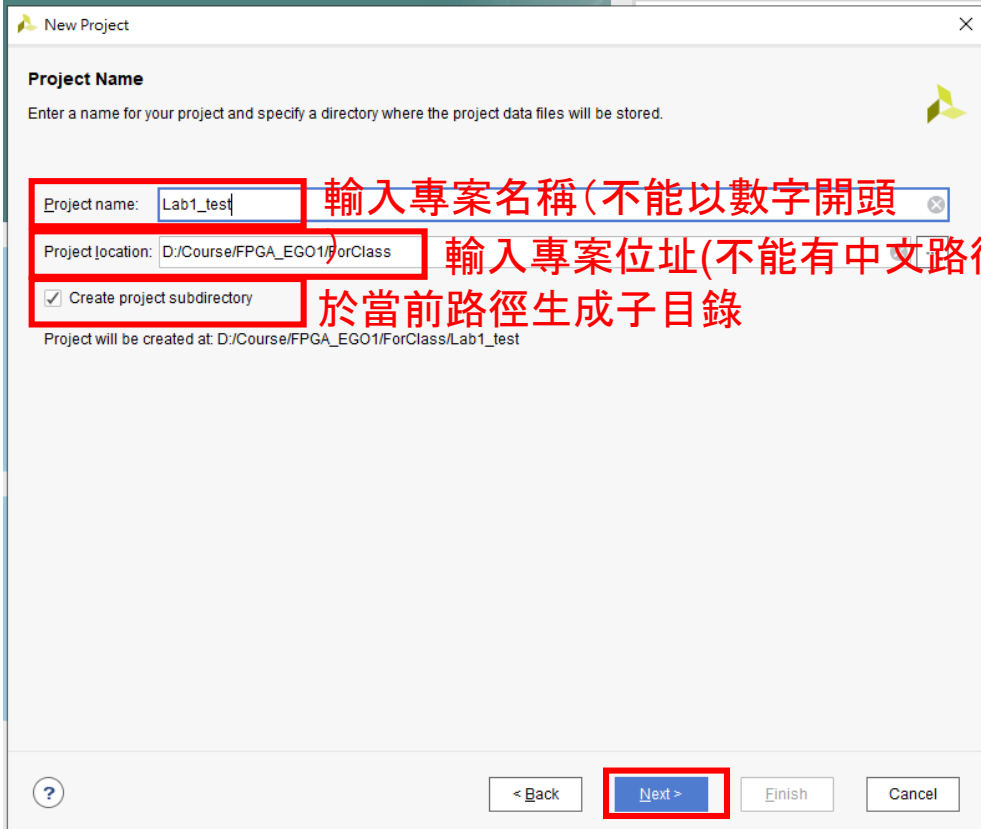
# Vivado 2018.2

- ❖ 創新專案
- ❖ 無意義開場白
- ❖ 直接“Next”



# Vivado 2018.2

- ❖ 輸入專案名稱
- ❖ 輸入專案位址
- ❖ “Next”



The image shows the 'New Project' dialog box in Vivado 2018.2. The dialog has a title bar 'New Project' and a close button. Below the title bar, it says 'Project Name' and 'Enter a name for your project and specify a directory where the project data files will be stored.' There are three input fields: 'Project name:' with the text 'Lab1\_test', 'Project location:' with the text 'D:/Course/FPGA\_EGO1/ForClass', and a checkbox 'Create project subdirectory' which is checked. Below these fields, it says 'Project will be created at: D:/Course/FPGA\_EGO1/ForClass/Lab1\_test'. At the bottom, there are four buttons: '< Back', 'Next >', 'Finish', and 'Cancel'. The 'Next >' button is highlighted with a red box. Red annotations in Chinese are present: '輸入專案名稱(不能以數字開頭)' points to the 'Project name' field, '輸入專案位址(不能有中文路徑)' points to the 'Project location' field, and '於當前路徑生成子目錄' points to the 'Create project subdirectory' checkbox.

Project Name  
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: Lab1\_test 輸入專案名稱(不能以數字開頭)

Project location: D:/Course/FPGA\_EGO1/ForClass 輸入專案位址(不能有中文路徑)

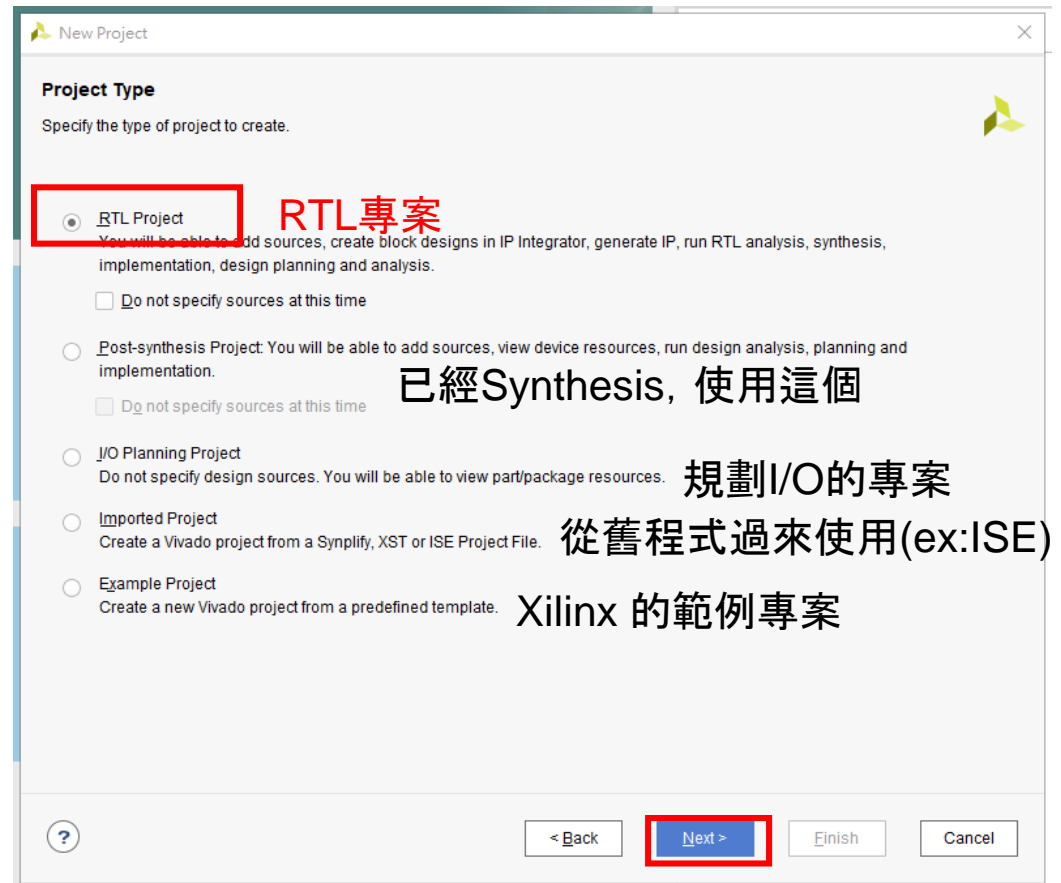
☒ Create project subdirectory 於當前路徑生成子目錄

Project will be created at: D:/Course/FPGA\_EGO1/ForClass/Lab1\_test

< Back Next > Finish Cancel

# Vivado 2018.2

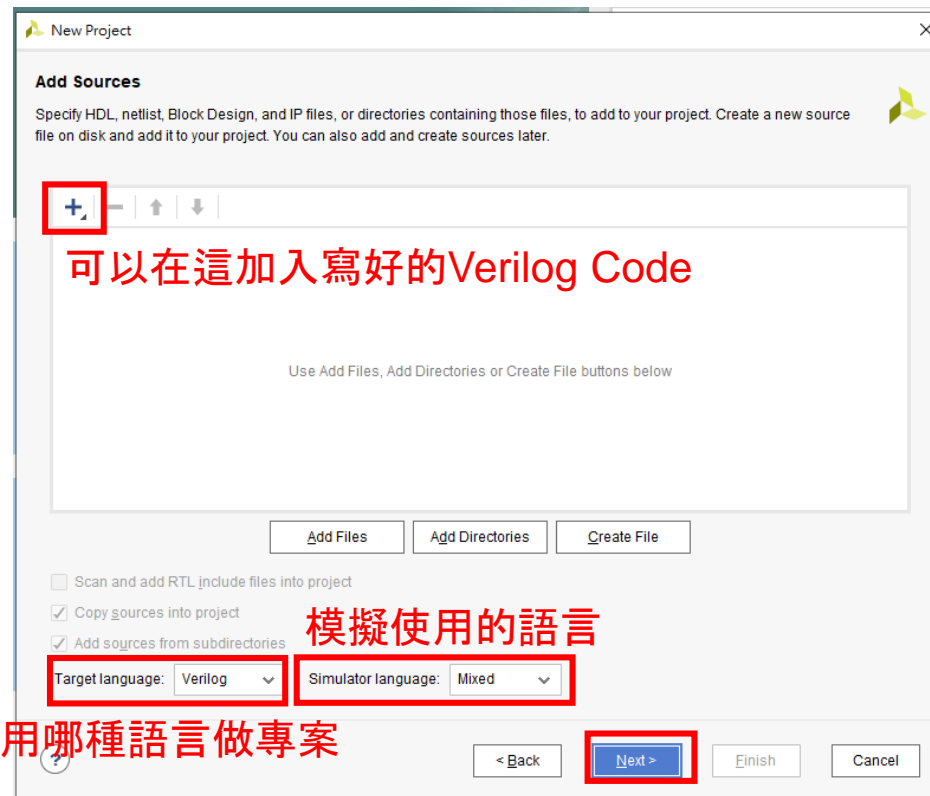
- ❖ 選 "RTL Project"
- ❖ "Next"





# Vivado 2018.2

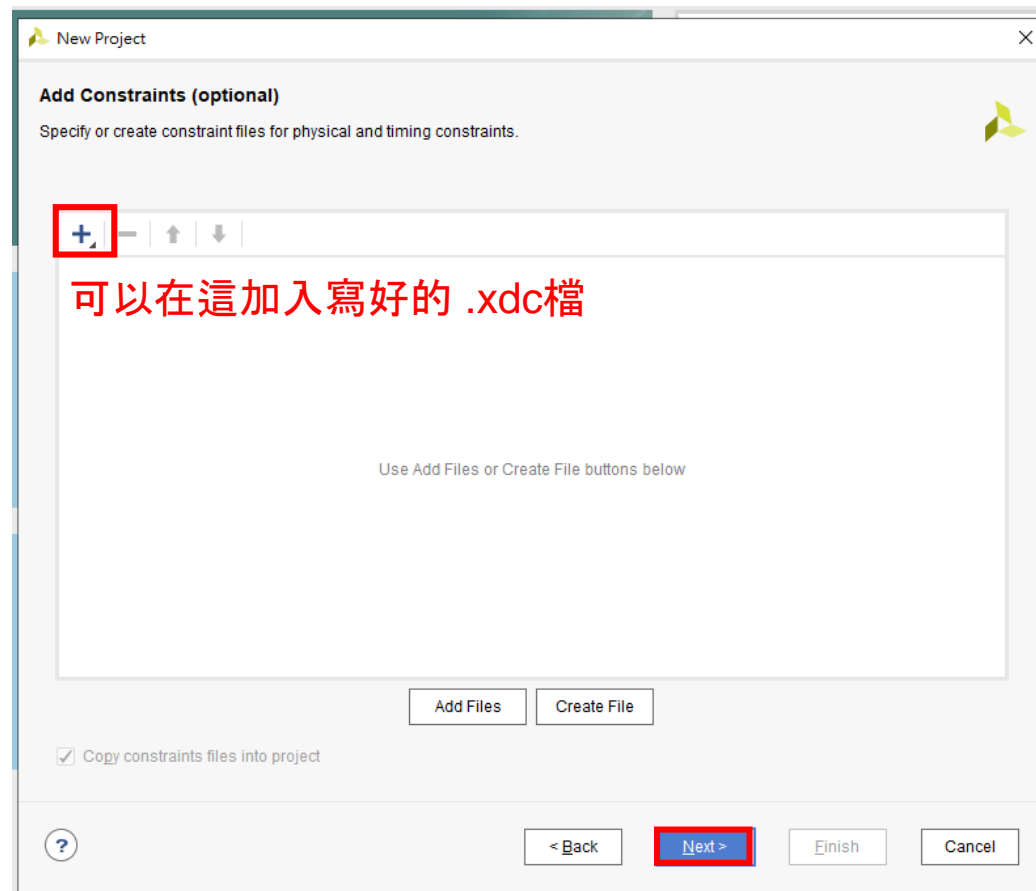
- ❖ 加入Design Source
- ❖ Target language 選 Verilog ， Simulation 選 Mixed
- ❖ “Next”



# Vivado 2018.2

❖ 加入Constraints (.xdc檔)

❖ “Next”



# Vivado 2018.2

- ❖ 選擇對應的板子
- ❖ Family: Artix-7
- ❖ Package: csg324
- ❖ Speed: -1
- ❖ Part: xc7a35tcsg324-1
- ❖ “Next”

New Project

**Default Part** 選擇對應的FPGA板型號

Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

[Reset All Filters](#)

Category: All Package: csg324 Temperature: All Remaining

Family: Artix-7 Speed: -1

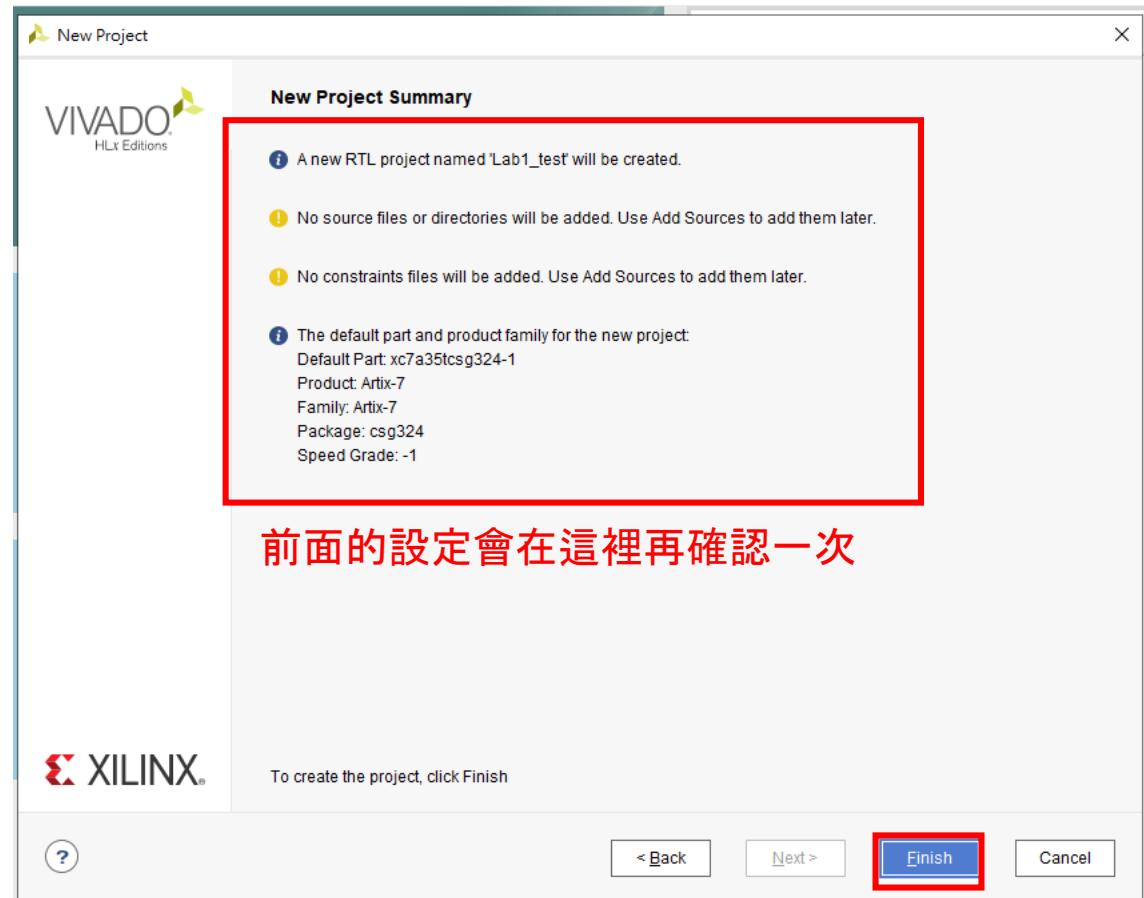
Search: Q

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Transceiv
xc7a15tcsg324-1	324	210	10400	20800	25	0	45	0
xc7a35tcsg324-1	324	210	20800	41600	50	0	90	0
xc7a50tcsg324-1	324	210	32000	64000	75	0	120	0
xc7a75tcsg324-1	324	210	47200	94400	105	0	180	0
xc7a100tcsg324-1	324	210	63400	126800	135	0	240	0

< Back Next > Finish Cancel

# Vivado 2018.2

- ❖ 進行最後的確認
- ❖ “Finish”



# Vivado 2018.2

## 專案操作介面

Lab1\_test - [D:/Course/FPGA\_EGO1/ForClass/Lab1\_test/Lab1\_test.xpr] - Vivado 2018.2

File Edit Flow Tools Repgrts Window Layout View Help Quick Access

Flow Navigator PROJECT MANAGER - Lab1\_test

**PROJECT MANAGER**

- Settings
- Add Sources
- Language Templates
- IP Catalog

**IP INTEGRATOR**

- Create Block Design
- Open Block Design
- Generate Block Design

**SIMULATION**

- Run Simulation

**RTL ANALYSIS**

- Open Elaborated Design

**SYNTHESIS**

- Run Synthesis
- Open Synthesized Design

**IMPLEMENTATION**

- Run Implementation
- Open Implemented Design

**PROGRAM AND DEBUG**

- Generate Bitstream
- Open Hardware Manager

**Sources**

- Design Sources
  - Constraints
- Simulation Sources
  - sim\_1

**Project Summary**

Settings Edit

Project name: Lab1\_test  
Project location: D:/Course/FPGA\_EGO1/ForClass/Lab1\_test  
Product family: Artix-7  
Project part: xc7a35tcsq324-1  
Top module name: Not defined  
Target language: Verilog  
Simulator language: Mixed

**Synthesis**

Status: Not started  
Messages: No errors or warnings  
Part: xc7a35tcsq324-1  
Strategy: Vivado Synthesis Defaults  
Report Strategy: Vivado Synthesis Default Reports

**Implementation**

Status: Not started  
Messages: No errors or warnings  
Part: xc7a35tcsq324-1  
Strategy: Vivado Implementation Defaults  
Report Strategy: Vivado Implementation Default Reports  
Incremental compile: None

**DRC Violations**

Run Implementation to see DRC results

**Timing**

Run Implementation to see timing results

**Properties**

Select an object to see properties

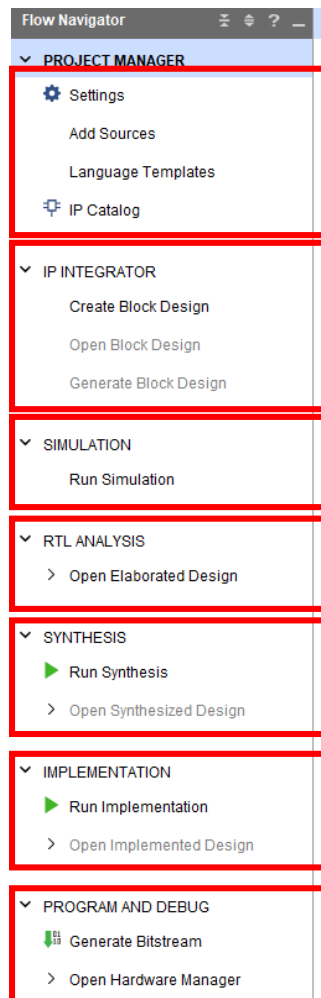
**Tcl Console** Messages Log Reports **Design Runs**

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2018)	Vivado Synthesis Default Reports (Vivado Synthesis 2018)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2018)	Vivado Implementation Default Reports (Vivado Implementation 2018)

設計理念，由上到下

# Vivado 2018.2

## ❖ 操作介面介紹



專案設定  
新增資料(Verilog, Constraint)  
資源範例  
IP庫

使用圖形化介面創建專案

模擬 (驗證RTL邏輯是否正確)

RTL分析 (轉成Gate分析)

合成 (將RTL轉成Gate Level, 並且設定腳位資訊)

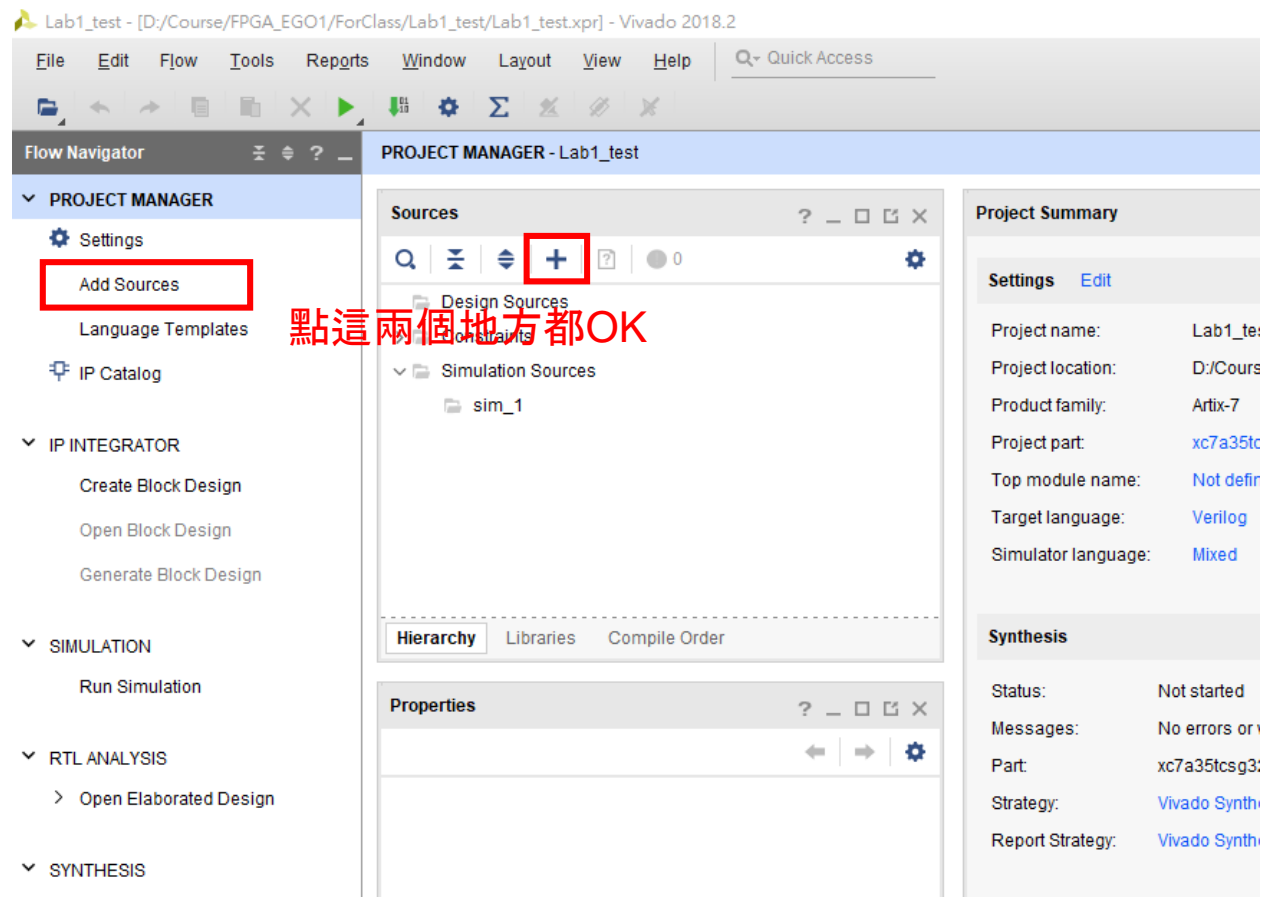
實現 (將合成的結果 映射到FPGA板)

將實現的結果轉成板子看得懂的檔案(bitstream檔, .bit檔)  
再將bitstream燒錄至FPGA板



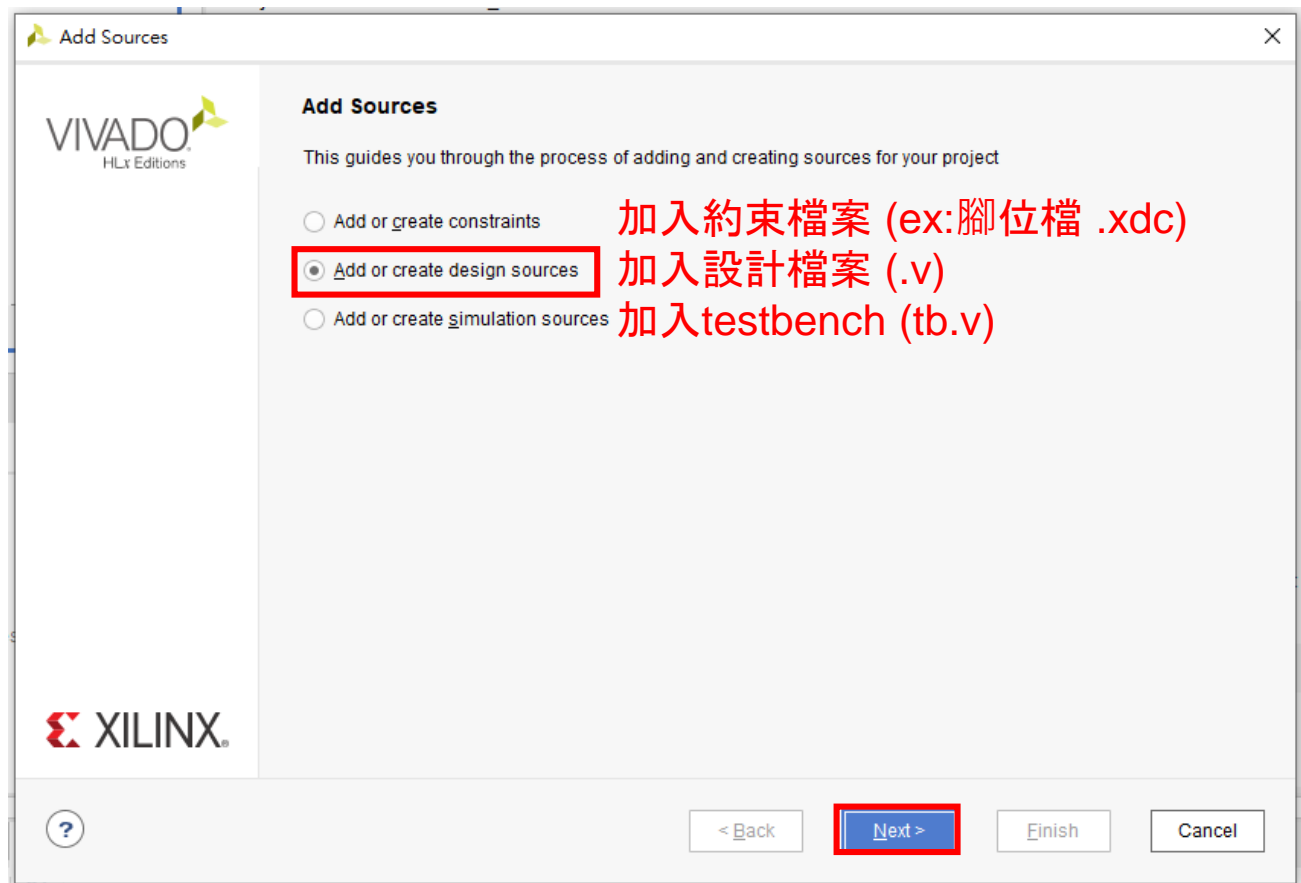
# Vivado 2018.2

## ❖ 加入Design Source (Verilog code)



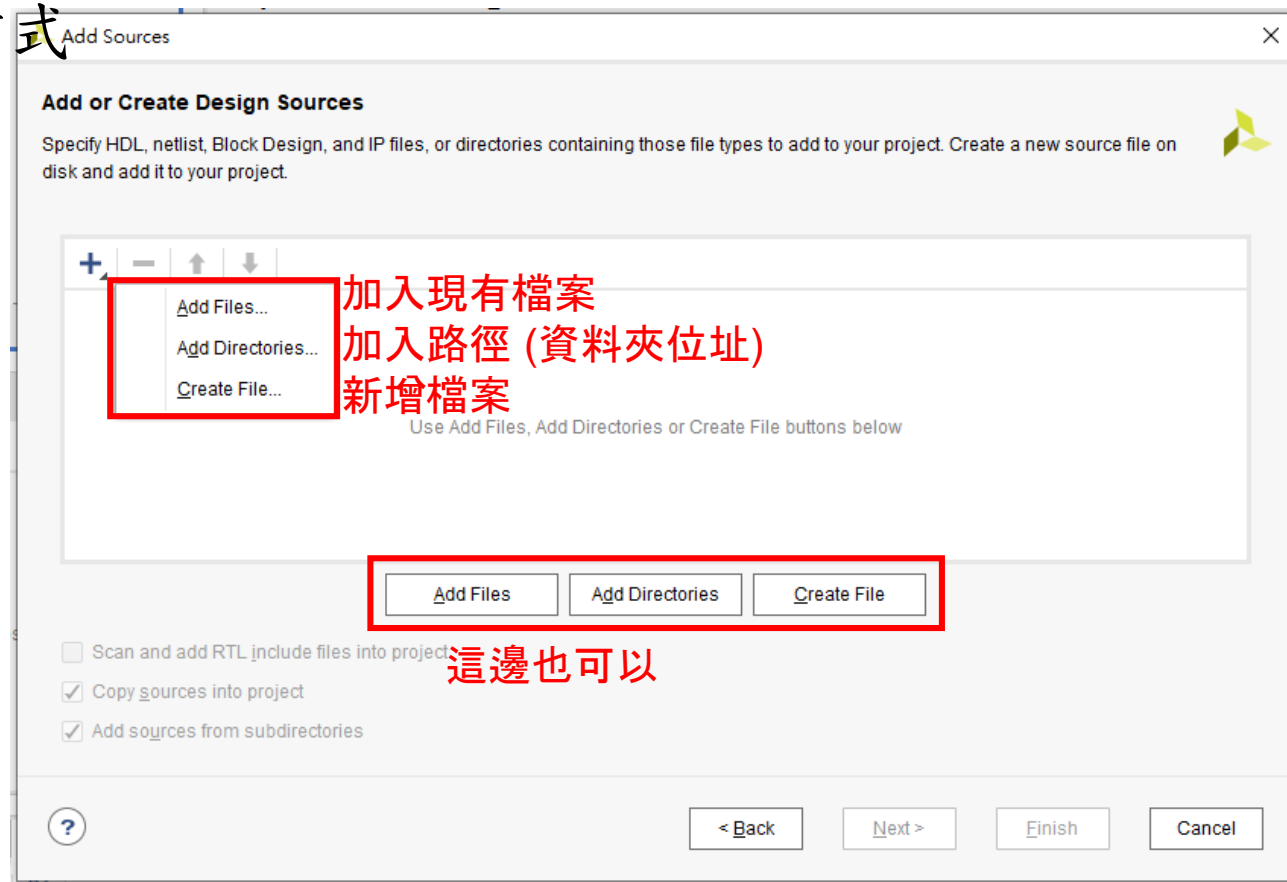
# Vivado 2018.2

- ❖ 加入Design Source (Verilog code)
- ❖ “design source”
- ❖ “Next”



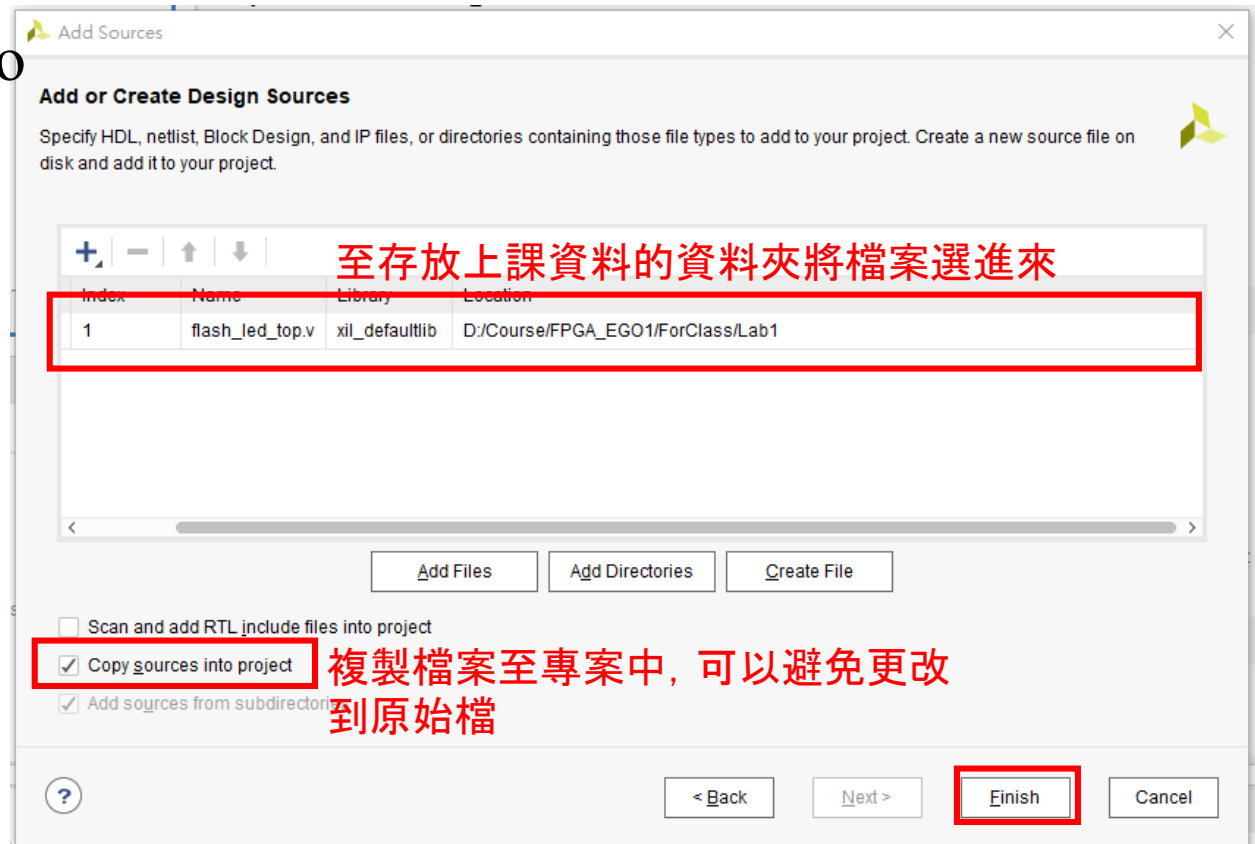
# Vivado 2018.2

- ❖ 加入Design Source (Verilog code)
- ❖ 選擇加入資料方式
- ❖ “Add Files”



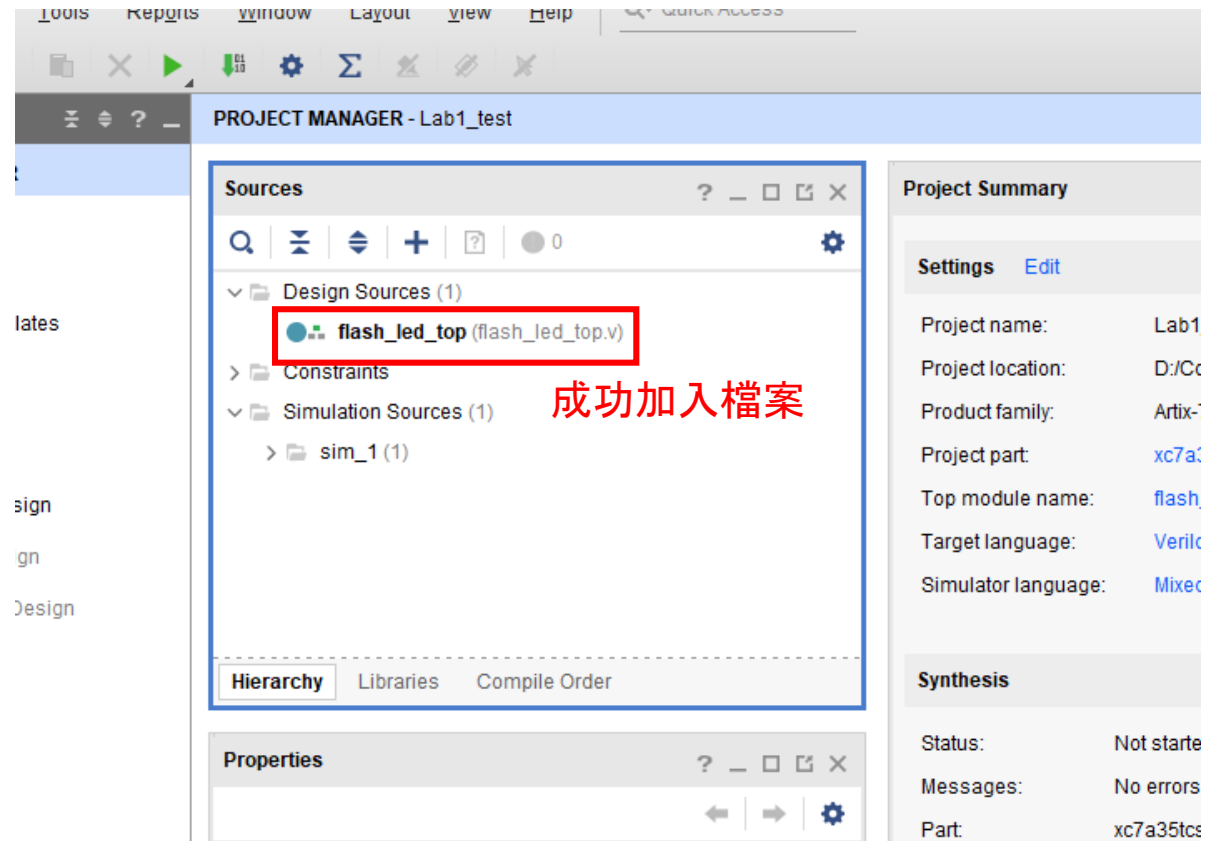
# Vivado 2018.2

- ❖ 加入Design Source (Verilog code)
- ❖ 載入上課範例檔案
- ❖ “Copy source into project” 打勾
- ❖ “Finish”



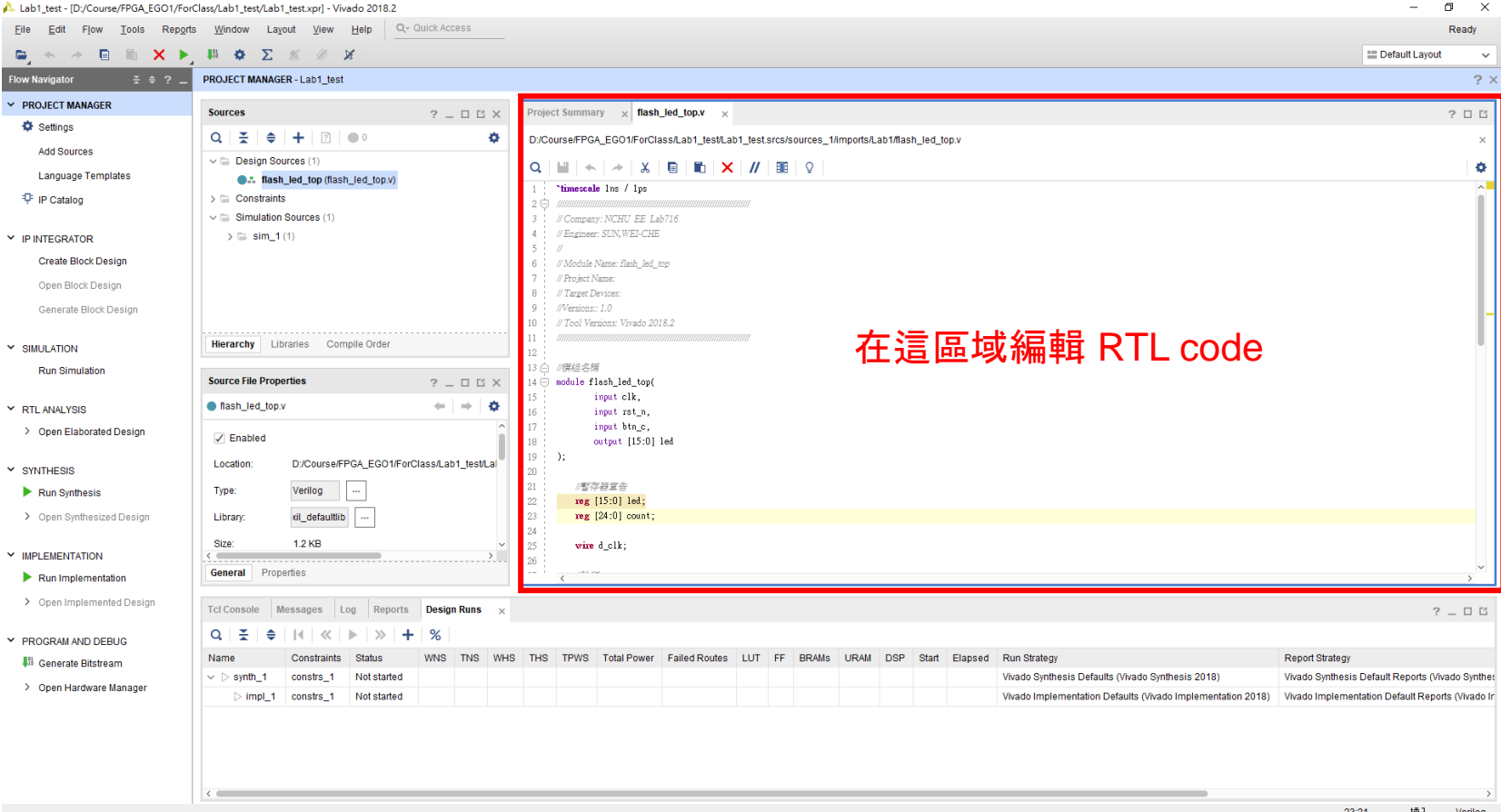
# Vivado 2018.2

- ❖ 確定Verilog code 成功加入
- ❖ 連擊檔案開啟編輯



# Vivado 2018.2

❖ 編輯RTL檔，必須沒有紅色底線(若有則代表有錯誤)



Project Summary | flash\_led\_top.v

D:/Course/FPGA\_EGO1/ForClass/Lab1\_test/Lab1\_test/srcs/sources\_1/imports/Lab1/flash\_led\_top.v

```
1 timescale 1ns / 1ps
2
3 // Company: NCHU EE Lab716
4 // Engineer: SUN,WEI-CHE
5 //
6 // Module Name: flash_led_top
7 // Project Name:
8 // Target Devices:
9 // Versions: 1.0
10 // Tool Versions: Vivado 2018.2
11
12
13 //模組名稱
14 module flash_led_top(
15     input clk,
16     input rst_n,
17     input btn_c,
18     output [15:0] led
19 );
20
21 //暫存器宣告
22 reg [15:0] led;
23 reg [24:0] count;
24
25 wire d_clk;
26
```

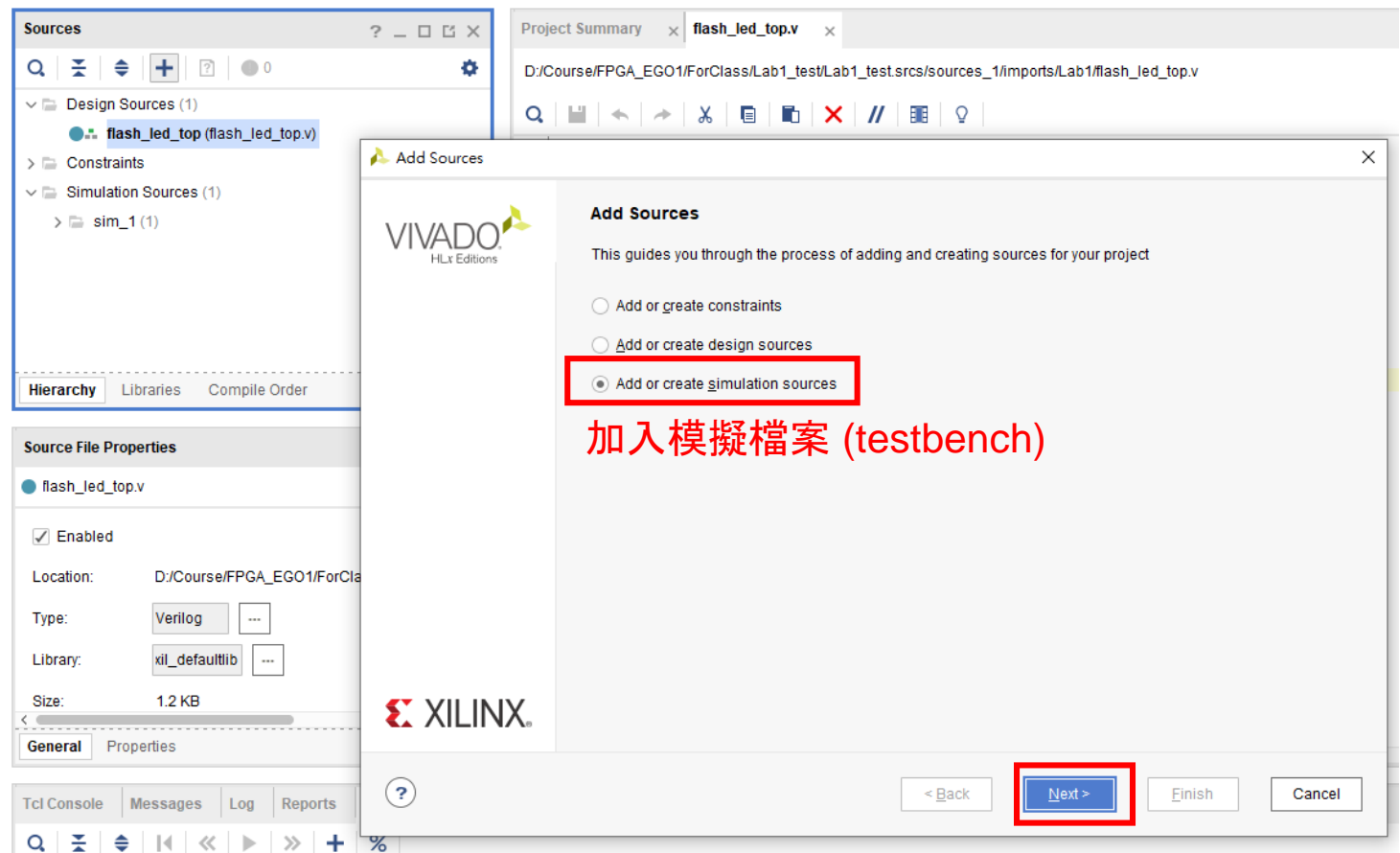
在這區域編輯 RTL code

Name	Constraints	Status	WNS	TNS	WHS	THS	TPWS	Total Power	Failed Routes	LUT	FF	BRAMs	URAM	DSP	Start	Elapsed	Run Strategy	Report Strategy
synth_1	constrs_1	Not started															Vivado Synthesis Defaults (Vivado Synthesis 2018)	Vivado Synthesis Default Reports (Vivado Synthesis 2018)
impl_1	constrs_1	Not started															Vivado Implementation Defaults (Vivado Implementation 2018)	Vivado Implementation Default Reports (Vivado Implementation 2018)

# Vivado 2018.2

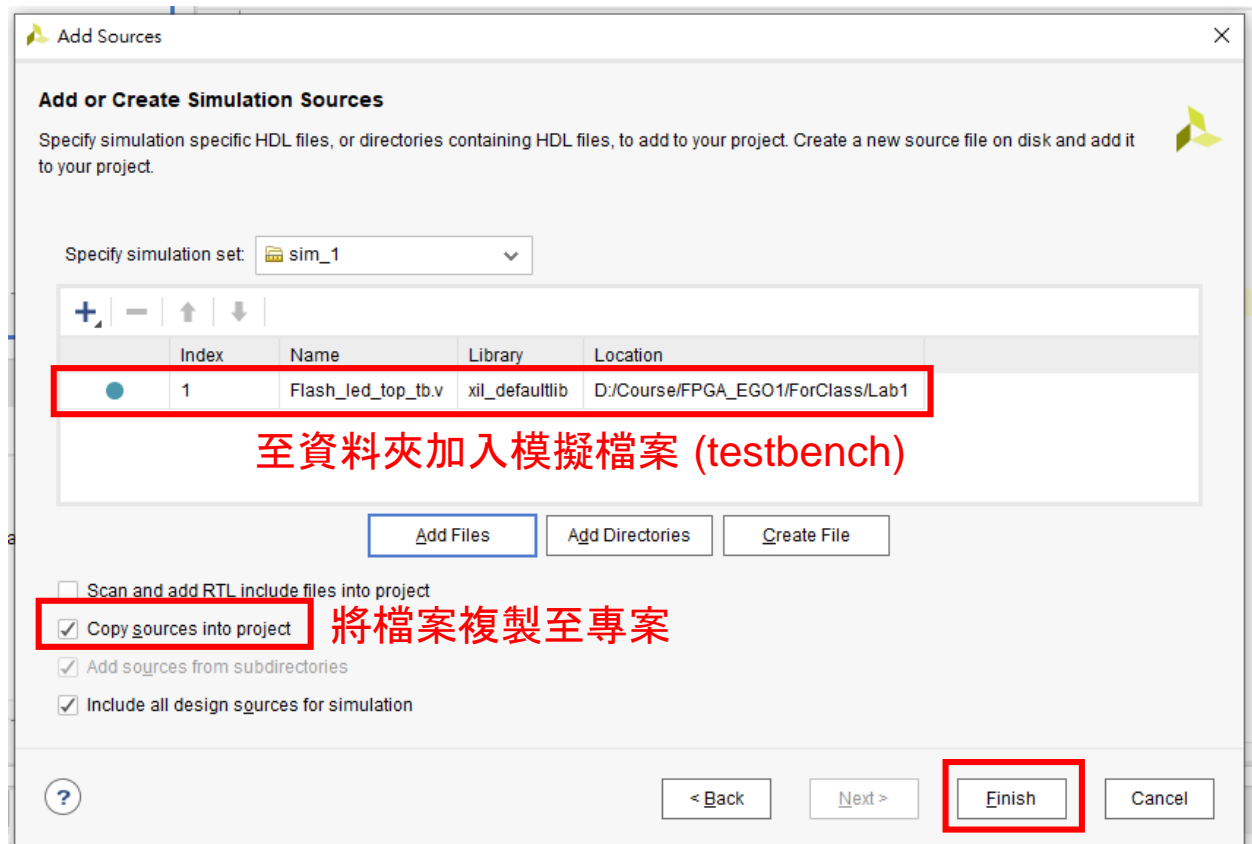
❖ 加入Simulation Source

❖ “Next”



# Vivado 2018.2

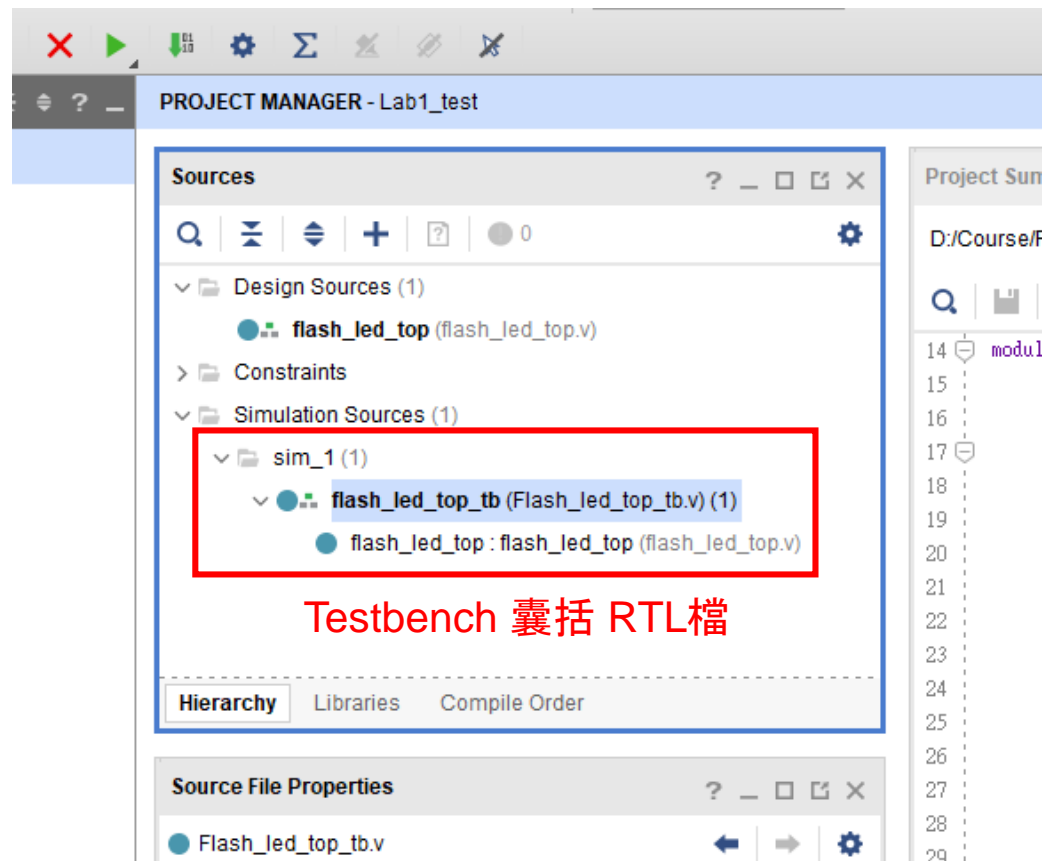
- ❖ 加入Simulation Source
- ❖ “Copy source into project”
- ❖ “Finish”





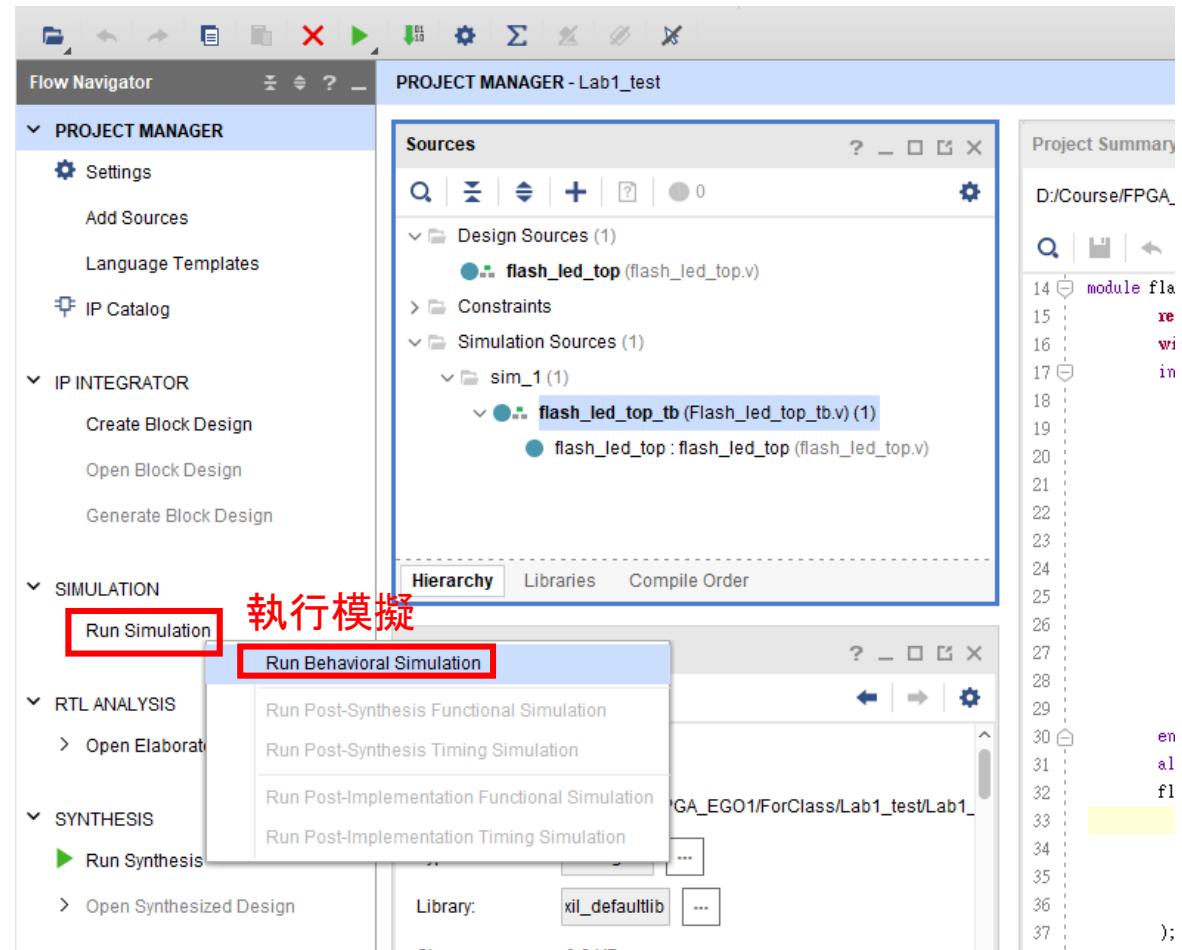
# Vivado 2018.2

- ❖ 確認加入Simulation Source
- ❖ 並且有抓到RTL檔



# Vivado 2018.2

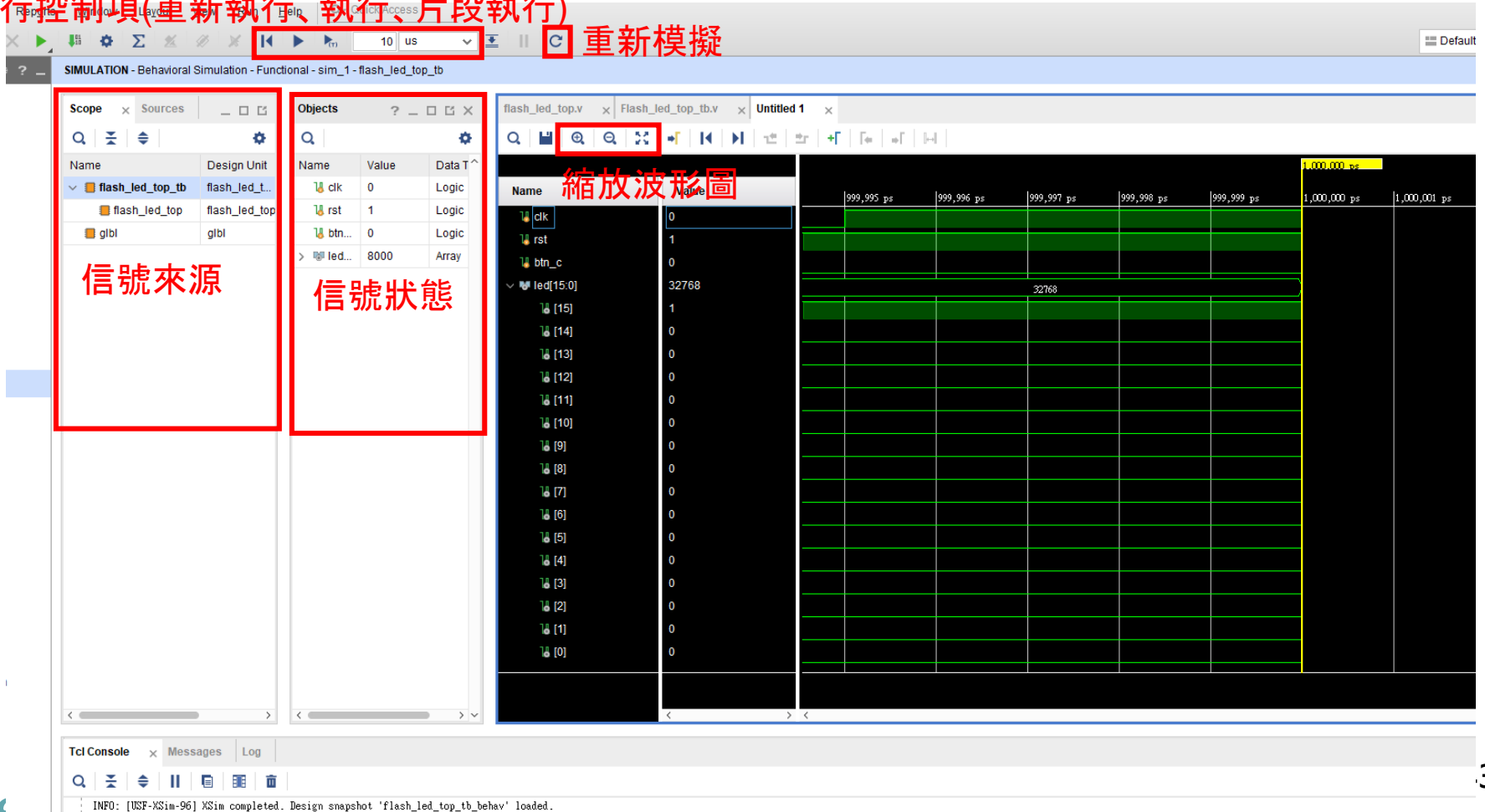
- ❖ 進行模擬
- ❖ “Run Simulation”
- ❖ “Run Behavioral Simulation”



# Vivado 2018.2

## ❖ 模擬版面介紹

執行控制項(重新執行、執行、片段執行)



The screenshot shows the Vivado 2018.2 simulation interface. The top toolbar contains execution controls: a red box highlights the 'Run' (play) button, and another red box highlights the 'Refresh' (circular arrow) button, with the text '重新模擬' (Reload Simulation) next to it. Below the toolbar, the 'Scope' window on the left is annotated with '信號來源' (Signal Source) and lists the design hierarchy: flash\_led\_top\_tb, flash\_led\_top, and glbl. The 'Objects' window in the center is annotated with '信號狀態' (Signal State) and shows a table of signal values: clk (0), rst (1), btn... (0), and led... (8000). The right side of the interface displays a waveform viewer with the title '縮放波形圖' (Zoomed Waveform). The waveform shows digital signals for clk, rst, btn\_c, and a 16-bit LED array (led[15:0]). A yellow vertical line is positioned at 1,000,000 ps. The bottom status bar shows the message: 'INFO: [USF-XSim-96] XSim completed. Design snapshot 'flash\_led\_top\_tb\_behav' loaded.'

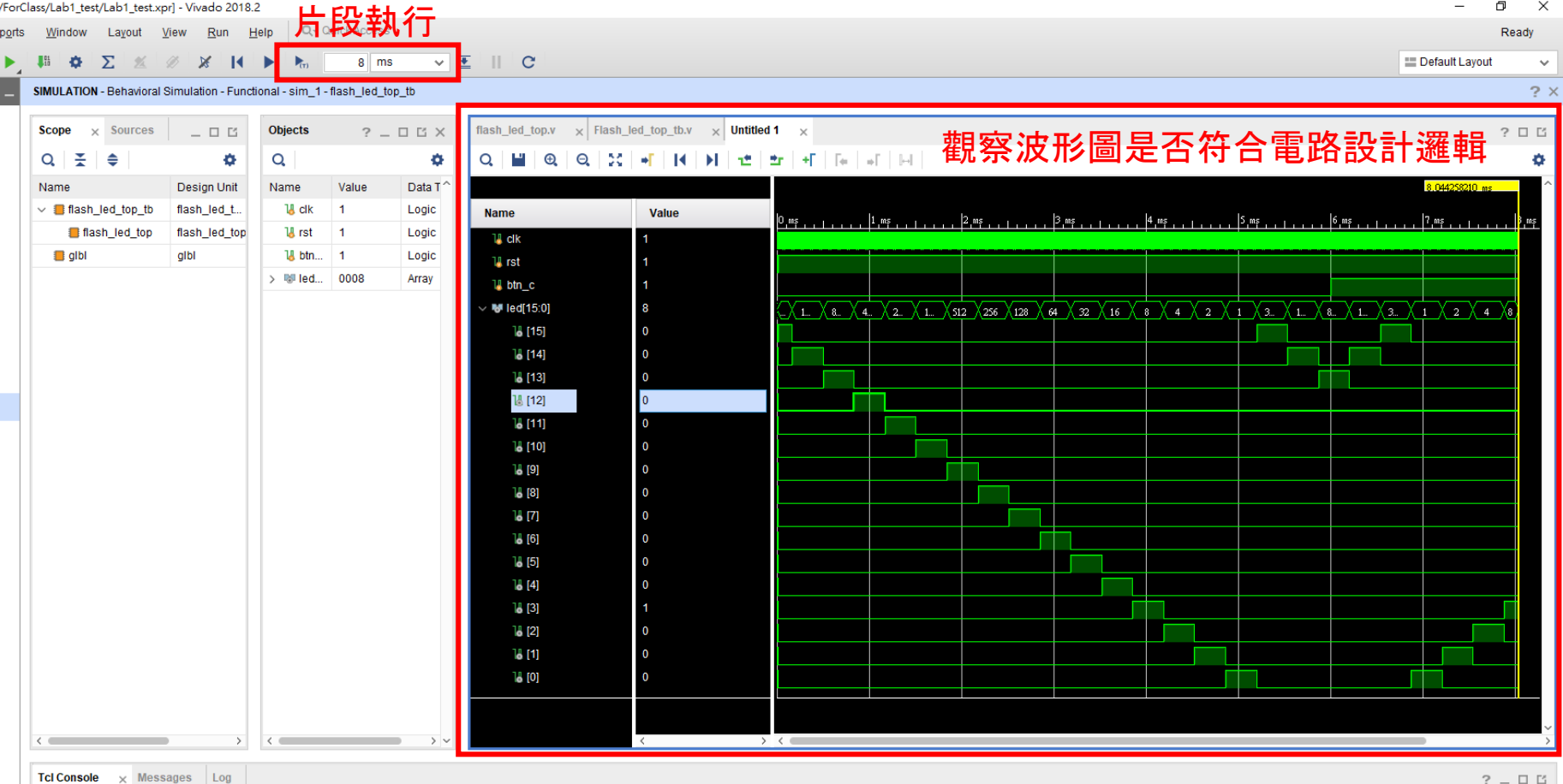
Name	Value	Data Type
clk	0	Logic
rst	1	Logic
btn...	0	Logic
led...	8000	Array

# Vivado 2018.2

❖ 再往前執行8ms

片段執行

觀察波形圖是否符合電路設計邏輯

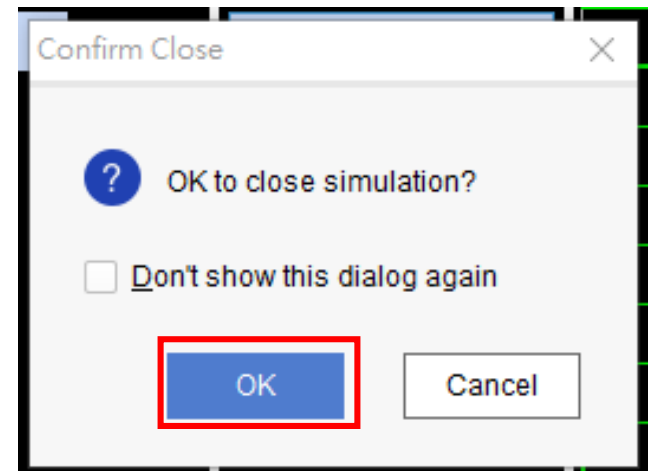
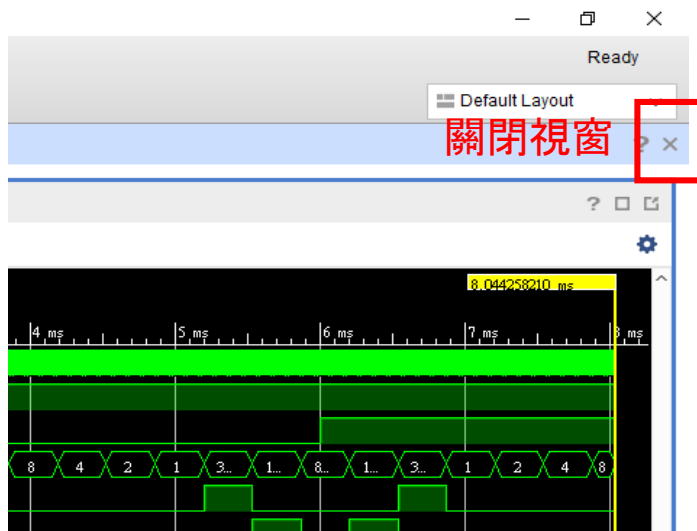


Name	Value	Data Type
clk	1	Logic
rst	1	Logic
btn...	1	Logic
led...	0008	Array

Name	Value
clk	1
rst	1
btn_c	1
led[15:0]	8
led[15]	0
led[14]	0
led[13]	0
led[12]	0
led[11]	0
led[10]	0
led[9]	0
led[8]	0
led[7]	0
led[6]	0
led[5]	0
led[4]	0
led[3]	1
led[2]	0
led[1]	0
led[0]	0

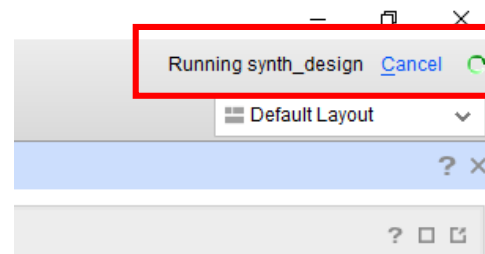
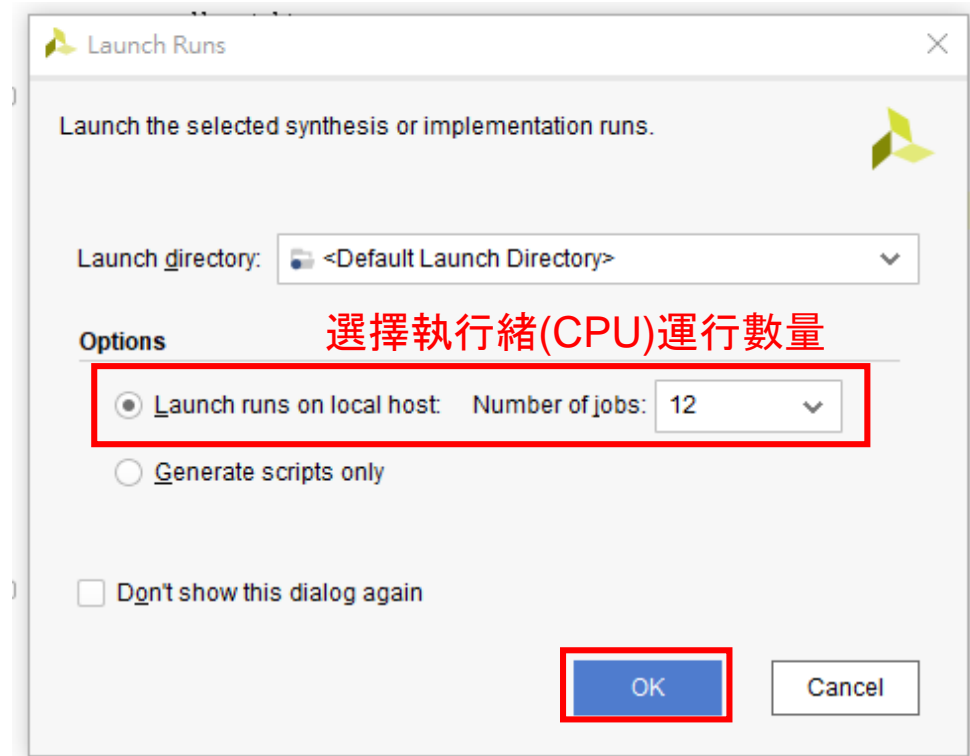
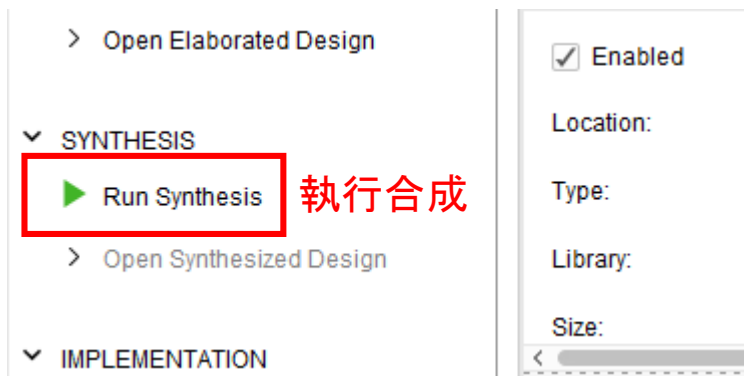
# Vivado 2018.2

- ❖ 沒問題，關閉Simulation視窗
- ❖ “OK”



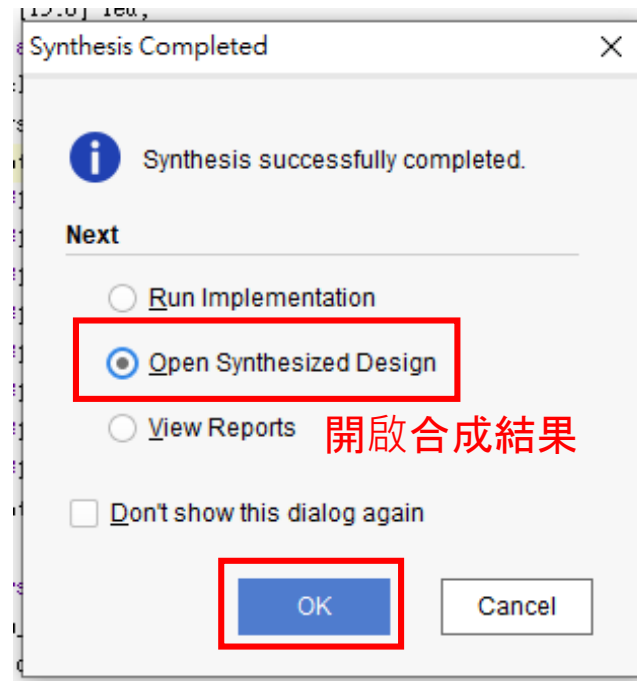
# Vivado 2018.2

- ❖ 執行合成
- ❖ “Run Synthesis”
- ❖ “OK”



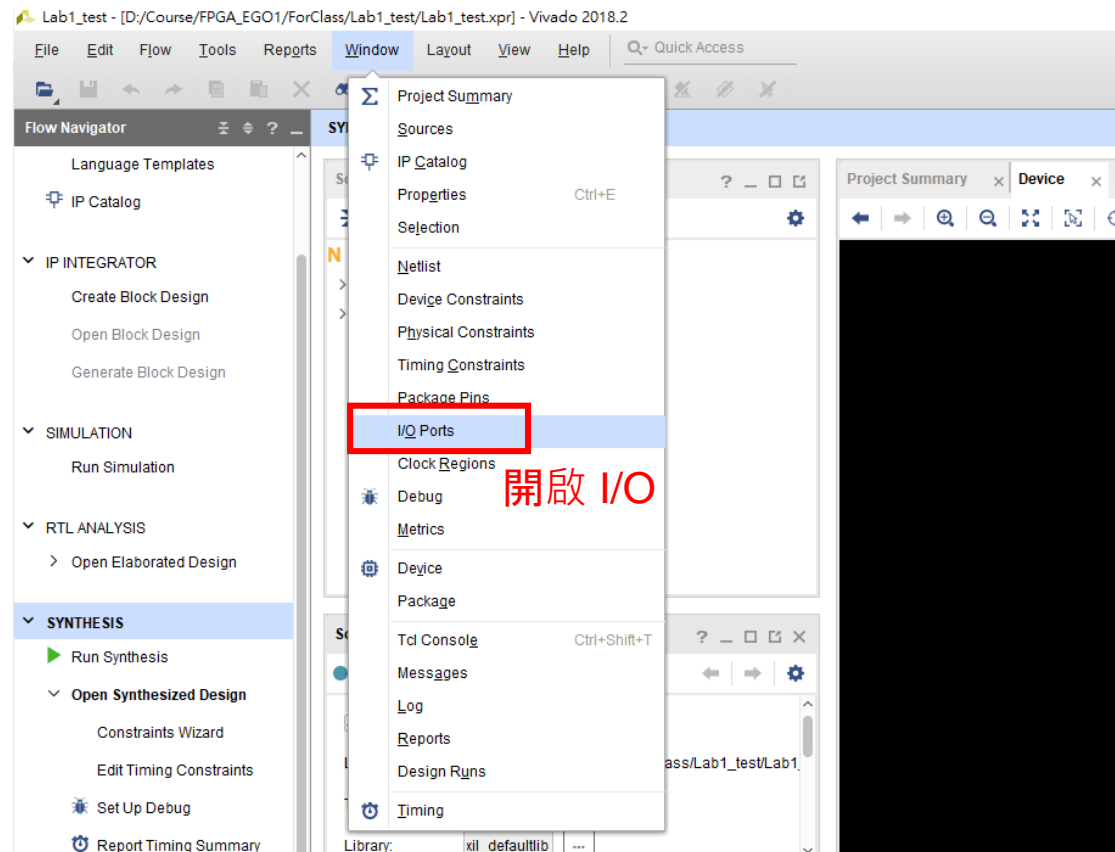
# Vivado 2018.2

- ❖ 合成完畢，開啟合成結果
- ❖ “Open Synthesized Design”
- ❖ “OK”



# Vivado 2018.2

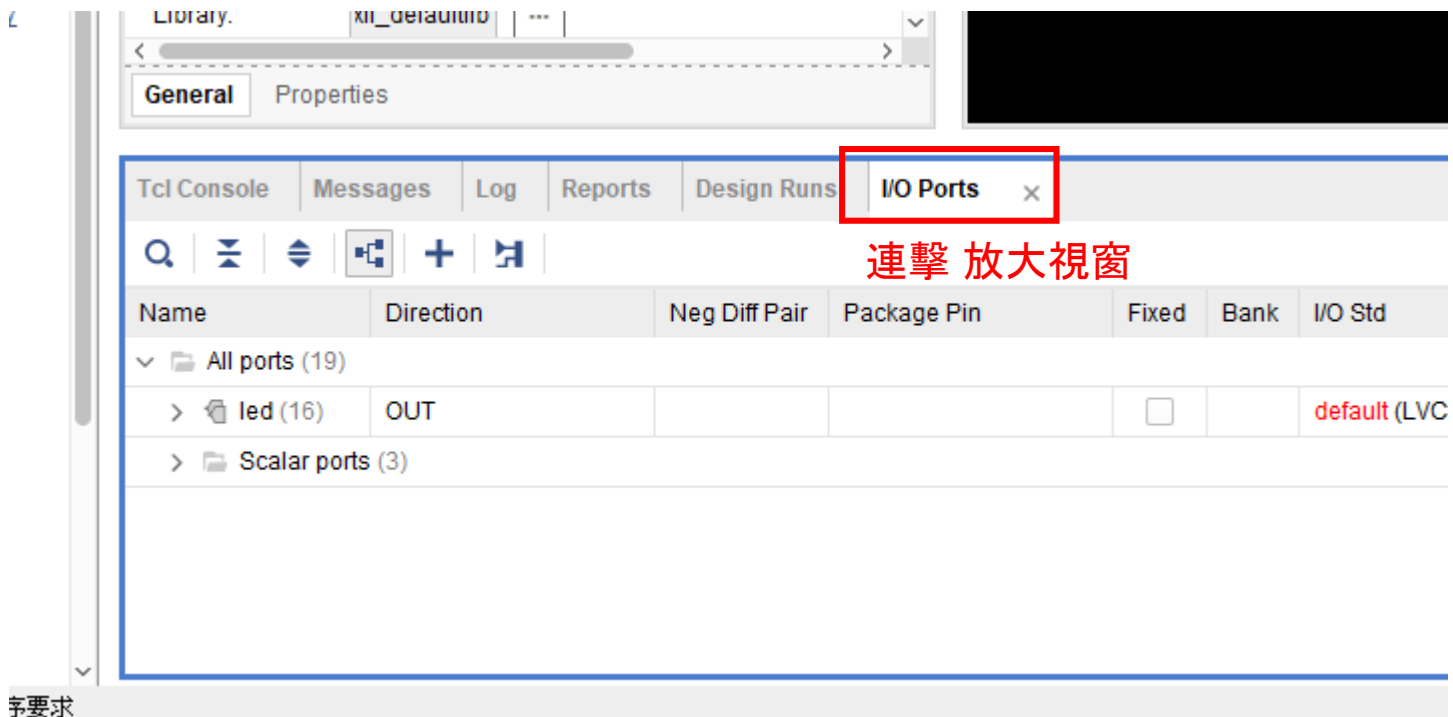
- ❖ 設定腳位資料
- ❖ “Window”→“I/O Ports”





# Vivado 2018.2

- ❖ 於下方視窗出現I/O Ports
- ❖ 連擊 I/O Ports標題放大視窗



# Vivado 2018.2

- ❖ 將I/O Ports 設定至對應的腳位、工作電壓(LVCMOS33)
- ❖ 參考前面的腳位對應表

SYNTHESIZED DESIGN \* - xc7a35tcs9324-1 (active)

Tcl Console Messages Log Reports Design Runs I/O Ports x

選擇工作電壓 (3.3V)

輸入或選擇對應腳位

Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	Slew Type	Pull Type	Off-Chip Termination	IN_TERM
All ports (19)													
led[15]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[14]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[13]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[12]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[11]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[10]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[9]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[8]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[7]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[6]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[5]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[4]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[3]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[2]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[1]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
led[0]	OUT					LVC MOS33*	3.300		12	SLOW	NONE	FP_VTT_50	
Scalar ports (3)													
btn_c	IN					LVC MOS33*	3.300				NONE	NONE	
clk	IN					LVC MOS33*	3.300				NONE	NONE	
rst_n	IN					LVC MOS33*	3.300				NONE	NONE	

# Vivado 2018.2

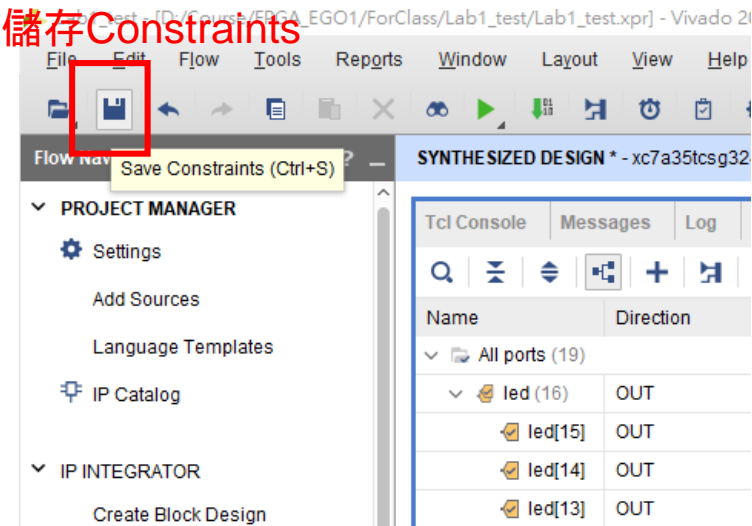
- ❖ 確認腳位設定
- ❖ 儲存約束檔案 Constraint

Tcl Console Messages Log Reports Design Runs I/O Ports

確認是否都完成設定

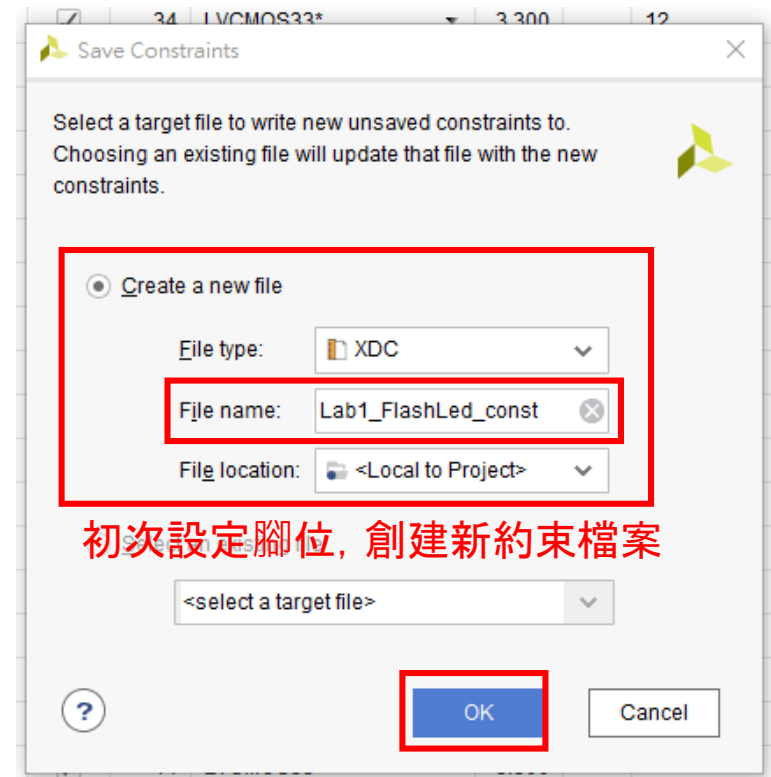
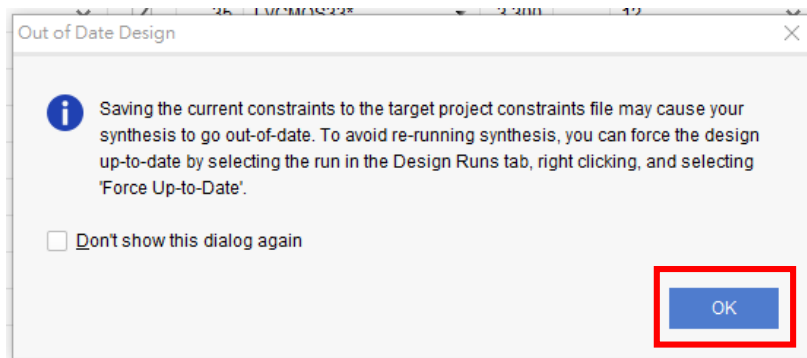
Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vre	Drive St
▼ All ports (19)									
▼ led (16)	OUT			✓	(Multiple)	LVC MOS33*	3.300		12
led[15]	OUT		F6	✓	35	LVC MOS33*	3.300		12
led[14]	OUT		G4	✓	35	LVC MOS33*	3.300		12
led[13]	OUT		G3	✓	35	LVC MOS33*	3.300		12
led[12]	OUT		J4	✓	35	LVC MOS33*	3.300		12
led[11]	OUT		H4	✓	35	LVC MOS33*	3.300		12
led[10]	OUT		J3	✓	35	LVC MOS33*	3.300		12
led[9]	OUT		J2	✓	35	LVC MOS33*	3.300		12
led[8]	OUT		K2	✓	35	LVC MOS33*	3.300		12
led[7]	OUT		K1	✓	35	LVC MOS33*	3.300		12
led[6]	OUT		H6	✓	35	LVC MOS33*	3.300		12
led[5]	OUT		H5	✓	35	LVC MOS33*	3.300		12
led[4]	OUT		J5	✓	35	LVC MOS33*	3.300		12
led[3]	OUT		K6	✓	34	LVC MOS33*	3.300		12
led[2]	OUT		L1	✓	34	LVC MOS33*	3.300		12
led[1]	OUT		M1	✓	34	LVC MOS33*	3.300		12
led[0]	OUT		K3	✓	34	LVC MOS33*	3.300		12
▼ Scalar ports (3)									
btn_c	IN		R15	✓	14	LVC MOS33*	3.300		
clk	IN		P17	✓	14	LVC MOS33*	3.300		
rst_n	IN		P15	✓	14	LVC MOS33*	3.300		

儲存 Constraints



# Vivado 2018.2

- ❖ 提醒儲存約束檔案，會導致合成結果過期，需重新合成
- ❖ “OK”
- ❖ 設定腳位檔名稱
- ❖ “OK”



# Vivado 2018.2

## ❖ 關閉 Synthesized Design

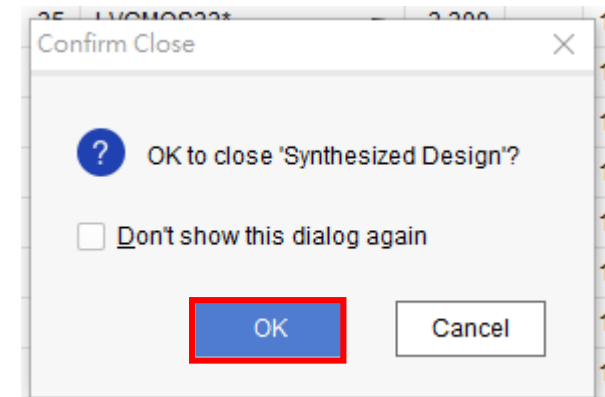
合成過期

Synthesis Out-of-date details

Default Layout

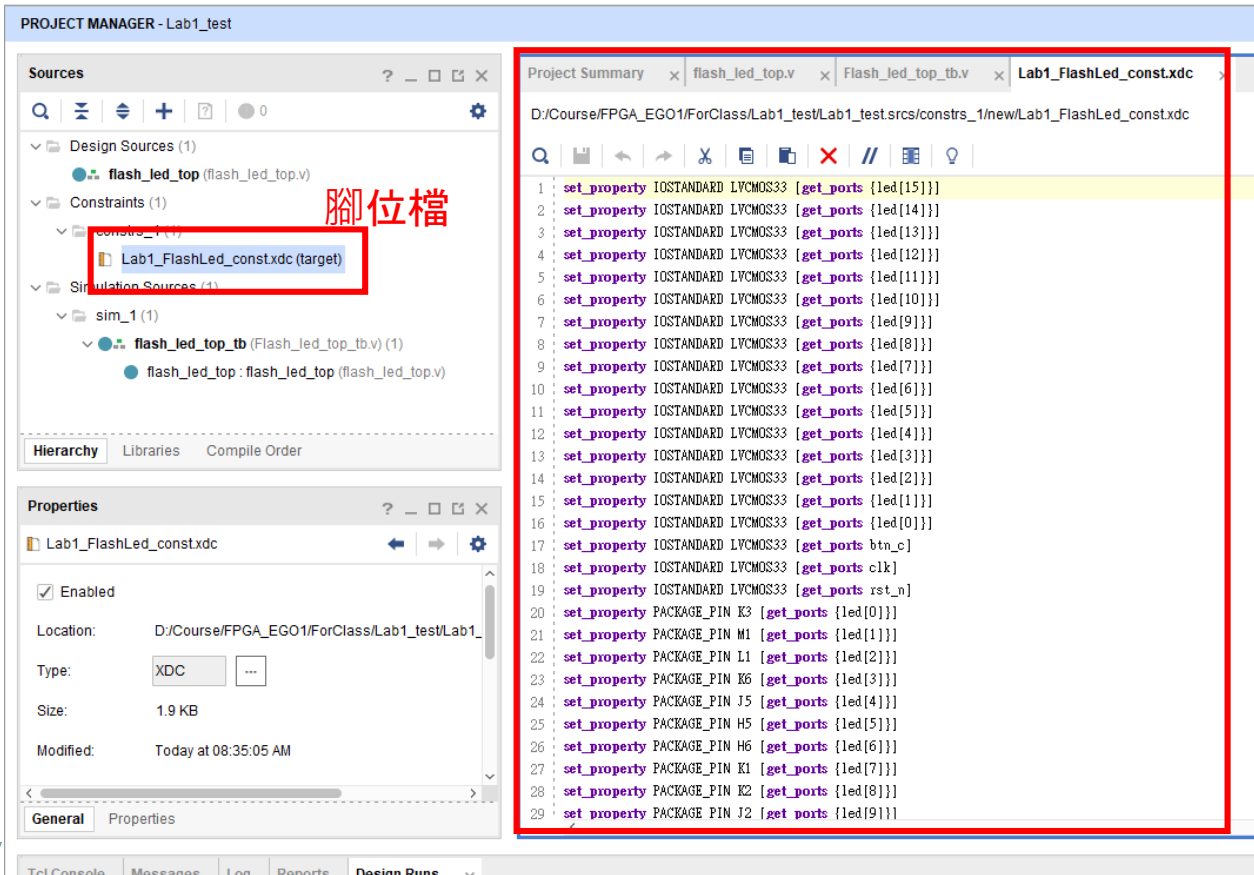
關閉 Synthesized Design

All Type	Off-Chip Termination	IN_TERM
ONE	FP_VTT_50	
ONE	FP_VTT_50	
ONE	FP_VTT_50	
ONE	FP_VTT_50	
ONE	FP_VTT_50	
ONE	FP_VTT_50	
ONE	FP_VTT_50	
ONE	FP_VTT_50	



# Vivado 2018.2

- ❖ 查看腳位檔(.xdc檔)
- ❖ 在接下來的實驗中將通過直接添加constraints的方式來對設計進行腳位分配。



The screenshot displays the Vivado 2018.2 Project Manager interface for a project named 'Lab1\_test'. In the 'Sources' window, the 'Constraints' section shows a file named 'Lab1\_FlashLed\_const.xdc (target)' highlighted with a red box. A red label '腳位檔' (Pin Configuration File) points to this file. The 'Properties' window for this file shows it is an 'XDC' file, located at 'D:/Course/FPGA\_EGO1/ForClass/Lab1\_test/Lab1\_'. The right pane shows the content of the XDC file, which is a list of 'set\_property' commands for pin configuration. The commands are as follows:

```
1 set_property IOSTANDARD LVCMOS33 [get_ports {led[15]]}
2 set_property IOSTANDARD LVCMOS33 [get_ports {led[14]]}
3 set_property IOSTANDARD LVCMOS33 [get_ports {led[13]]}
4 set_property IOSTANDARD LVCMOS33 [get_ports {led[12]]}
5 set_property IOSTANDARD LVCMOS33 [get_ports {led[11]]}
6 set_property IOSTANDARD LVCMOS33 [get_ports {led[10]]}
7 set_property IOSTANDARD LVCMOS33 [get_ports {led[9]]}
8 set_property IOSTANDARD LVCMOS33 [get_ports {led[8]]}
9 set_property IOSTANDARD LVCMOS33 [get_ports {led[7]]}
10 set_property IOSTANDARD LVCMOS33 [get_ports {led[6]]}
11 set_property IOSTANDARD LVCMOS33 [get_ports {led[5]]}
12 set_property IOSTANDARD LVCMOS33 [get_ports {led[4]]}
13 set_property IOSTANDARD LVCMOS33 [get_ports {led[3]]}
14 set_property IOSTANDARD LVCMOS33 [get_ports {led[2]]}
15 set_property IOSTANDARD LVCMOS33 [get_ports {led[1]]}
16 set_property IOSTANDARD LVCMOS33 [get_ports {led[0]]}
17 set_property IOSTANDARD LVCMOS33 [get_ports btn_c]
18 set_property IOSTANDARD LVCMOS33 [get_ports clk]
19 set_property IOSTANDARD LVCMOS33 [get_ports rst_n]
20 set_property PACKAGE_PIN K3 [get_ports {led[0]]}
21 set_property PACKAGE_PIN M1 [get_ports {led[1]]}
22 set_property PACKAGE_PIN L1 [get_ports {led[2]]}
23 set_property PACKAGE_PIN X6 [get_ports {led[3]]}
24 set_property PACKAGE_PIN J5 [get_ports {led[4]]}
25 set_property PACKAGE_PIN H5 [get_ports {led[5]]}
26 set_property PACKAGE_PIN H6 [get_ports {led[6]]}
27 set_property PACKAGE_PIN K1 [get_ports {led[7]]}
28 set_property PACKAGE_PIN K2 [get_ports {led[8]]}
29 set_property PACKAGE_PIN J2 [get_ports {led[9]]}
```

# Vivado 2018.2

## ❖ 重新進行合成(Synthesis)

SYNTHESIS 進行合成

▶ Run Synthesis

Open Synthesized Design

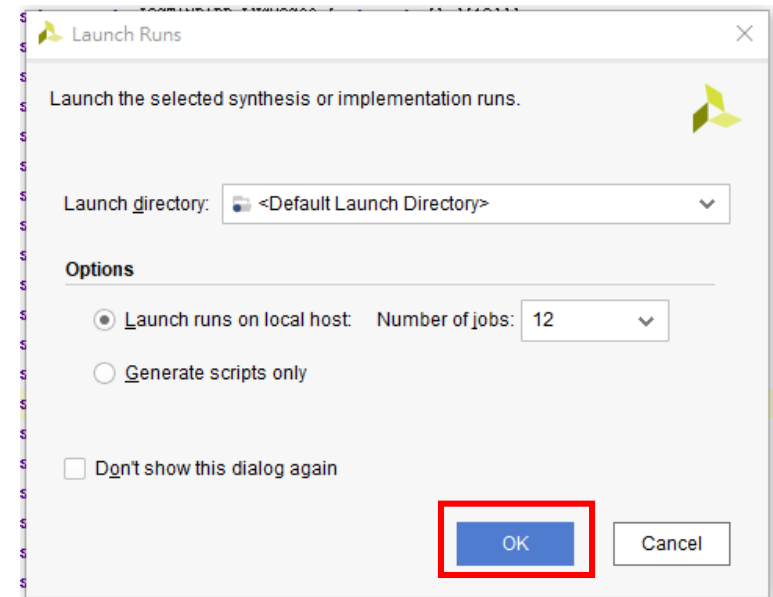
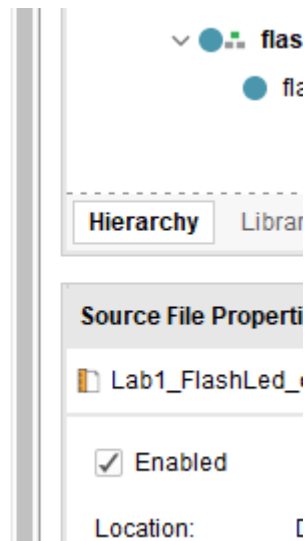
Constraints Wizard

Edit Timing Constraints

Set Up Debug

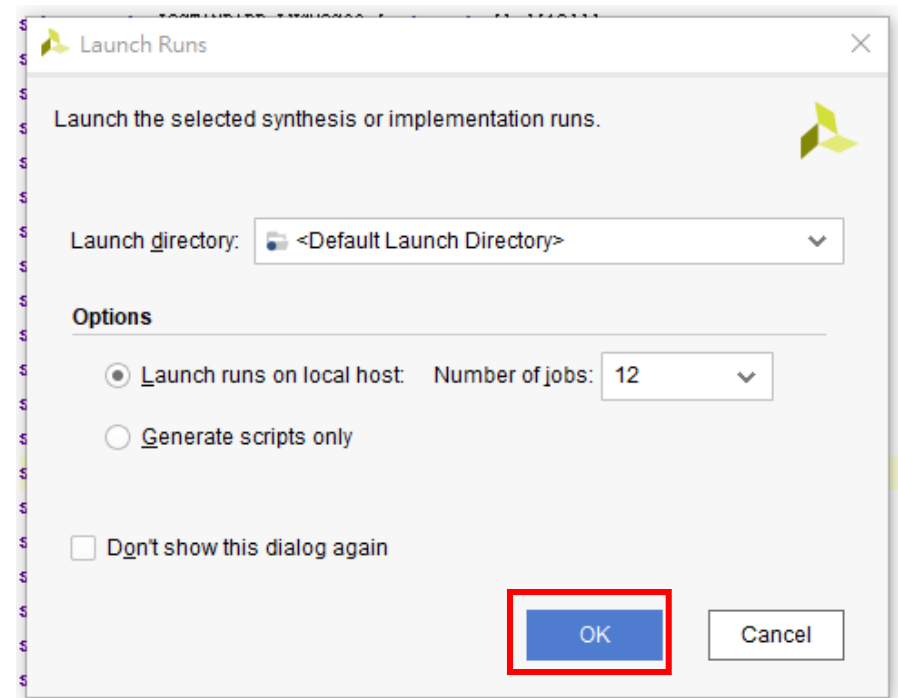
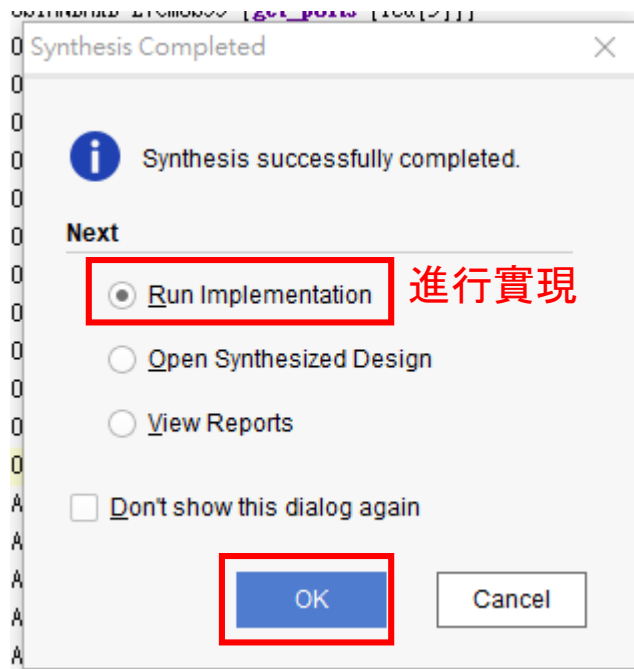
Report Timing Summary

Report Clock Networks



# Vivado 2018.2

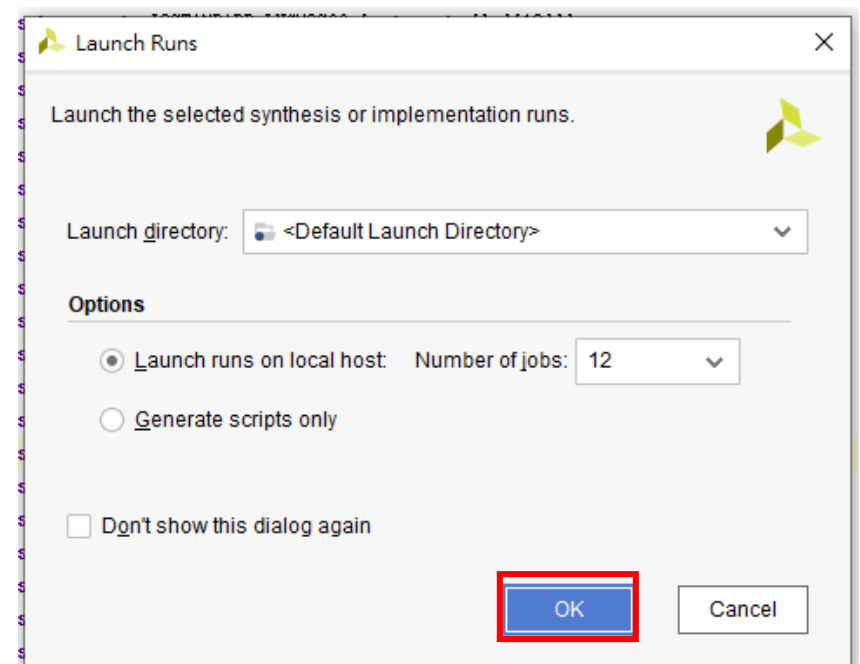
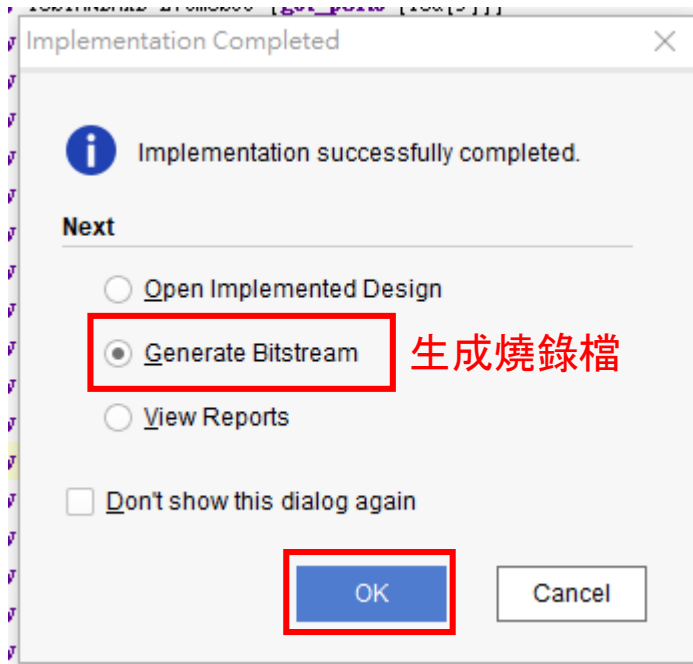
- ❖ 進行實現 (Implementation)
- ❖ “Run Implementation”
- ❖ “OK” “OK”





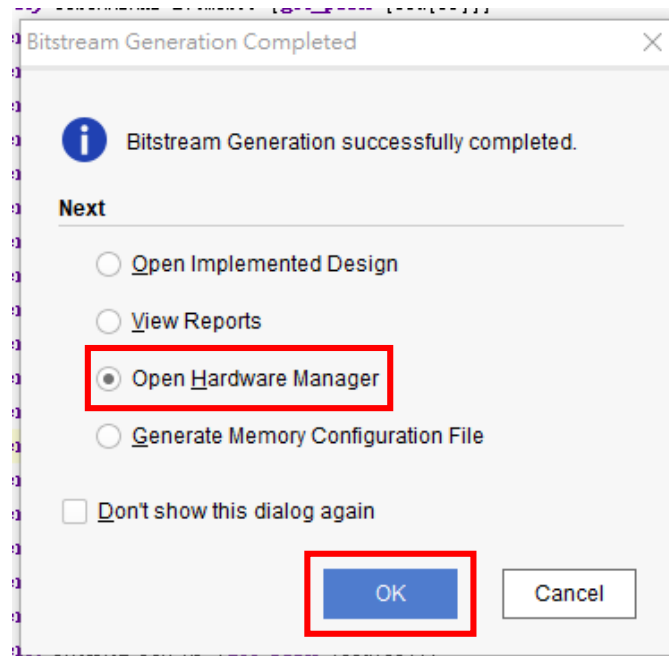
# Vivado 2018.2

- ❖ 生成燒錄檔 (Bitstream)
- ❖ “Generate Bitstream”
- ❖ “OK” “OK”



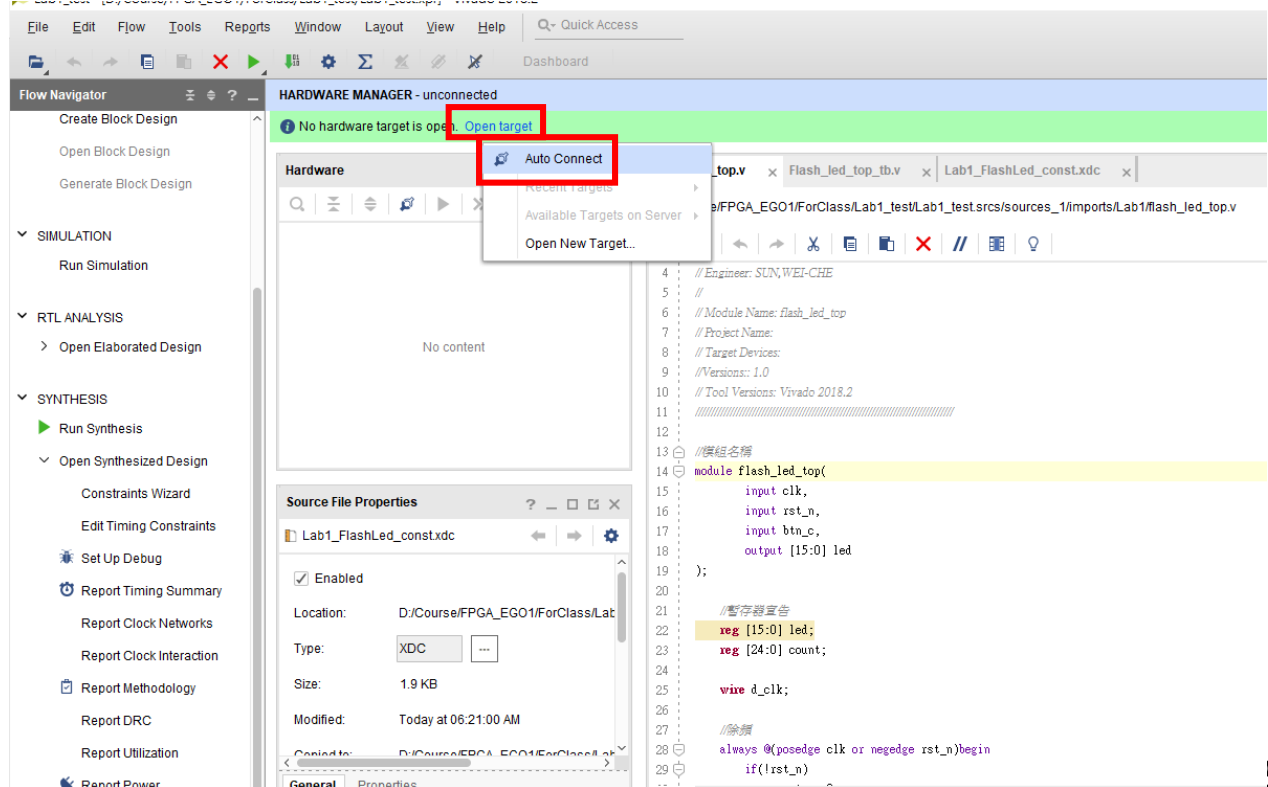
# Vivado 2018.2

- ❖ 生成燒錄檔完成後，選擇“Open Hardware Manager”



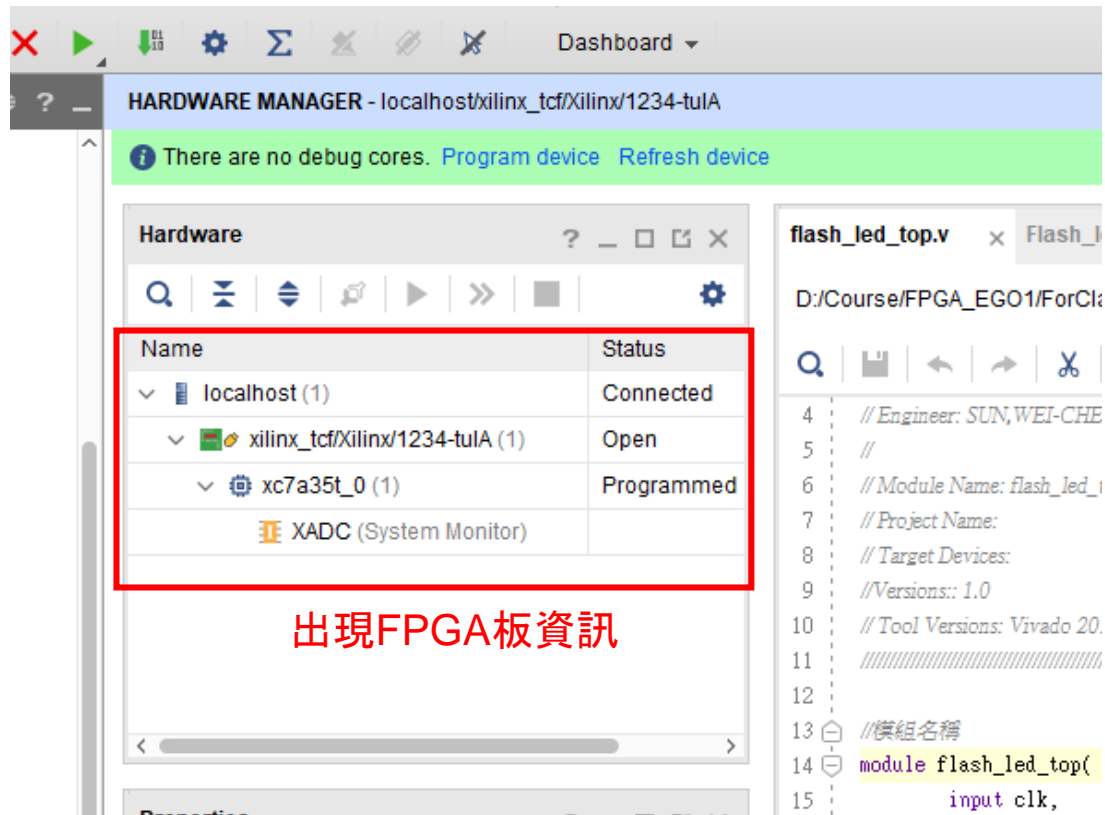
# Vivado 2018.2

- ❖ 將FPGA板連接至電腦，並開啟電源，才能讓軟體偵測到板子
- ❖ 點擊“Open target”，選擇“Auto Connect”



# Vivado 2018.2

- ❖ 出現FPGA板資訊，表示成功連接至電腦



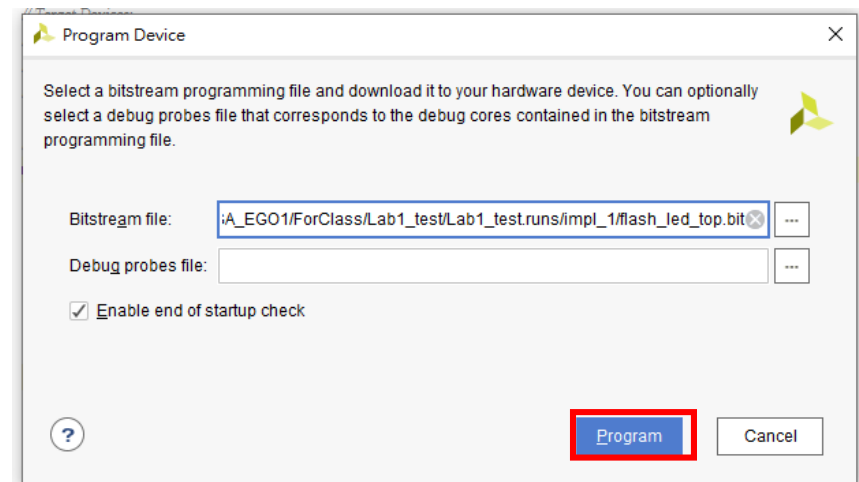
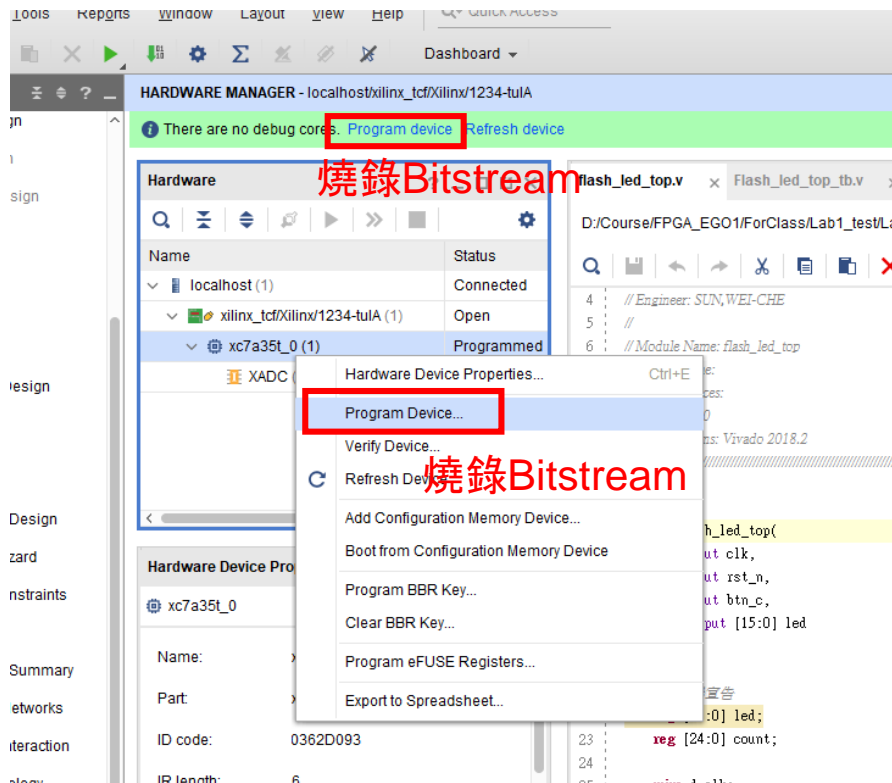
The screenshot shows the Vivado 2018.2 Hardware Manager window. The title bar reads "HARDWARE MANAGER - localhost/xilinx\_tcf/Xilinx/1234-tula". A green banner at the top states "There are no debug cores. Program device Refresh device". The main area displays a table of hardware components:

Name	Status
localhost (1)	Connected
xilinx_tcf/Xilinx/1234-tula (1)	Open
xc7a35t_0 (1)	Programmed
XADC (System Monitor)	

A red rectangle highlights the table content. Below the table, the text "出現FPGA板資訊" (FPGA board information appears) is written in red. The right pane shows the Verilog code for "flash\_led\_top.v".

# Vivado 2018.2

- ❖ 將Bitstream燒錄至FPGA板
- ❖ 點擊“Program”



# Vivado 2018.2



國立中興大學  
National Chung Hsing University

❖ 完成燒錄!!!

Synthesis

Verilog

Implementation

Vivado

Program .v

FPGA

Bitstream

testbench

.xdc

I/O Ports





**Thank you for your  
attention!**

