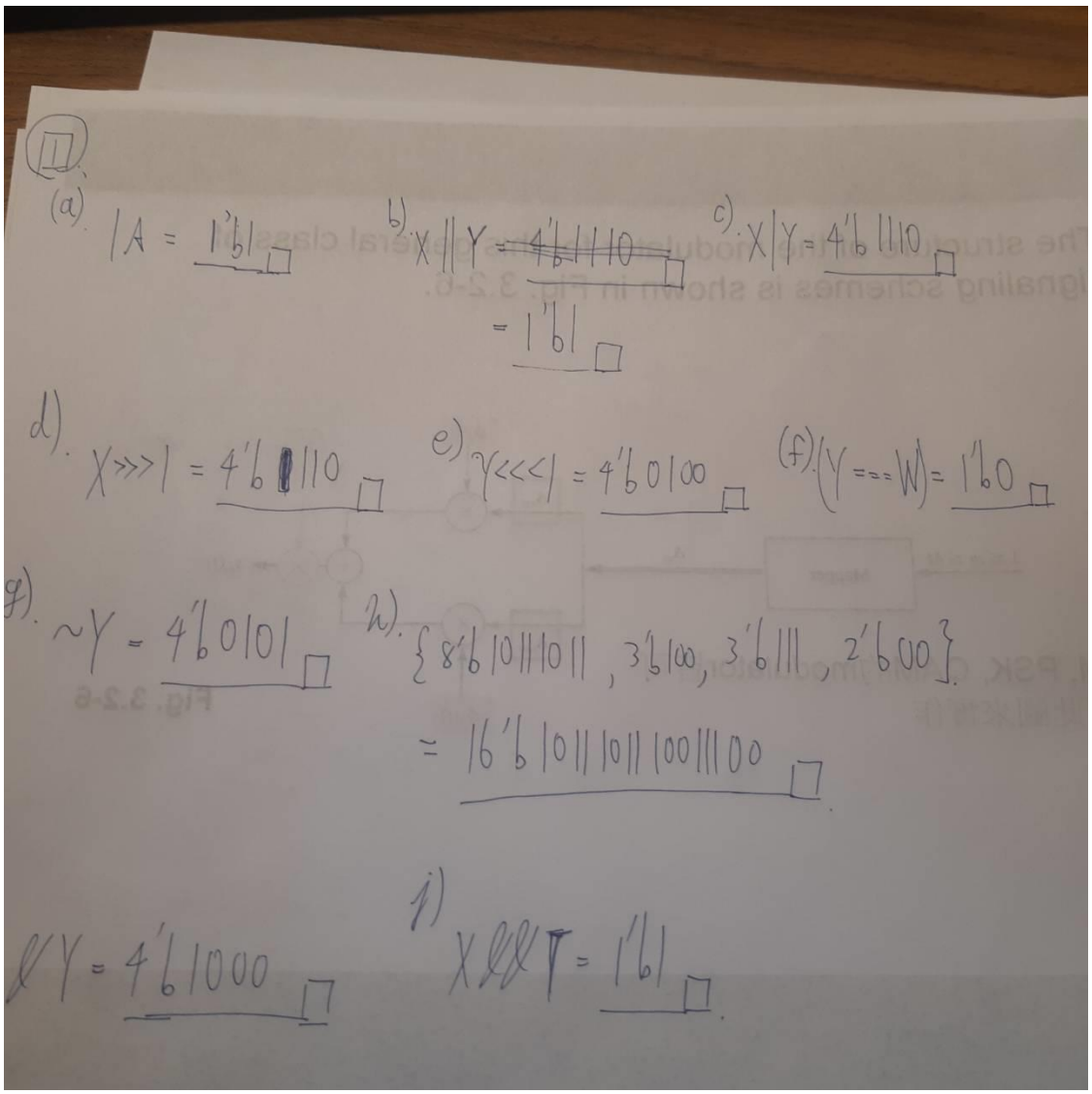
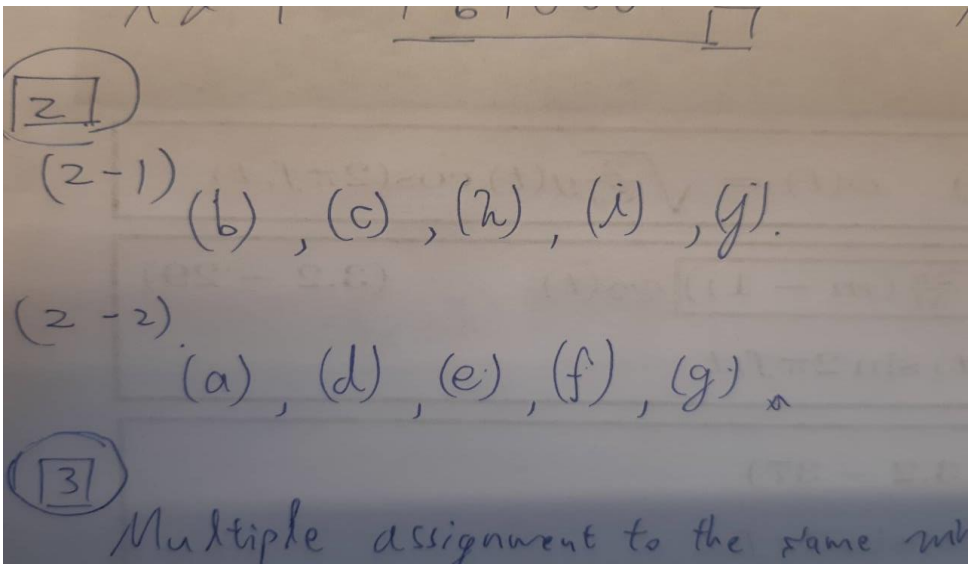
FPGA 期末考， 111 年 6 月 15 日(星期三)下午 3:10-5:00

班級 ____四 A_____， 學號 4107064003， 姓名 葉舜良

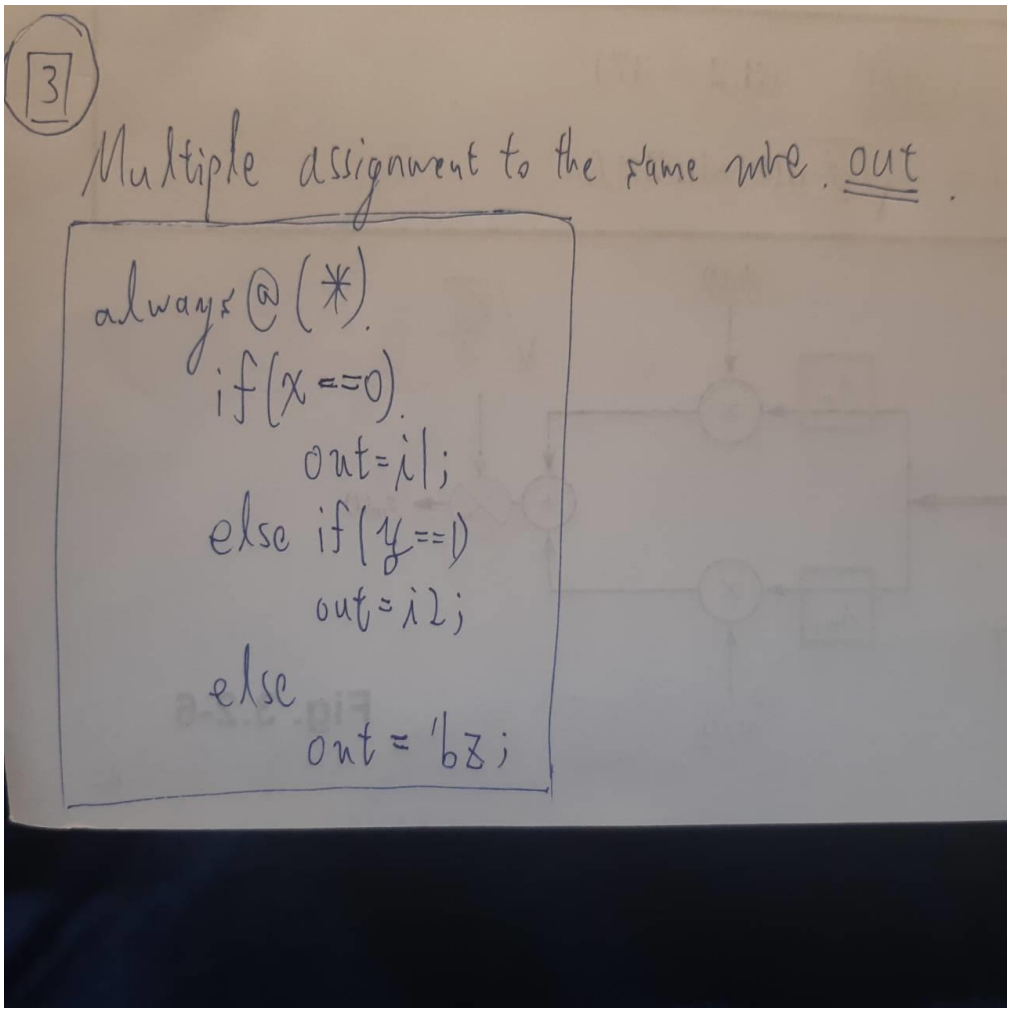
(1)



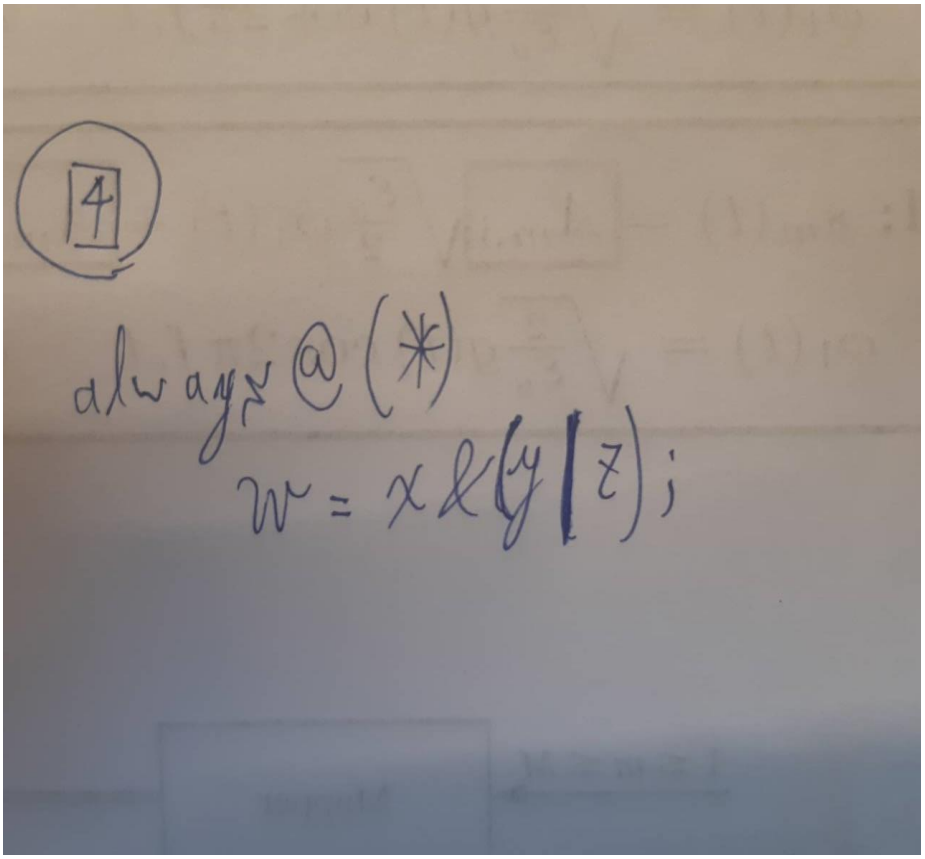
(2)



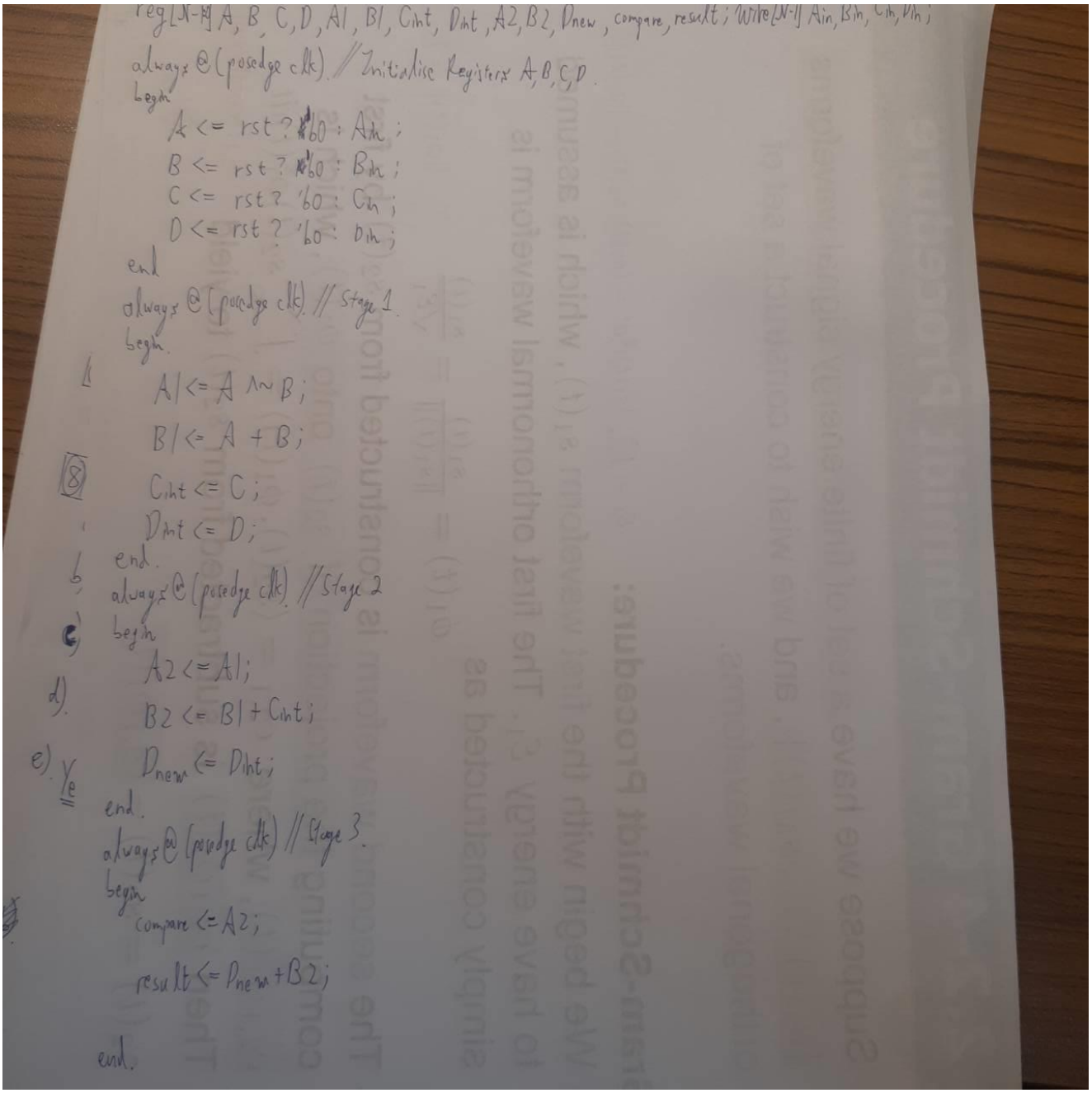
(3)


3
Multiple assignment to the same wire. out.
always @(*)
if(x==0)
out=i1;
else if(y==1)
out=i2;
else
out='bz;

(4)

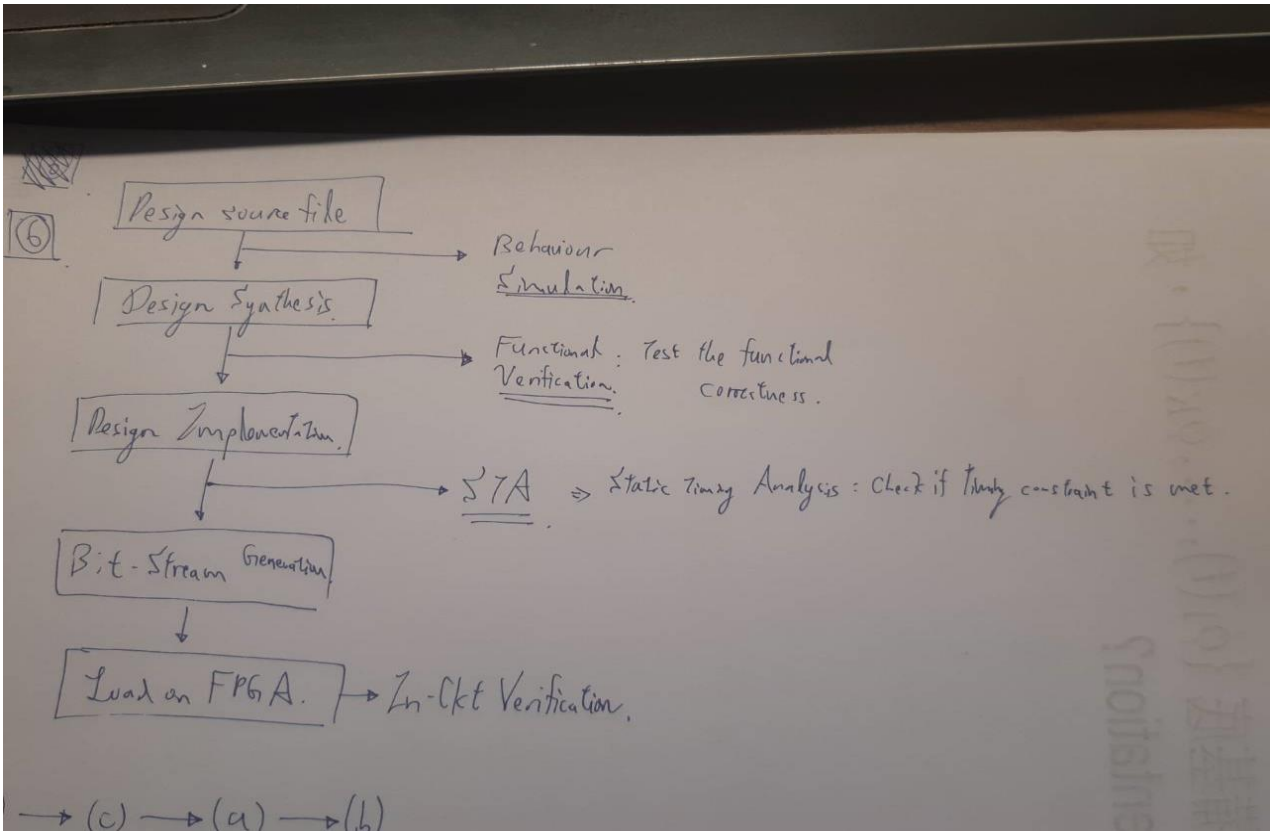

4
always @(*)
w=x&(y|z);

(5)

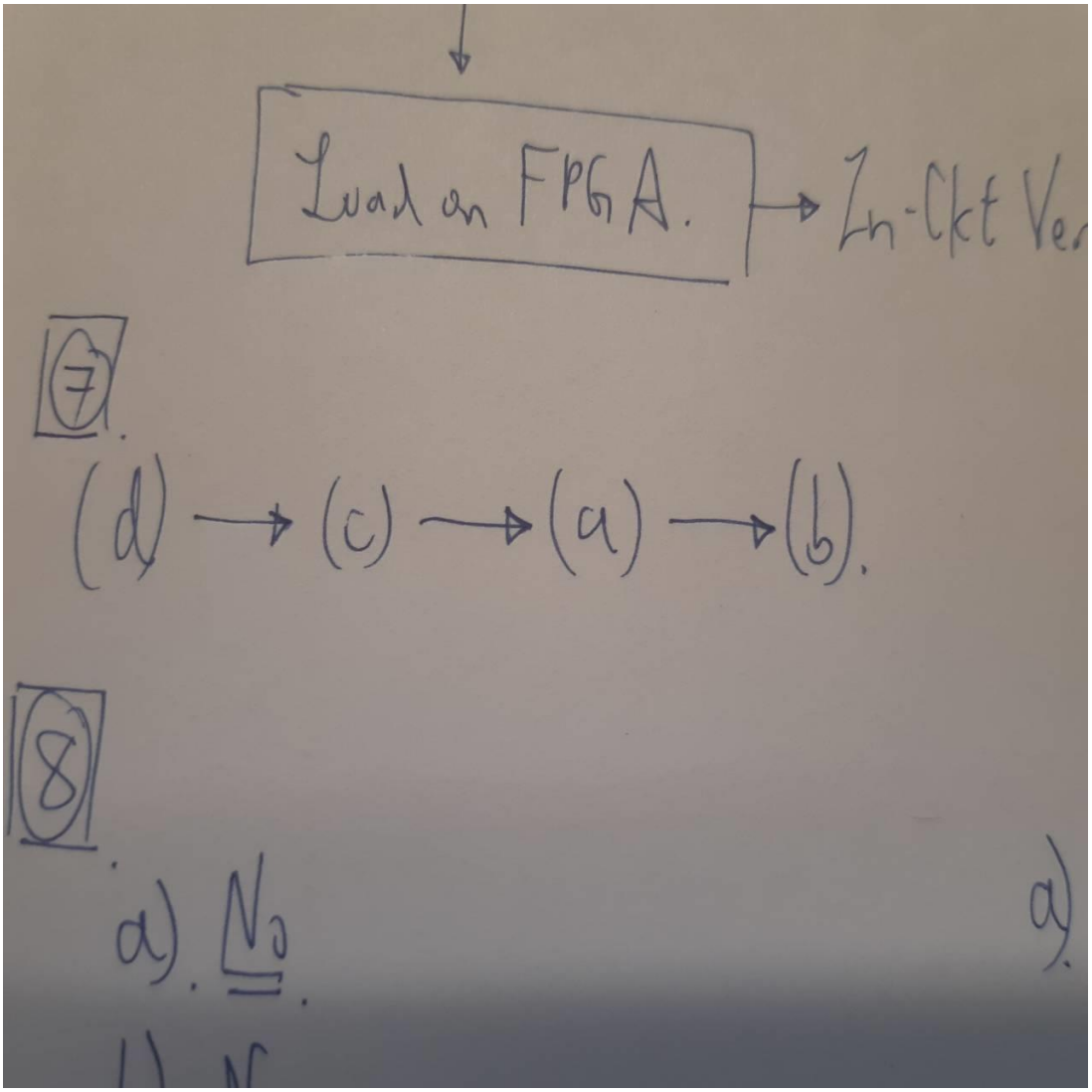


```
reg[N-1] A, B, C, D, A1, B1, Cint, Dint, A2, B2, Dnew, compare, result; wire[N-1] Ain, Bin, Cin, Din;
always @(posedge clk) // Initialise Registers A, B, C, D.
begin
    A <= rst ? 'b0 : Ain;
    B <= rst ? 'b0 : Bin;
    C <= rst ? 'b0 : Cin;
    D <= rst ? 'b0 : Din;
end
always @(posedge clk) // Stage 1.
begin
a)  A1 <= A ^ B;
    B1 <= A + B;
b)  Cint <= C;
    Dint <= D;
end.
always @(posedge clk) // Stage 2
begin
c)  A2 <= A1;
d)  B2 <= B1 + Cint;
e)  Dnew <= Dint;
end.
always @(posedge clk) // Stage 3.
begin
    compare <= A2;
    result <= Dnew + B2;
end.
```

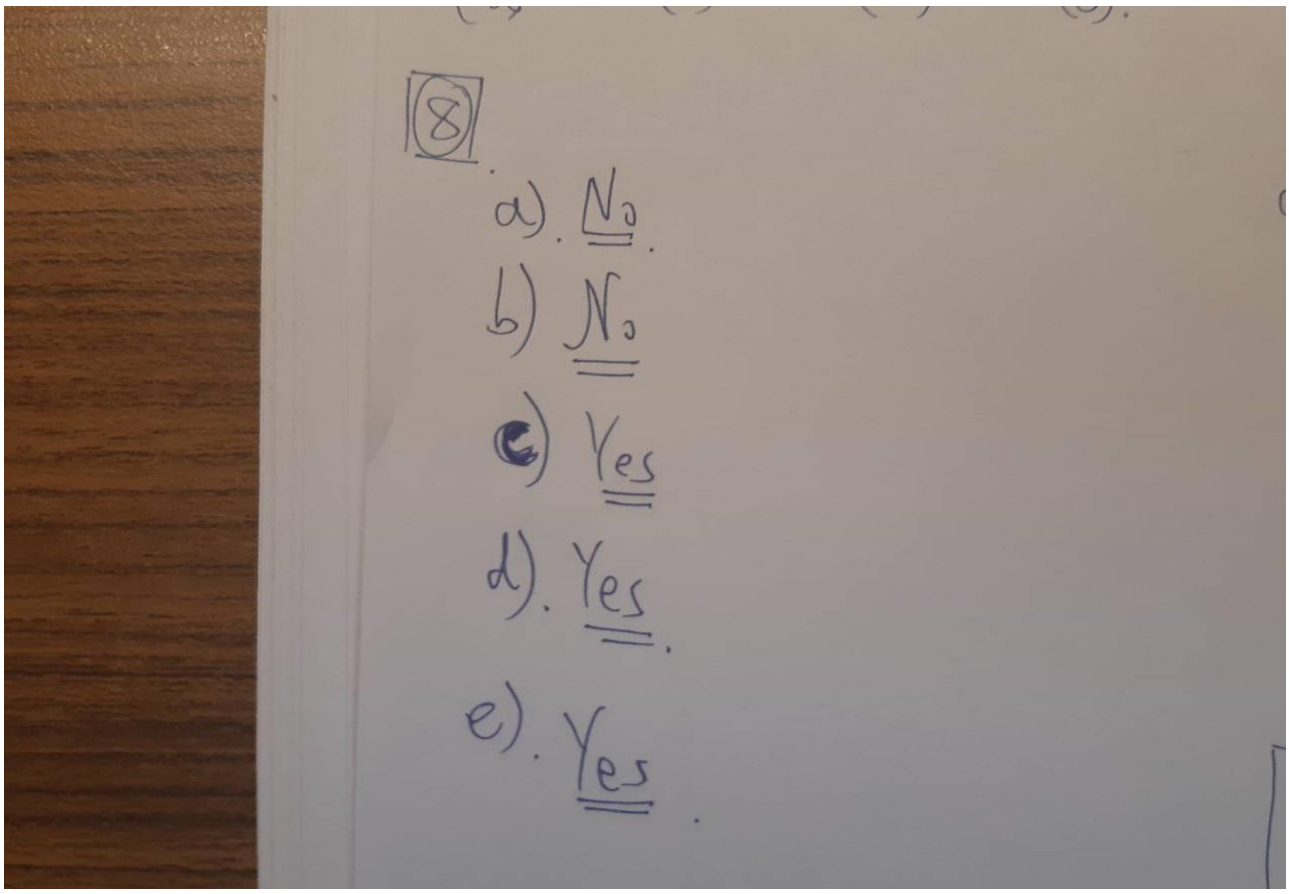
(6)


⑥
Design source file
Behaviour Simulation.
Design Synthesis
Functional Verification.
Test the functional correctness.
Design Implementation
STA ⇒ Static Timing Analysis : Check if timing constraint is met.
Bit-Stream Generation
Load on FPGA. → In-Ckt Verification.
→ (c) → (a) → (b)

(7)


Load on FPGA. → In-Ckt Ver
⑦
(d) → (c) → (a) → (b).
⑧
a). No.
a).

(8)



⑧.

a). No.

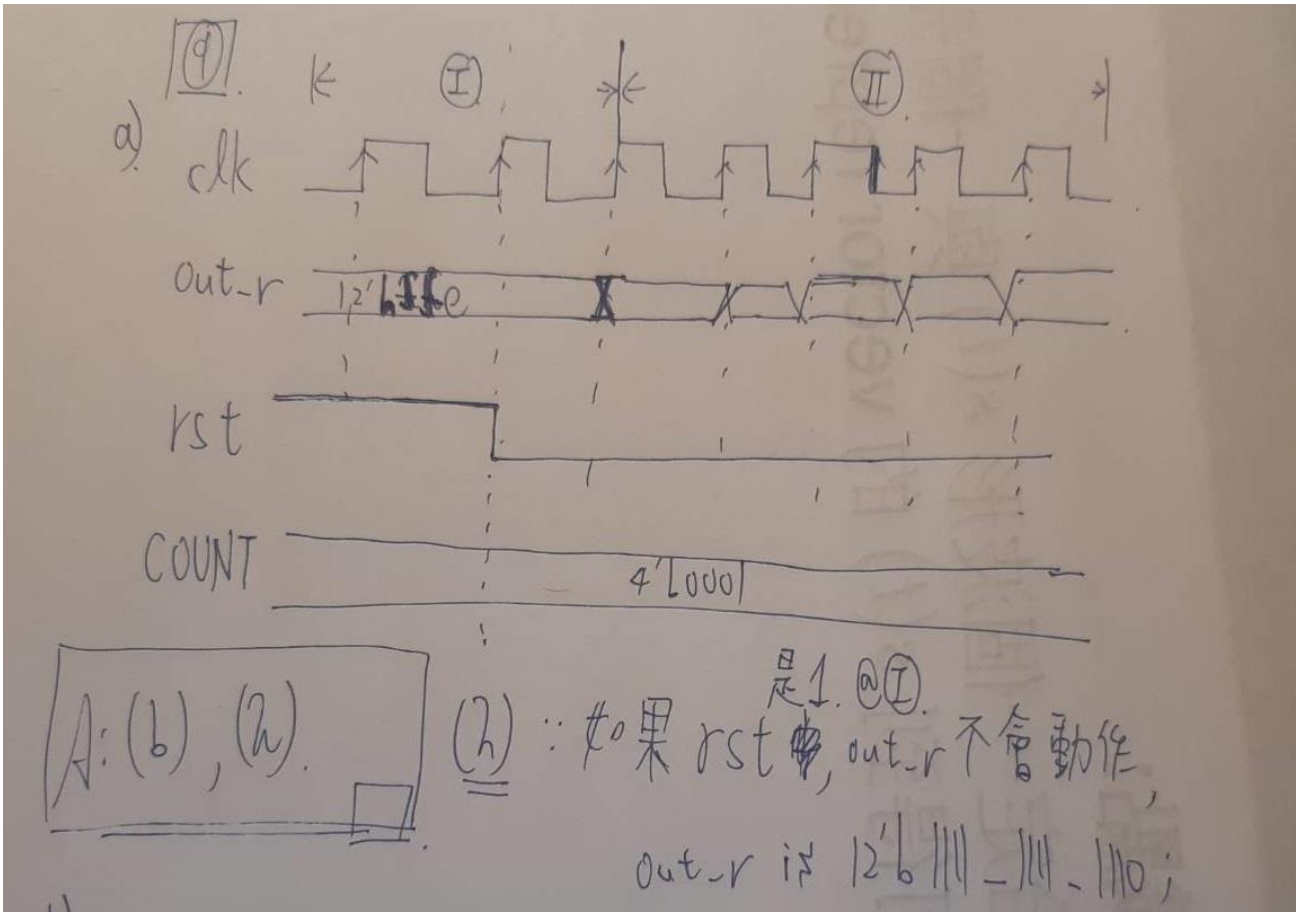
b) No

c) Yes

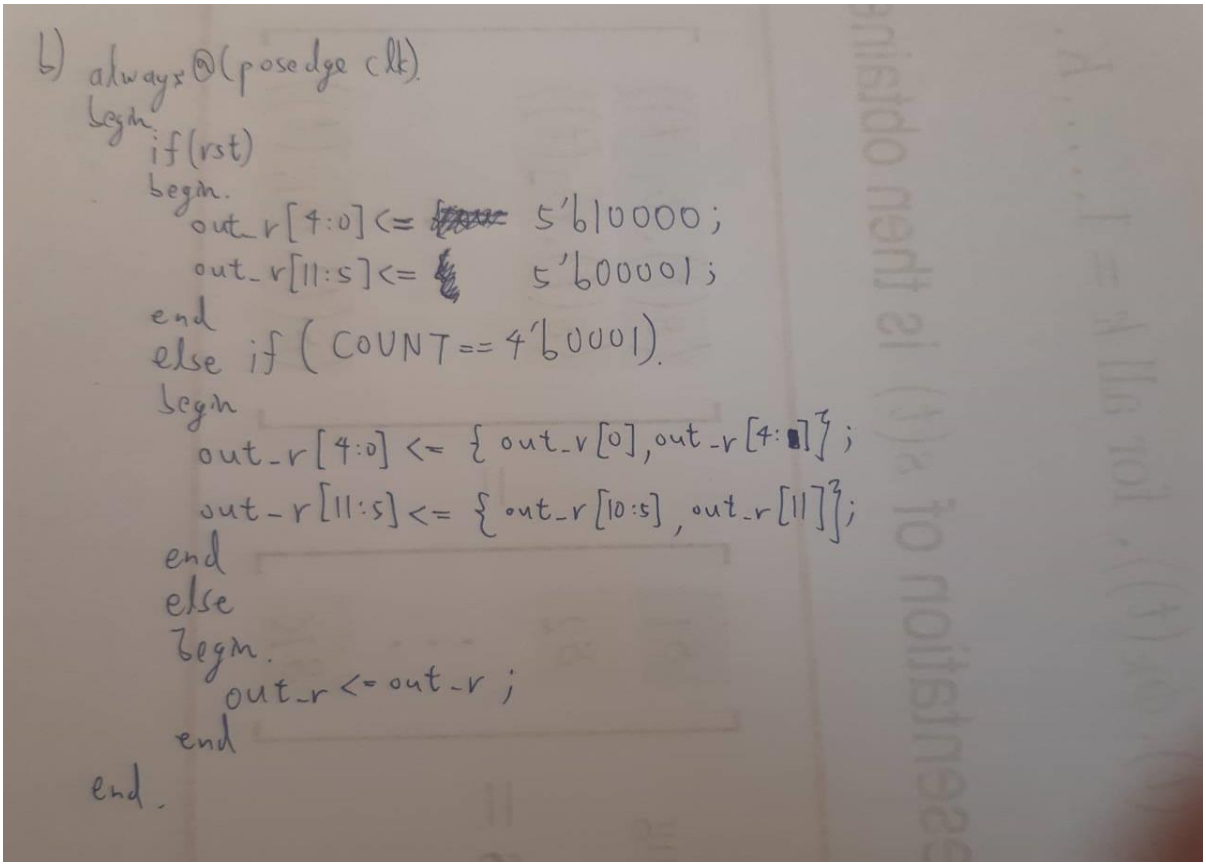
d). Yes.

e). Yes.

(9)-a



9-b



```
b) always @(posedge clk)
begin
    if(rst)
    begin
      out_r[4:0] <= 5'b10000;
      out_r[11:5] <= 5'b00001;
    end
    else if ( COUNT == 4'b0001)
    begin
      out_r[4:0] <= {out_r[0], out_r[4:1]};
      out_r[11:5] <= {out_r[10:5], out_r[11]};
    end
    else
    begin
      out_r <= out_r;
    end
end
```