2023 FPGA Final Exercise

Topic：Polish notation

I. Introduction

Polish Notation in the data structure is a method of expressing mathematical, logical, and algebraic equations universally. This notation is used by the compiler to evaluate mathematical equations based on their order of operations. When parsing mathematical expressions, three types of notations are commonly used : Infix Notation, Prefix Notation, and Postfix Notation. Here is some example in the table.

Infix Expression	Prefix Expression (normal Polish notation)	Postfix Expression (reverse Polish notation)
(A＋B)＊C	＊＋ABC	AB＋C＊
A＊B＋C＊D	＋＊AB＊CD	AB＊CD＊＋
A－(B＋C)－D	－－A＋BCD	ABC＋－D－

As you can see in the table, we do not need to use Parentheses in prefix and postfix expression. Take (A＋B)＊C for example. In prefix expression, the addition will do before multiplication because its operand priority is higher.

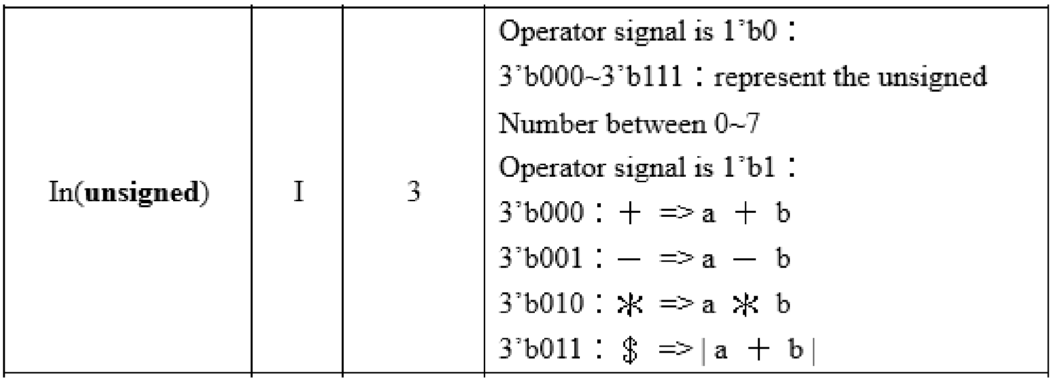
II. Lab Introduction

In this lab, you have to calculate the answers in different modes. Each mode will get a different length of the "in_valid" signal.

If the “mode” signal is 0 or 1, the “in_valid” signal will be randomly chosen between 6, 9, or 12 cycles.

If the “mode” signal is 2 or 3, the “in_valid” signal will be randomly chosen between 5, 7, or 9 cycles.

When the “in_valid” signal is high, TESTBED will send the 3－bit signal “in” and 1－bit signal “operator”. The 1－bit “operator” signal will decide whether the “in” signal is an operand or operator (if it’s an operand, it will not appear in 3’b100~3’b111).



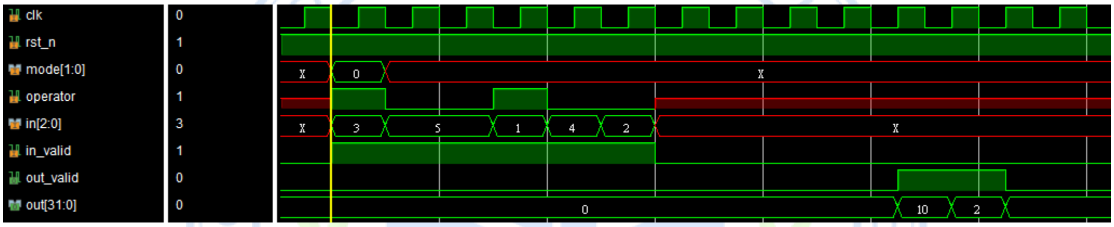
In(unsigned)	I	3	Operator signal is 1’b0： 3’b000~3’b111：represent the unsigned Number between 0~7 Operator signal is 1’b1： 3’b000：＋ => a ＋ b 3’b001：－ => a － b 3’b010：＊ => a ＊ b 3’b011：$ => |a ＋ b|

The two－bit “mode” signal will be given in the first cycle while “in_valid” is high, then turn back to unknown. And the following description will tell you what should do in the different modes.

case 1

If the “**mode**” signal is 2’d0, prefix notation will be chosen. Each **three continuous “in”** signals will group into a prefix expression. And you have to calculate each group, then based on the answer, sort it in **descending order(big to small)**.

For example, when “in_valid” is high for 6 cycles, the “mode” signal is 2’d0, the “in” signal is 3’d3, 3’d5, 3’d5, 3’d1, 3’d4, 3’d2 for the continuous six cycles, and the “operator” signal is 1’b1, 1’b0, 1’b0, 1’b1, 1’b0, 1’b0 for the continuous six cycles. Then it means that it’s prefix expression_1 ” $ 55” and expression_2 “－42”. After calculation, you will get ans_1：”10”, and ans_2：”2”. Before you raise the “out_valid” signal, you should sort the answer in descending order. The “**out**” signal will be 32’d10, and 32’d2 in continuous 2 cycles, and the “**out_valid**” signal should raise 2 cycles.



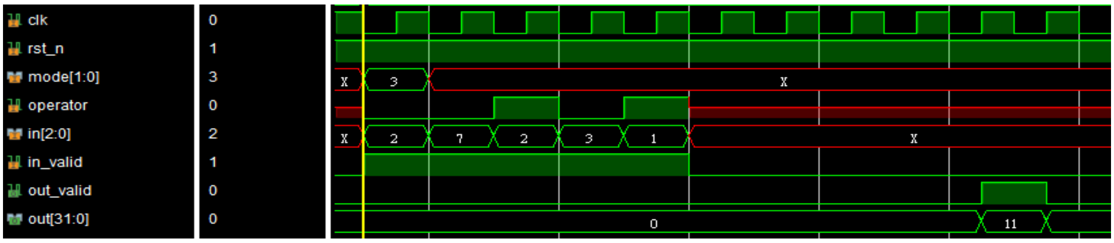
case 2

If the “**mode**” signal is 2’d1, postfix notation will be chosen. Each **three continuous “in”** signal will group into a postfix expression. And you have to calculate **each group**, then based on the answer, sort it in **ascending order(small to big)**.

case 3

If the “**mode**” signal is 2’d2, prefix notation will be chosen. And you have to calculate it and get the only solution.

case 4



If the “**mode**” signal is 2’d3, postfix notation will be chosen. And you have to calculate it and get the only solution.

For example, when “**in_valid**” is high for 5 cycles, the “**mode**” signal is **2’d3,** the “**in**” signal is 3’d2, 3’d7, 3’d2, 3’d3, 3’d1 for the continuous five cycles, and the “**operator**” signal is 1’b0, 1’b0, 1’b1, 1’b0, 1’b1 for the continuous five cycles. Then it means that it’s postfix expression “**27＊3－**”. After calculation, you will get the answer “11”. The “**out**” signal will be 32’d11 in a cycle, so as the “**out_valid**” signal.

III. I/O Description

Signal Name	I/O	Width	Simple Description
clk	I	1	Posedge triggered Clock
Rst_n	I	1	Asynchronous active－low reset
mode	I	2	0：prefix and sorting in **descending order.** 1：postfix and sorting in **ascending order** 2：normal Polish notation(NPN) 3：reverse polish natation(RPN)
Operator	I	1	1’b0：**in** is an operand 1’b1：**in** is an operator
In(**unsigned**)	I	3	Operator signal is 1’b0： 3’b000~3’b111：represent the unsigned Number between 0~7 Operator signal is 1’b1： 3’b000：＋ => a ＋ b 3’b001：－ => a － b 3’b010：＊ => a ＊ b 3’b011：$ => | a ＋ b |
in_valid	I	1	High when in is valid.
Out_valid	O	1	High when **out** is valid.
Out(**signed**)	O	32	The answer of output after calculation

IV. Specifications

1. All output signals should be reset after the “**rst_n**” signal is asserted.
2. The “**out_valid**” signal should not be high when “**in_valid**” signal is high.
3. The “**out**” signal should be 0 when your “**out_valid**” signal is pulled down.
4. Each of the pattern execution latency is limited in 1000 cycles.
5. When the “**mode**” signal is “0,1”, the cycles of the “**out_valid**” signal should be one－third of the “**in_valid**” signal. Otherwise, the “**out_valid**” signal can only raise one cycle.
6. While the “**out_valid**” signal raise high, TESBED will check if your “**out**” signal match the expectation or not. If true, nothing will happen before you pass the pattern. If false, error msg will tell you the expect out value. At the end of the msg will tell you the total amount of error. This will depend your grade.

7. Do not revise the don’t touch TESTBED code, or you may fail this lab.
8. Please upload the file to ilearning 3.0 with the following format："PN studentID.v". If the file is not submitted in this format, the score will be discounted by 30%.

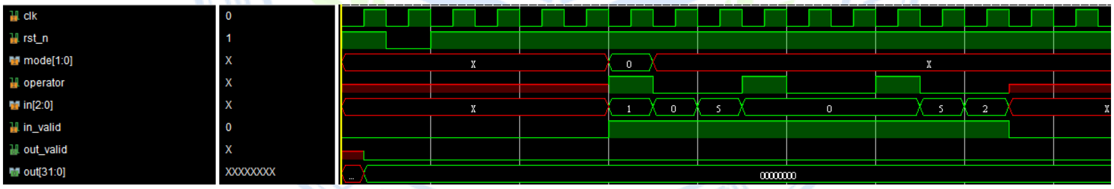
V. Grading Policy

- Violate the Specifications 1~5……………………………………………………0%
- If the total amount of error is less than 498…………………………………...30%
- If the total amount of error less than 200 ………………………….…………40%
- If the total amount of error less than 50………………………………………50%
- If you pass the first state task………………………………………………70%
- Without any error……………………………………………………………100%

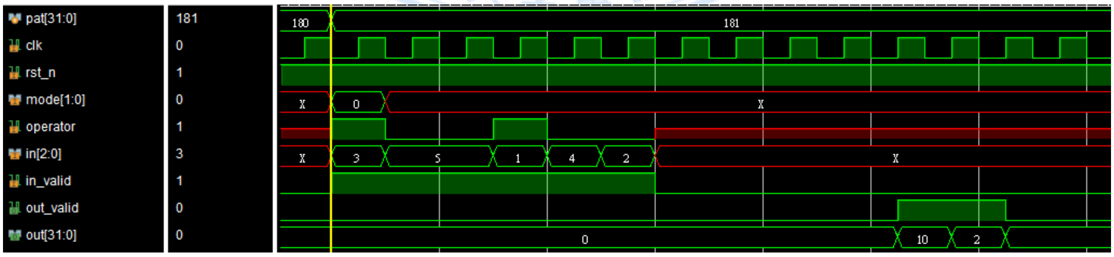
If you can write some documents about how you constructed this lab or what algorithm you choose, you will get another bonus point. For example, you choose bubble sort as your sorting algorithm because it’s more hardware friendly. For another example, you design a 4－state FSM due to the reason…. The document can only write one page of A4 in PDF format. Please upload to ilearning 3.0 with the following format："Final_studentID.pdf ".

VI. Wave Demonstration

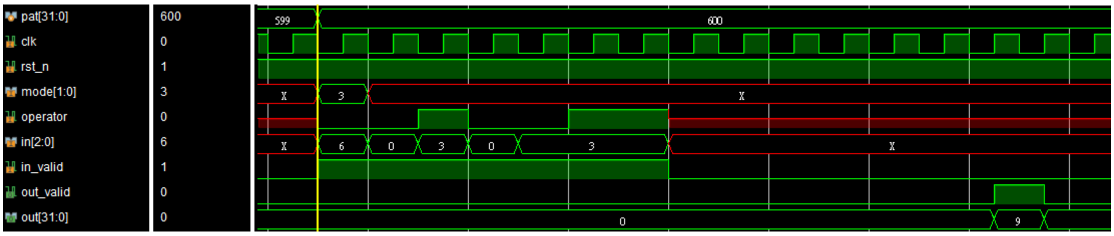
Input wave



Pattern 181



Pattern 600


pat[31:0]
clk
rst_n
mode[1:0]
operator
in[2:0]
in_valid
out_valid
out[31:0]
600
0
1
3
0
6
1
0
0
599
600
X
3
X
X
6
0
3
0
3
X
0
9