國立中興大學
National Chung Hsing University

FPGA Introduce

2022.03.30

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主講人：王星耀

Outline

國立中興大學
National Chung Hsing University

- EGO1
- 元件及腳位對應
- Vivado 2018.2

Outline

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EGO1

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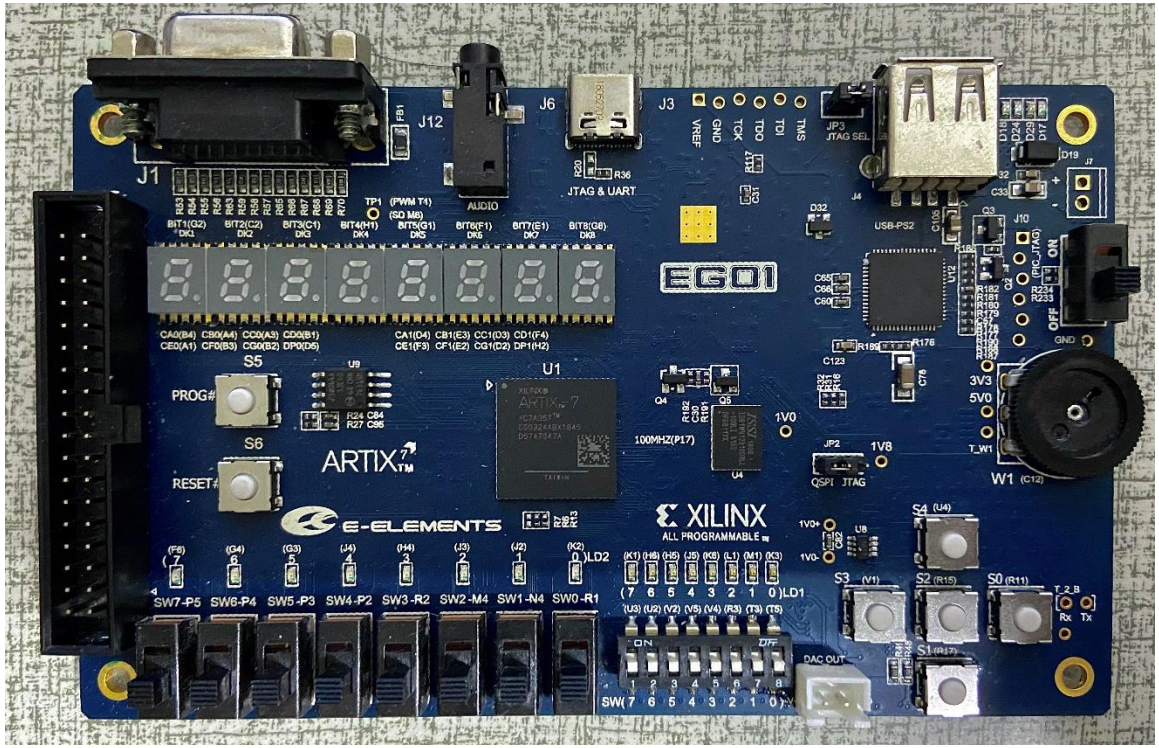
- EGO1是依元素科技基於 Xilinx Artix-7 FPGA研發的可攜式數模混和基礎教學平台。EGO-XA7配備的FPGA具有大容量高性能等特點，能實現較複雜的數位邏輯設計。



EGO1

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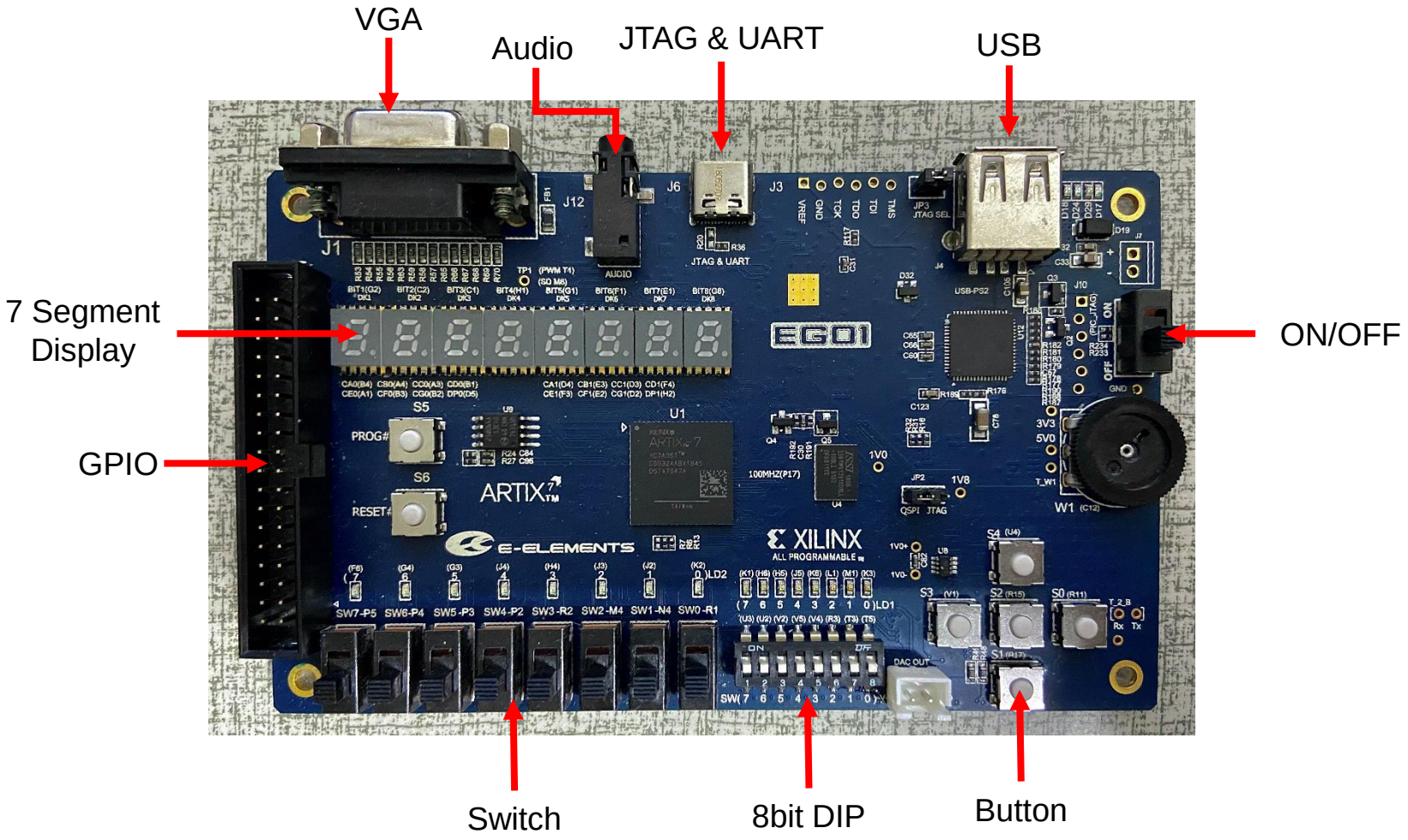

EGO1

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E-ELEMENTS

EGO1 User Manual

	Part Number	XC7A12T	XC7A15T	XC7A25T	XC7A35T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280
	Slices	2,000	2,600	3,650	5,200
	CLB Flip-Flops	16,000	20,800	29,200	41,600
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50
	Total Block RAM (Kb)	720	900	1,620	1,800
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5
I/O Resources	Maximum Single-Ended I/O	150	250	150	250
	Maximum Differential I/O Pairs	72	120	72	120
Embedded Hard IP Resources	DSP Slices	40	45	80	90
	PCIe® Gen2[1]	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]	2	4	4	4
Speed Grades	Commercial	-1, -2	-1, -2	-1, -2	-1, -2
	Extended	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L

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元件及腳位對應

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- EGO-XA7 搭載一個100MHz的時鐘晶片，輸出的時鐘訊號直接與FPGA全域時鐘輸入接腳(P17)相連。

名稱	電路圖訊號	FPGA IO PIN
時鐘接腳	SYS_CLK	P17

元件及腳位對應

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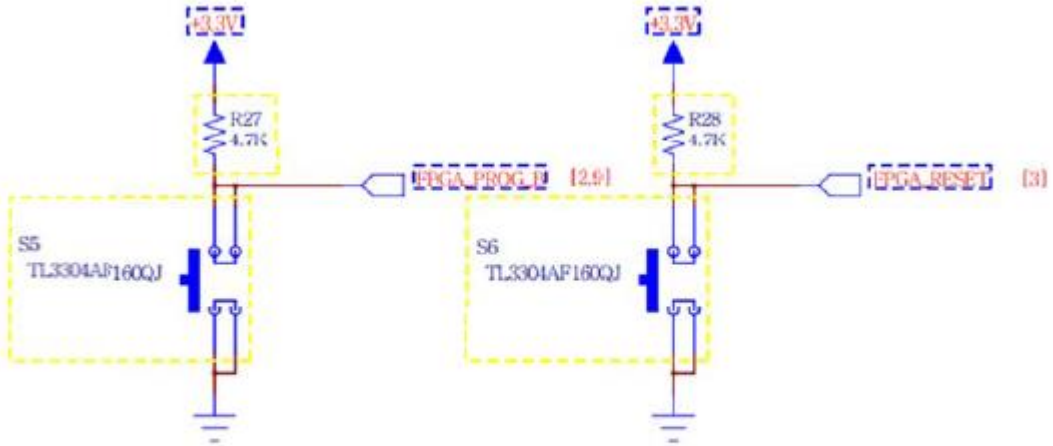
- 專用按鍵
- PROG：擦除FPGA配置
- RESET：邏輯重置



名稱	電路圖訊號	FPGA IO PIN
重置接腳	FPGA_RESET	P15

元件及腳位對應

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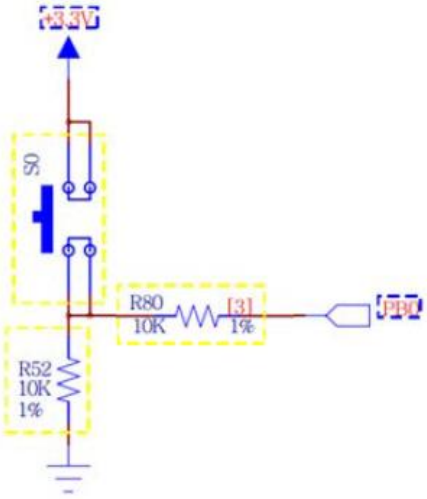
- 通用按鍵(S0 ~ S4)
- 預設為低電位，按鍵按下時輸出高電位



名稱	電路圖訊號	FPGA IO PIN
S0	PB0	R11
S1	PB1	R17
S2	PB2	R15
S3	PB3	V1
S4	PB4	U4

元件及腳位對應

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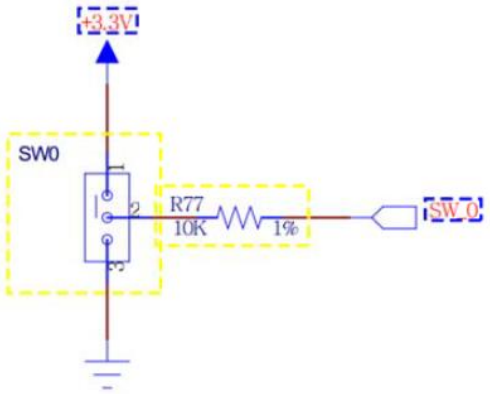
- 開關(Switch)
- 預設為低電位，向上撥動輸出高電位



名稱	電路圖訊號	FPGA IO PIN
SW0	SW_0	P5
SW1	SW_1	P4
SW2	SW_2	P3
SW3	SW_3	P2
SW4	SW_4	R2
SW5	SW_5	M4
SW6	SW_6	N4
SW7	SW_7	R1

元件及腳位對應

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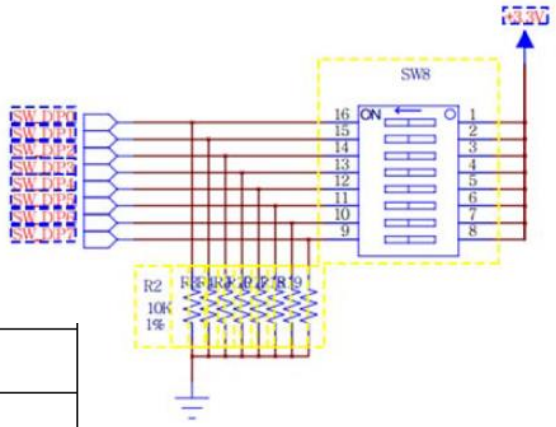
- 8bit 指撥開關(DIP Switch)
- 預設為低電位，向上撥動輸出高電位



SW8	SW_DIP0	U3
	SW_DIP1	U2
	SW_DIP2	V2
	SW_DIP3	V5
	SW_DIP4	V4
	SW_DIP5	R3
	SW_DIP6	T3
	SW_DIP7	T5

元件及腳位對應

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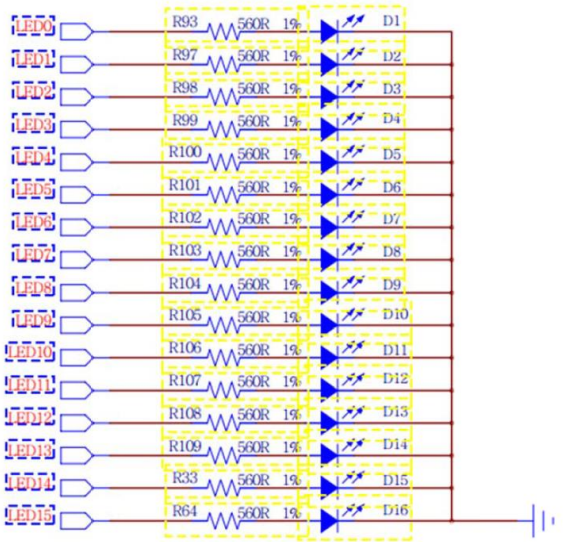
- LED燈
- 輸出高電位時被點亮



名稱	電路圖訊號	FPGA IO PIN	顏色
D0	LED0	F6	Green
D1	LED1	G4	Green
D2	LED2	G3	Green
D3	LED3	J4	Green
D4	LED4	H4	Green
D5	LED5	J3	Green
D6	LED6	J2	Green
D7	LED7	K2	Green
D8	LED8	K1	Green
D9	LED9	H6	Green
D10	LED10	H5	Green
D11	LED11	J5	Green
D12	LED12	K6	Green
D13	LED13	L1	Green
D14	LED14	M1	Green
D15	LED15	K3	Green

元件及腳位對應

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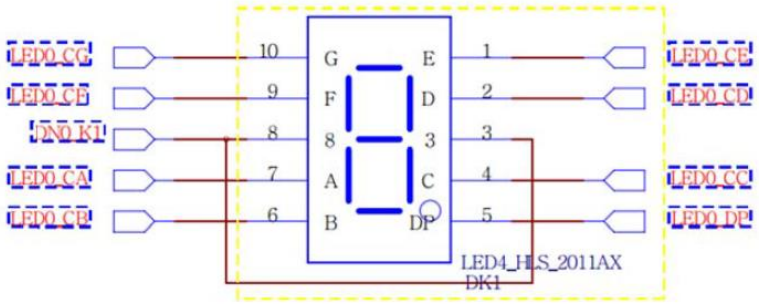
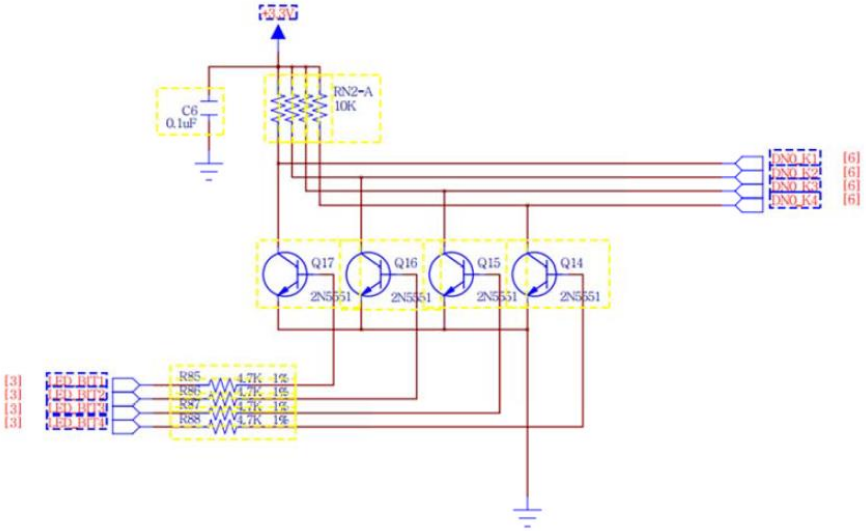
- 七段顯示器(7 Segment Display)
- 顯示器為共陰極顯示器，即公共極輸入低電位。
- 操控多顯示器需片選信號及段選信號。片選信號及段選信號須皆為高電位，顯示器上對應位置才可以被點亮。





元件及腳位對應

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- 七段顯示器(7 Segment Display)

段選信號

名稱	電路圖訊號	FPGA IO PIN
A0	LED0_CA	B4
B0	LED0_CB	A4
C0	LED0_CC	A3
D0	LED0_CD	B1
E0	LED0_CE	A1
F0	LED0_CF	B3
G0	LED0_CG	B2
DP0	LED0_DP	D5
A1	LED1_CA	D4
B1	LED1_CB	E3
C1	LED1_CC	D3
D1	LED1_CD	F4
E1	LED1_CE	F3
F1	LED1_CF	E2
G1	LED1_CG	D2
DP1	LED1_DP	H2

片選信號

DN0_K1	LED_BIT1	G2
DN0_K2	LED_BIT2	C2
DN0_K3	LED_BIT3	C1
DN0_K4	LED_BIT4	H1
DN1_K1	LED_BIT5	G1
DN1_K2	LED_BIT6	F1
DN1_K3	LED_BIT7	E1
DN1_K4	LED_BIT8	G6

元件及腳位對應

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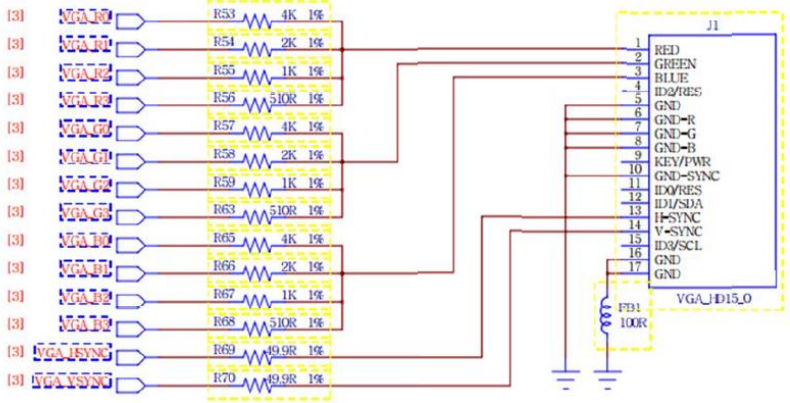
- VGA介面
- EGO-XA7上的VGA介面通過14位元信號線與FPGA連接，紅、綠、藍三個顏色信號各占4位，另外還包括水平同步和垂直同步信號。

名稱	電路圖訊號	FPGA IO PIN
RED	VGA_R0	F5
	VGA_R1	C6
	VGA_R2	C5
	VGA_R3	B7
GREEN	VGA_G0	B6
	VGA_G1	A6
	VGA_G2	A5
	VGA_G3	D8
BLUE	VGA_B0	C7
	VGA_B1	E6
	VGA_B2	E5
	VGA_B3	E7
H-SYNC	VGA_HSYNC	D7
V-SYNC	VGA_VSYNC	C4



元件及腳位對應

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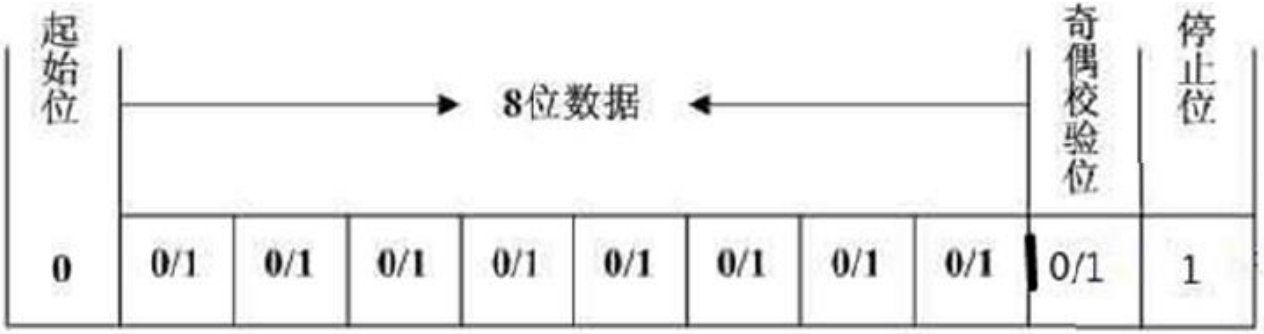
- UART
- 全稱為通用非同步收發器，是實現設備之間低速資料通信的標準協議。”非同步”指不需要額外的時鐘線進行資料的同步傳輸，雙方約定在同一個頻率下收發資料，此介面只需要兩條信號線(RXD、TXD)就可以完成資料的相互通信，接收盒發送可以同時進行，也就是全雙工。
- 收發的過程，在發送器閒置時間，資料線處於邏輯1狀態，當有資料要傳輸時，首先使資料線狀態為0，之後是8個資料位元、一位元校驗位、一位元停止位，停止位用於標示一幀的結束，接收過程亦類似。



元件及腳位對應

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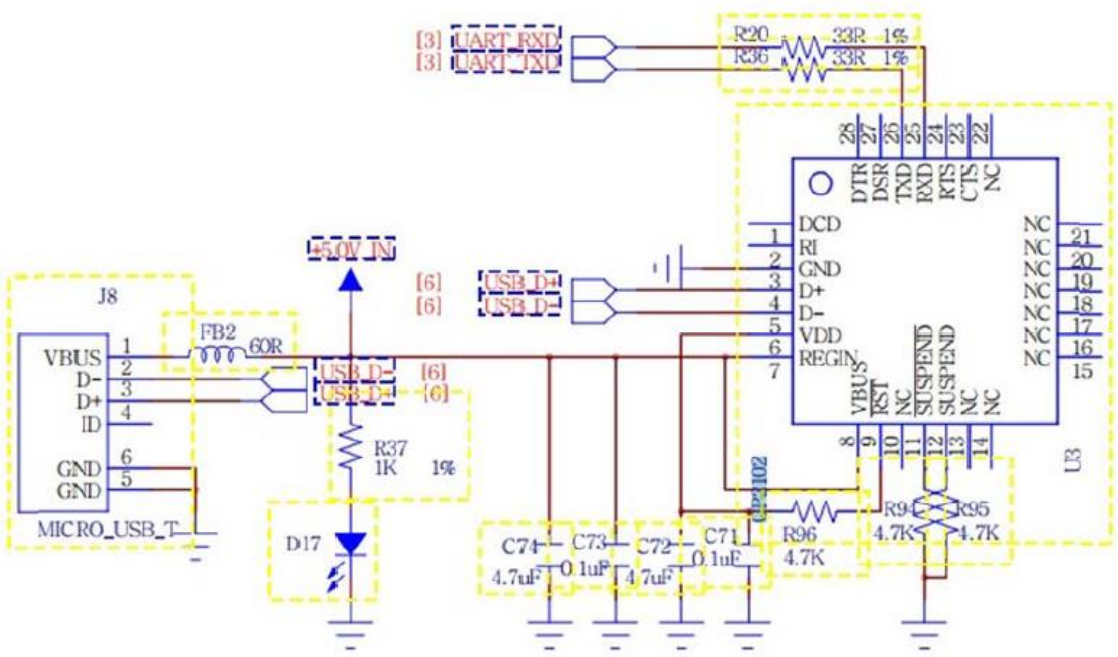
- UART



CP2102 標號	電路圖訊號	FPGA IO PIN
25	UART_RX	T4 （FPGA 串列埠發送
26	UART_TX	N5 （FPGA 串列埠接收

元件及腳位對應

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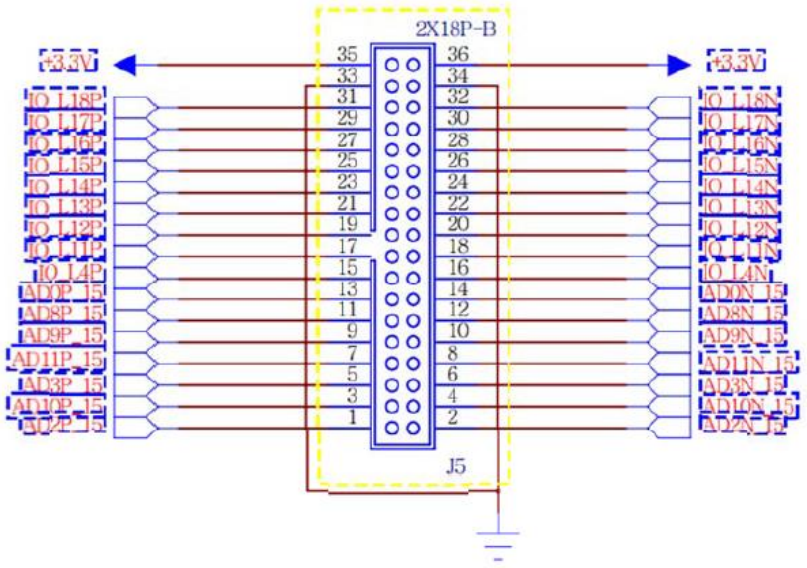
- GPIO (32雙向I/O)

2x18 標號	電路圖訊號	FPGA IO PIN
1	AD2P_15	B16
2	AD2N_15	A15
3	AD10P_15	A13
4	AD10N_15	B18
5	AD3P_15	F13
6	AD3N_15	B13
7	AD11P_15	D14
8	AD11N_15	B11
9	AD9P_15	E15
10	AD9N_15	D15
11	AD8P_15	H16
12	AD8N_15	F15
13	AD0P_15	H14
14	AD0N_15	E17
15	IO_L4P	K13
16	IO_L4N	H17
17	IO_L11P	B17
18	IO_L11N	A16
19	IO_L12P	A14
20	IO_L12N	A18
21	IO_L13P	F14
22	IO_L13N	B14
23	IO_L14P	C14
24	IO_L14N	A11
25	IO_L15P	E16
26	IO_L15N	C15
27	IO_L16P	G16



28	IO_L16N	F16
29	IO_L17P	G14
30	IO_L17N	D17
31	IO_L18P	J13
32	IO_L18N	G17

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Vivado 2018.2

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- 專案不能有中文路徑、不能以數字開頭
- 程式碼加入註解 (/*...*/ or //...)
- 在D槽以自己的學號創建新資料夾，之後全部上課資料都放裡面，避免公共電腦過於混亂

不要Copy同學的程式碼!!!

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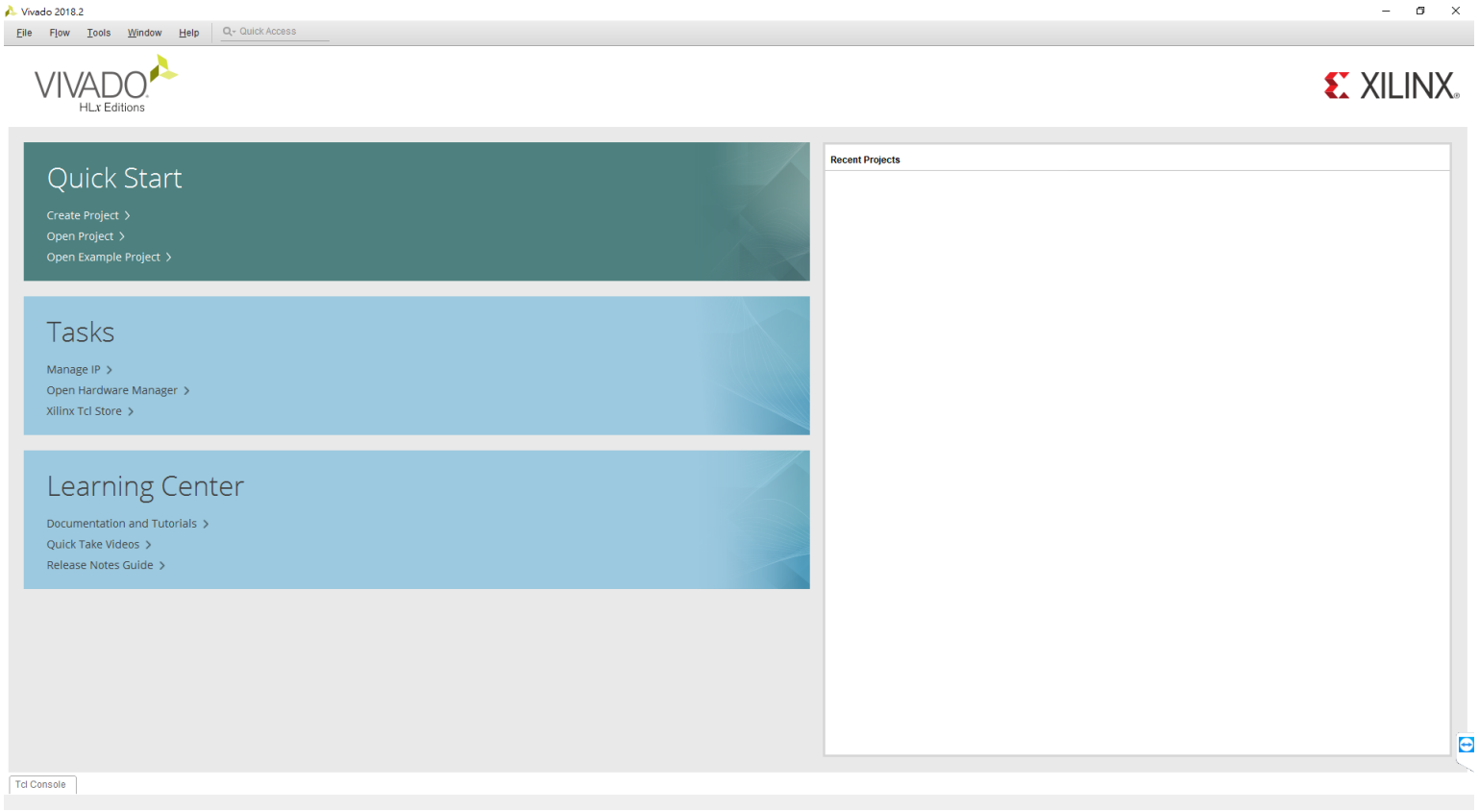
- 開啟 Vivado 2018.2



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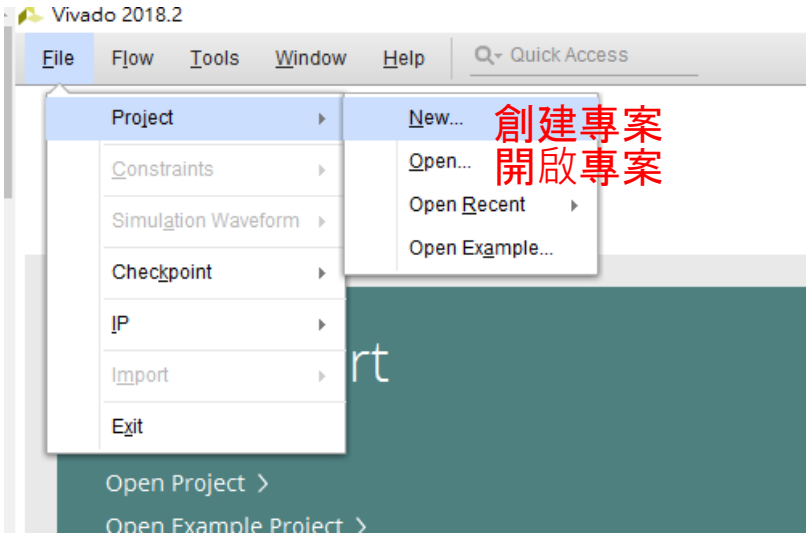
- 創建專案 / 開啟專案



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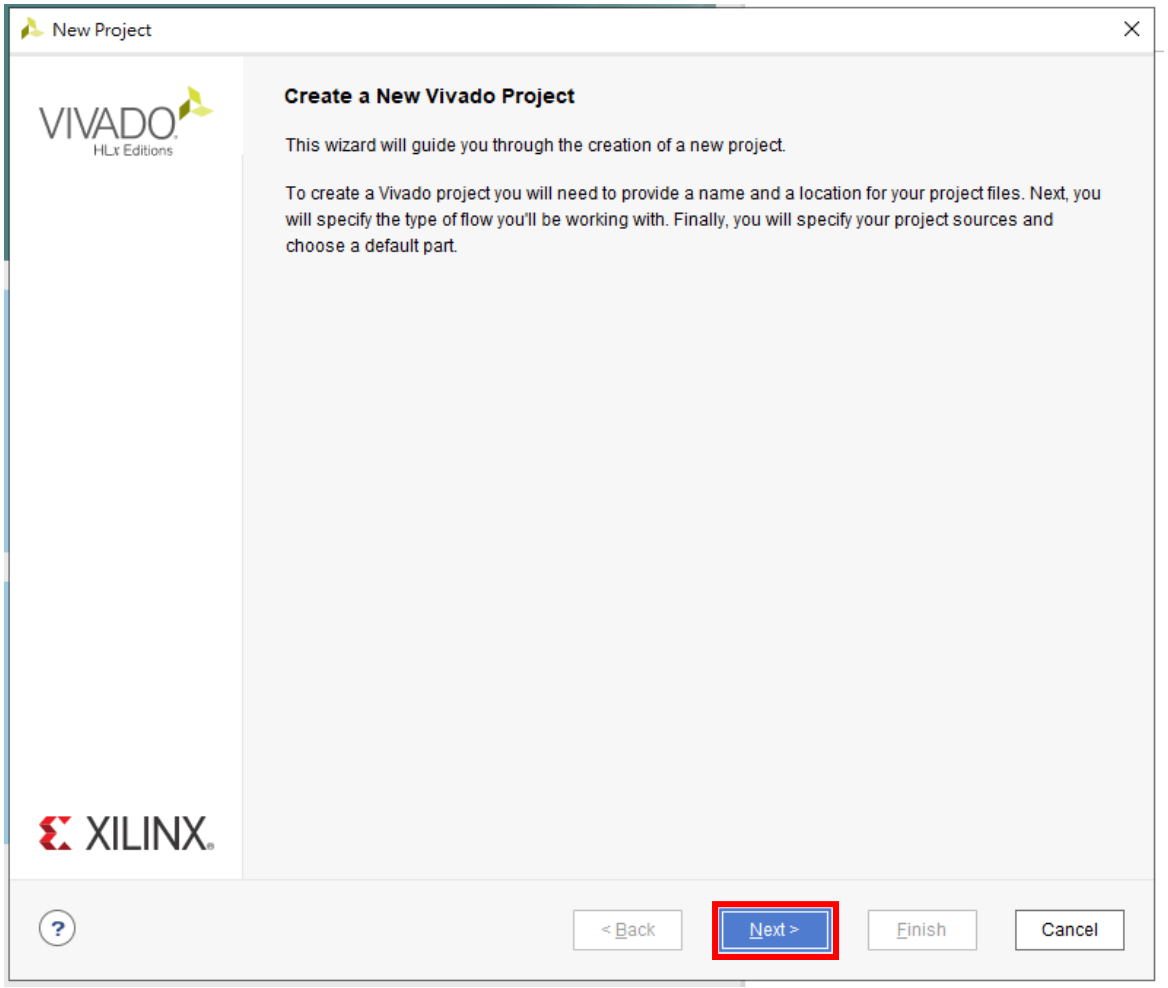
- 創新專案
- 無意義開場白
- 直接“Next”



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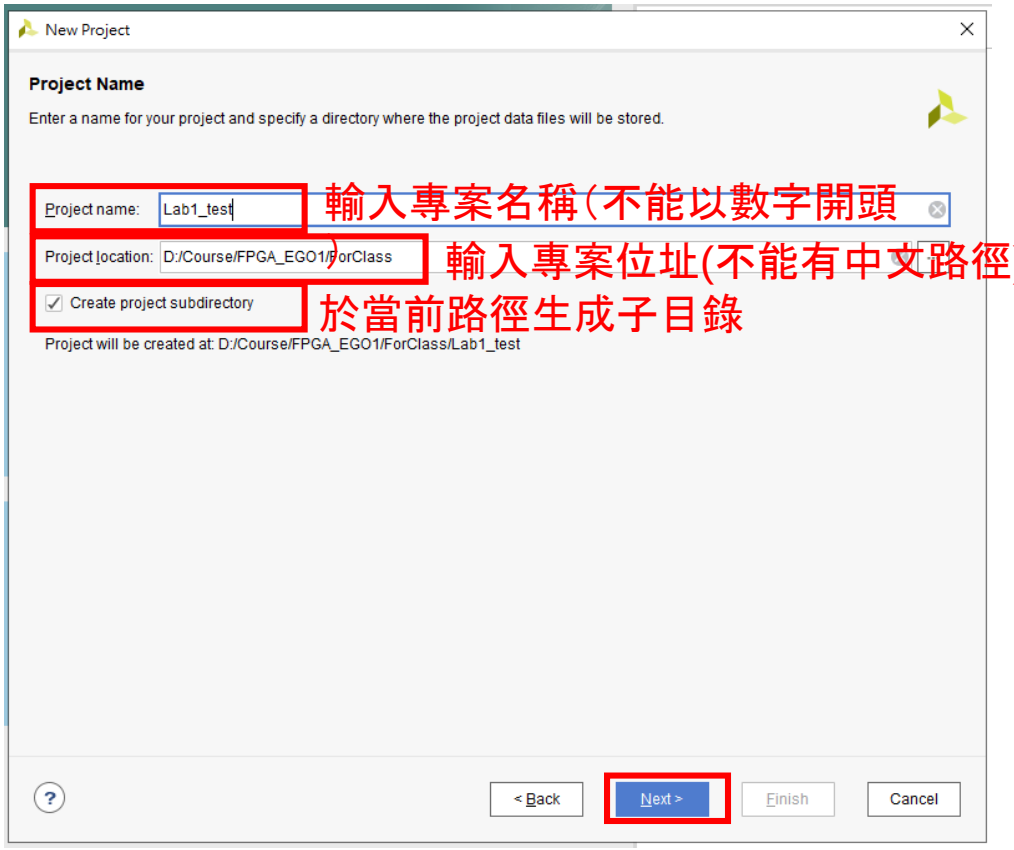
- 輸入專案名稱
- 輸入專案位址
- “Next”



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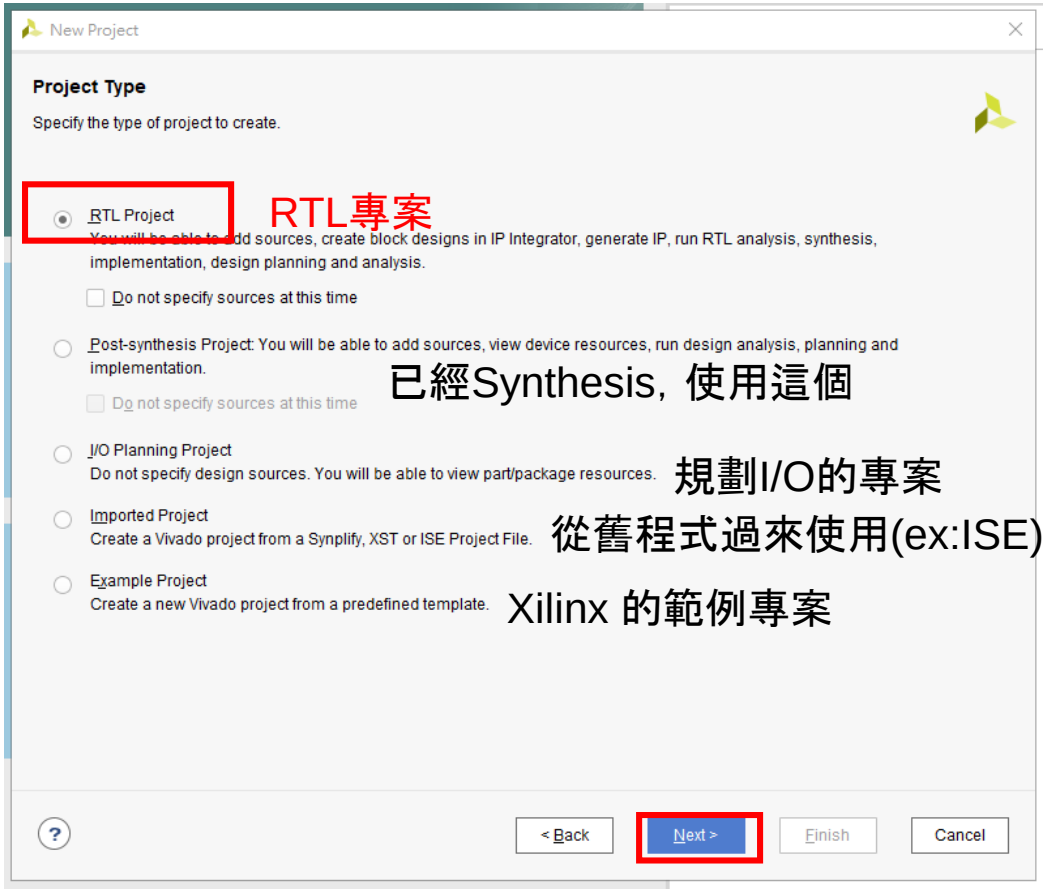
- 選 ”RTL Project”
- “Next”



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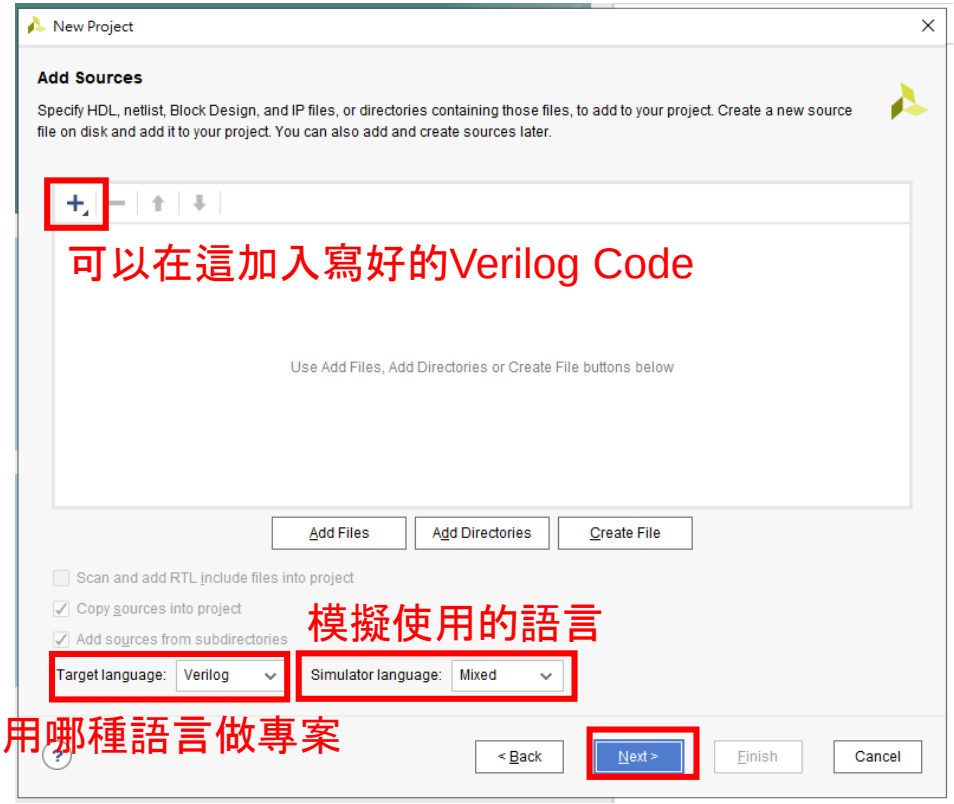
- 加入Design Source
- Target language 選Verilog ，Simulation 選Mixed
- “Next”



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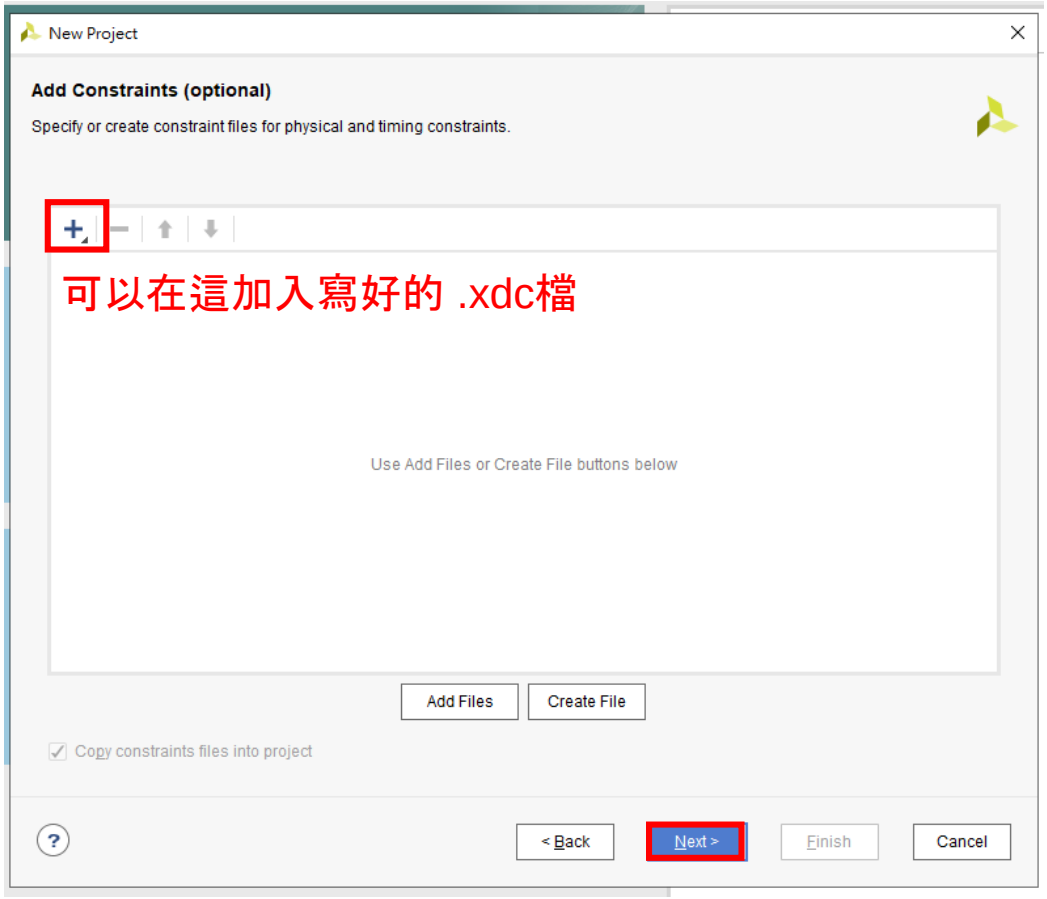
- 加入Constraints (.xdc檔)
- “Next”



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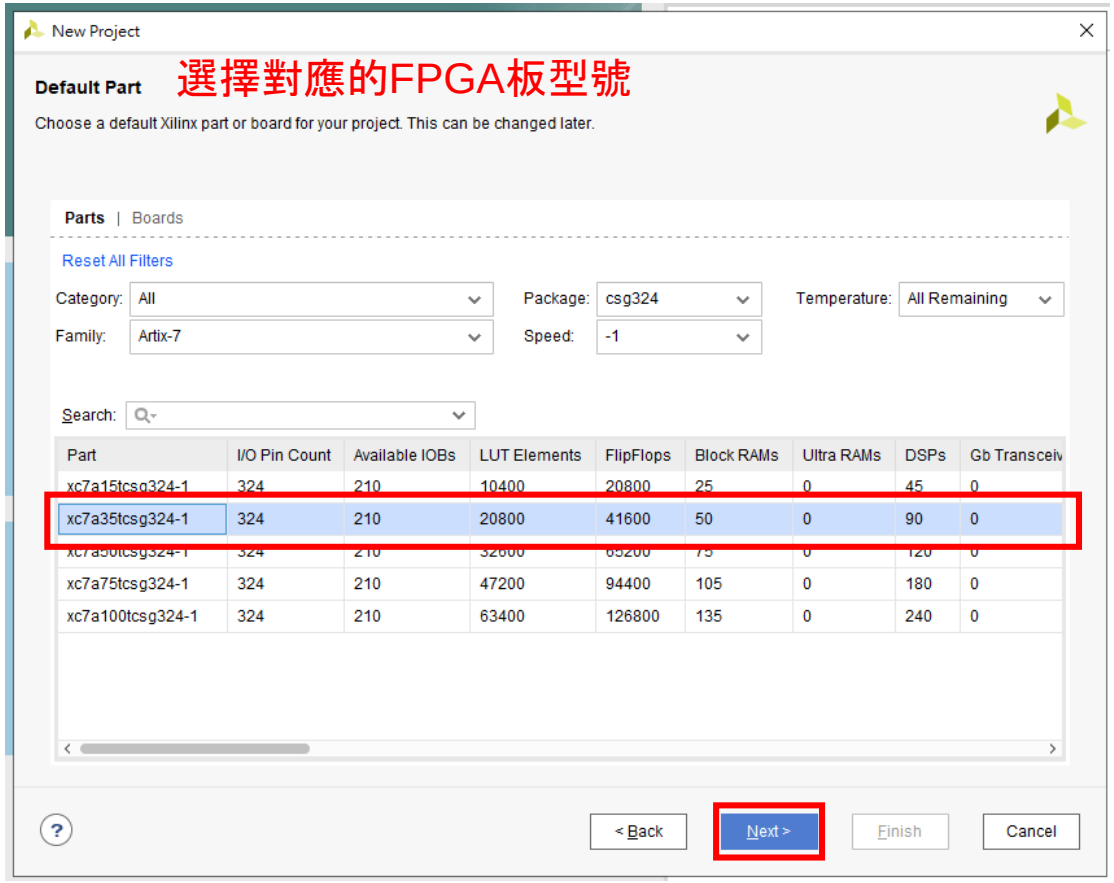
- 選擇對應的板子
- Family: Artix-7
- Package: csg324
- Speed: -1
- Part: xc7a35tcsg324-1
- “Next”



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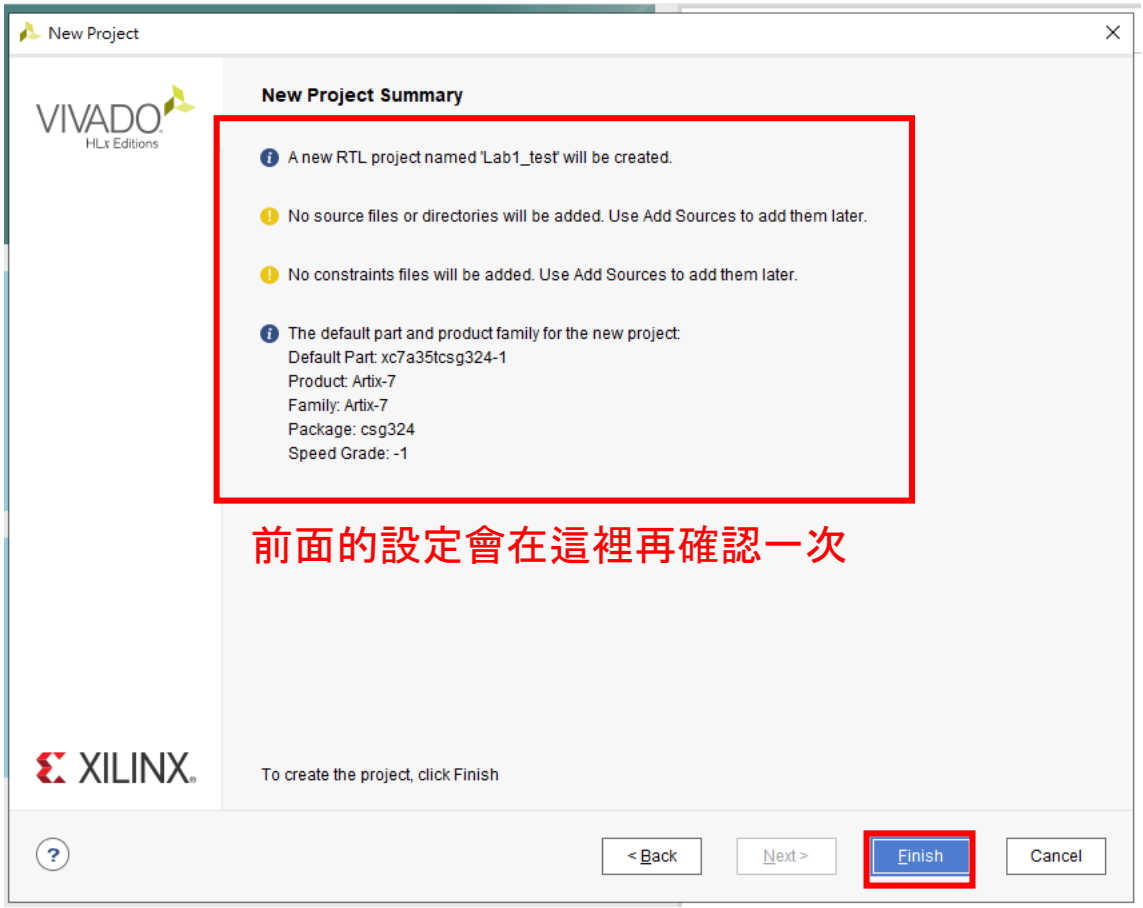
- 進行最後的確認
- “Finish”



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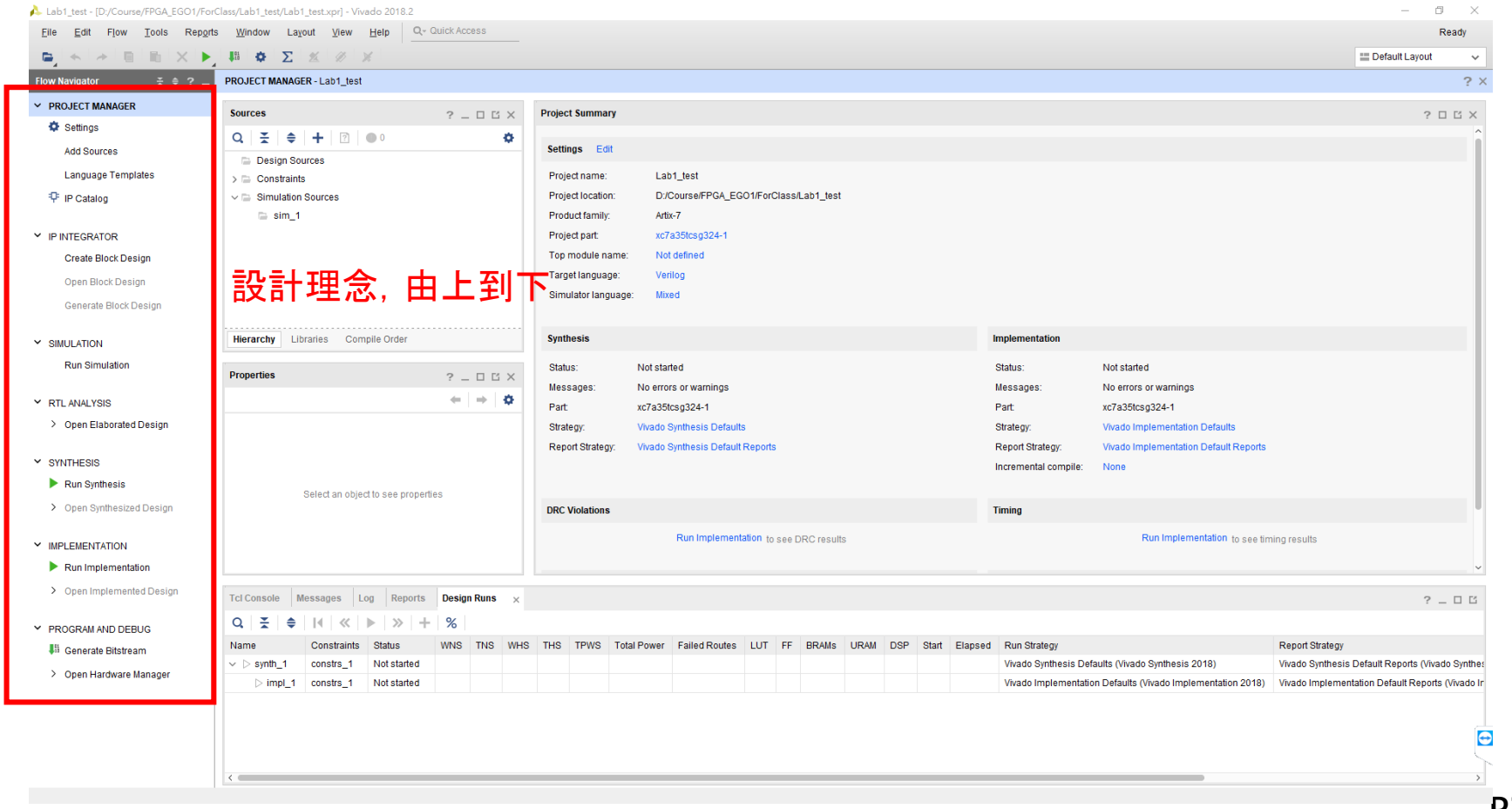
❖ 專案操作介面



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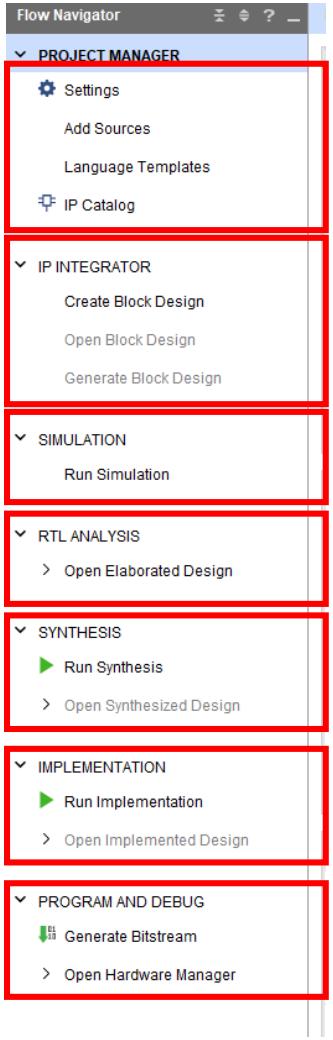
- 操作介面介紹



專案設定
新增資料(Verilog,Constraint)
資源範例
IP庫

使用圖形化介面創建專案

模擬 (驗證RTL邏輯是否正確)

RTL分析 (轉成Gate分析)

合成 (將RTL轉成Gate Level，並且設定腳位資訊)

實現 (將合成的結果 映射到FPGA板)

將實現的結果轉成板子看得懂的檔案(bitstream檔，.bit檔)
再將bitstream燒錄至FPGA板

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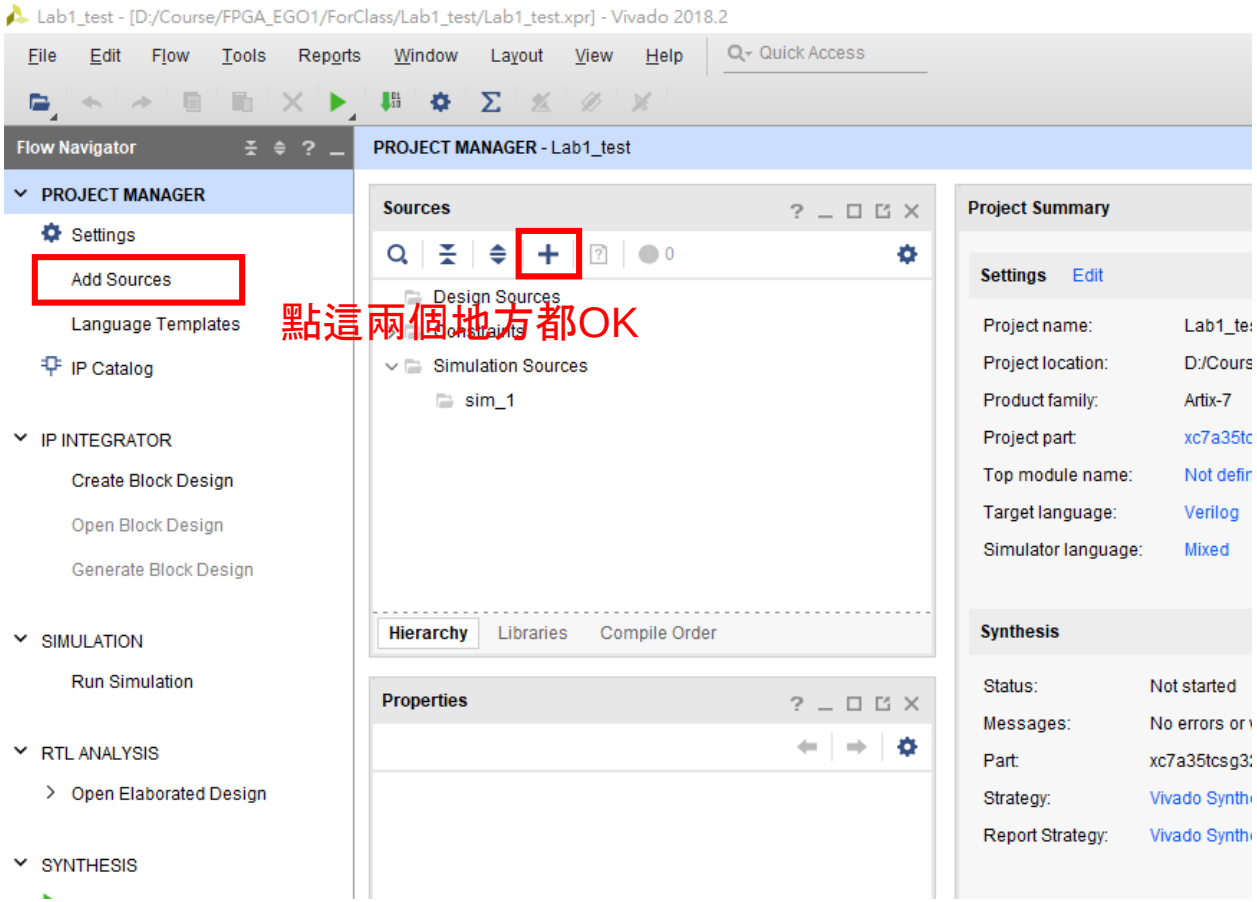
- 加入Design Source (Verilog code)



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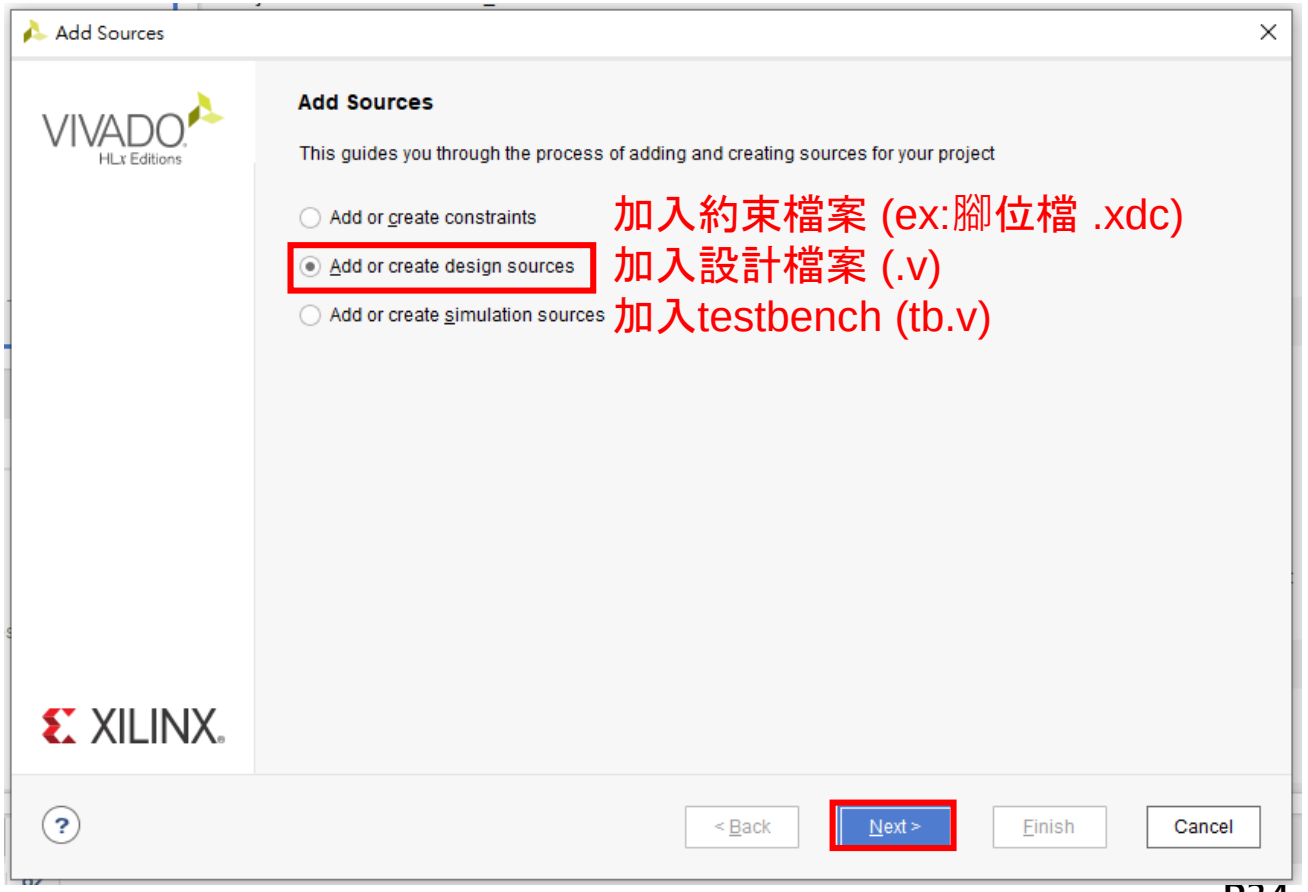
- 加入Design Source (Verilog code)
- “design source”
- “Next”



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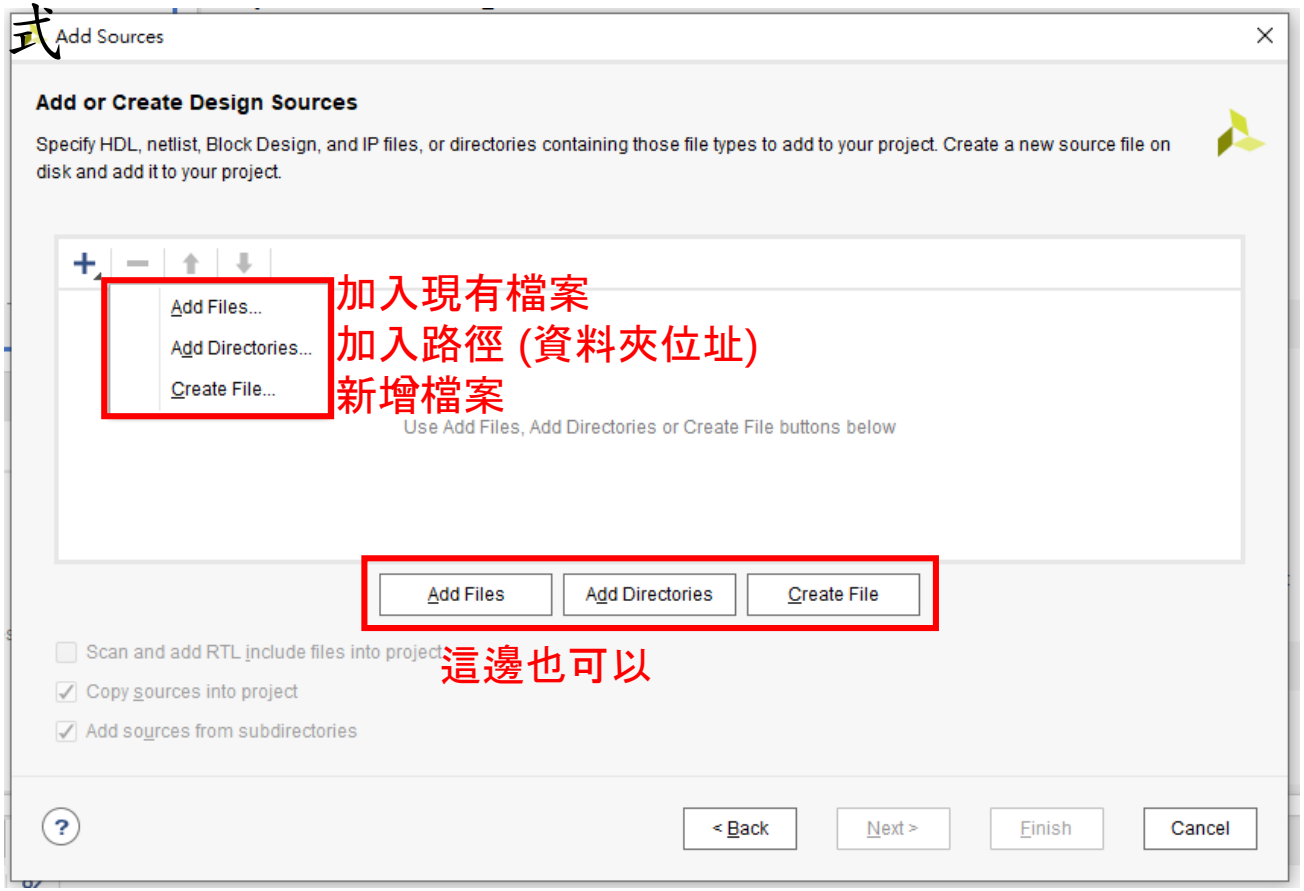
- 加入Design Source (Verilog code)
- 選擇加入資料方式
- “Add Files”



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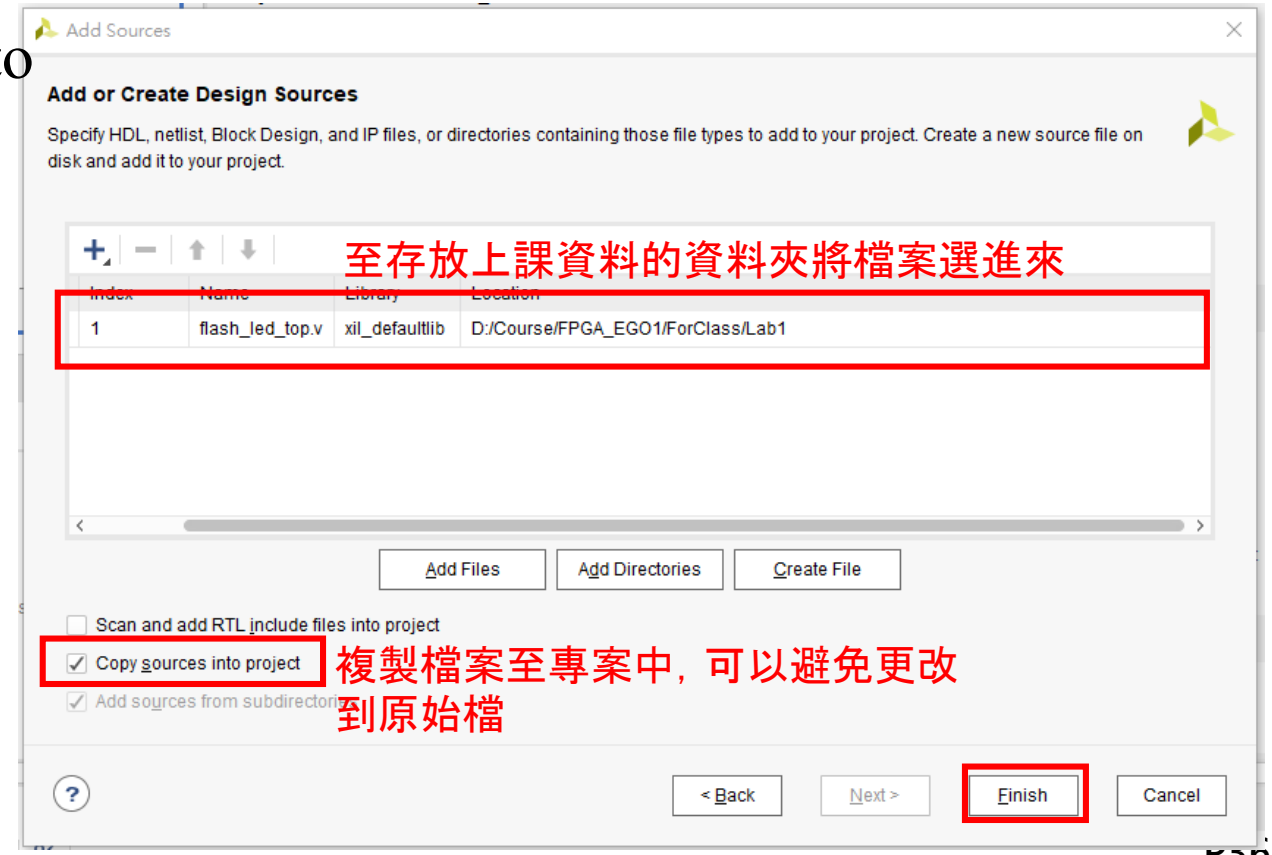
- 加入Design Source (Verilog code)
- 載入上課範例檔案
- “Copy source into project” 打勾
- “Finish”



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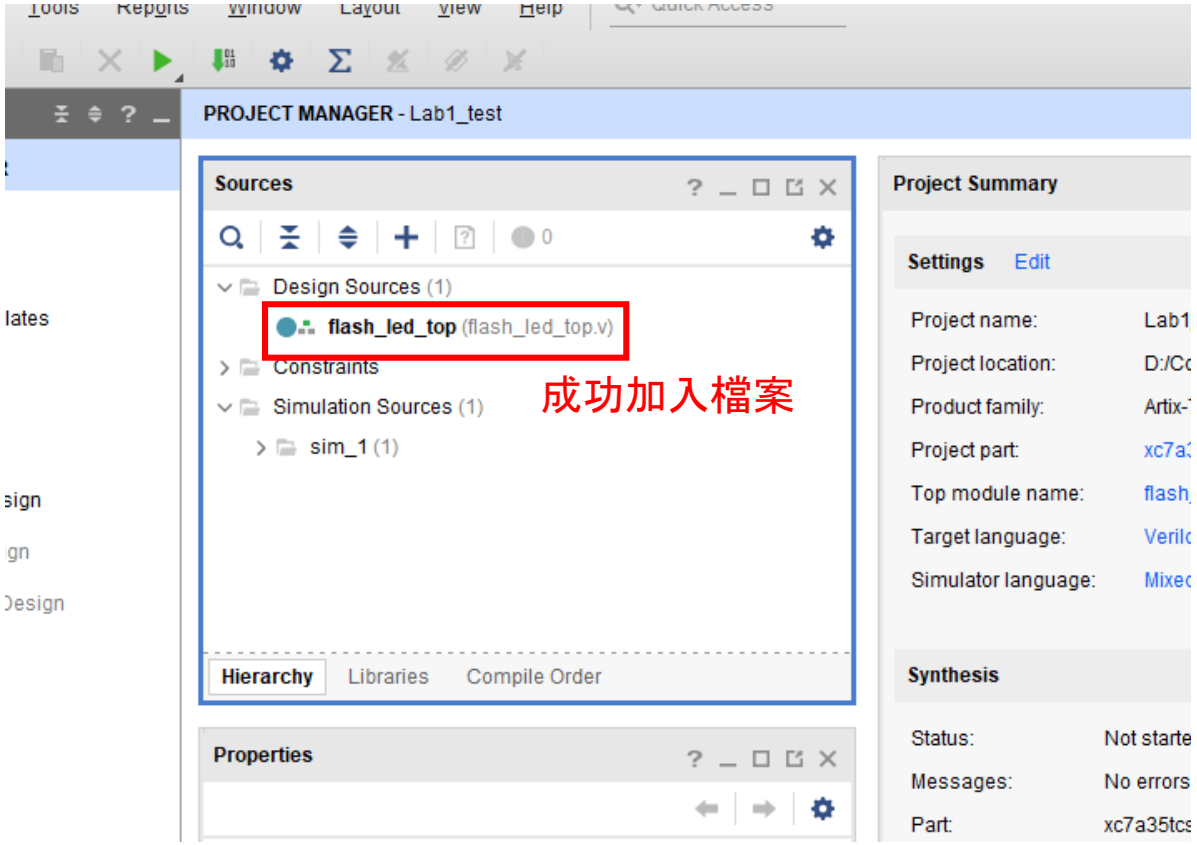
- 確定Verilog code 成功加入
- 連擊檔案開啟編輯



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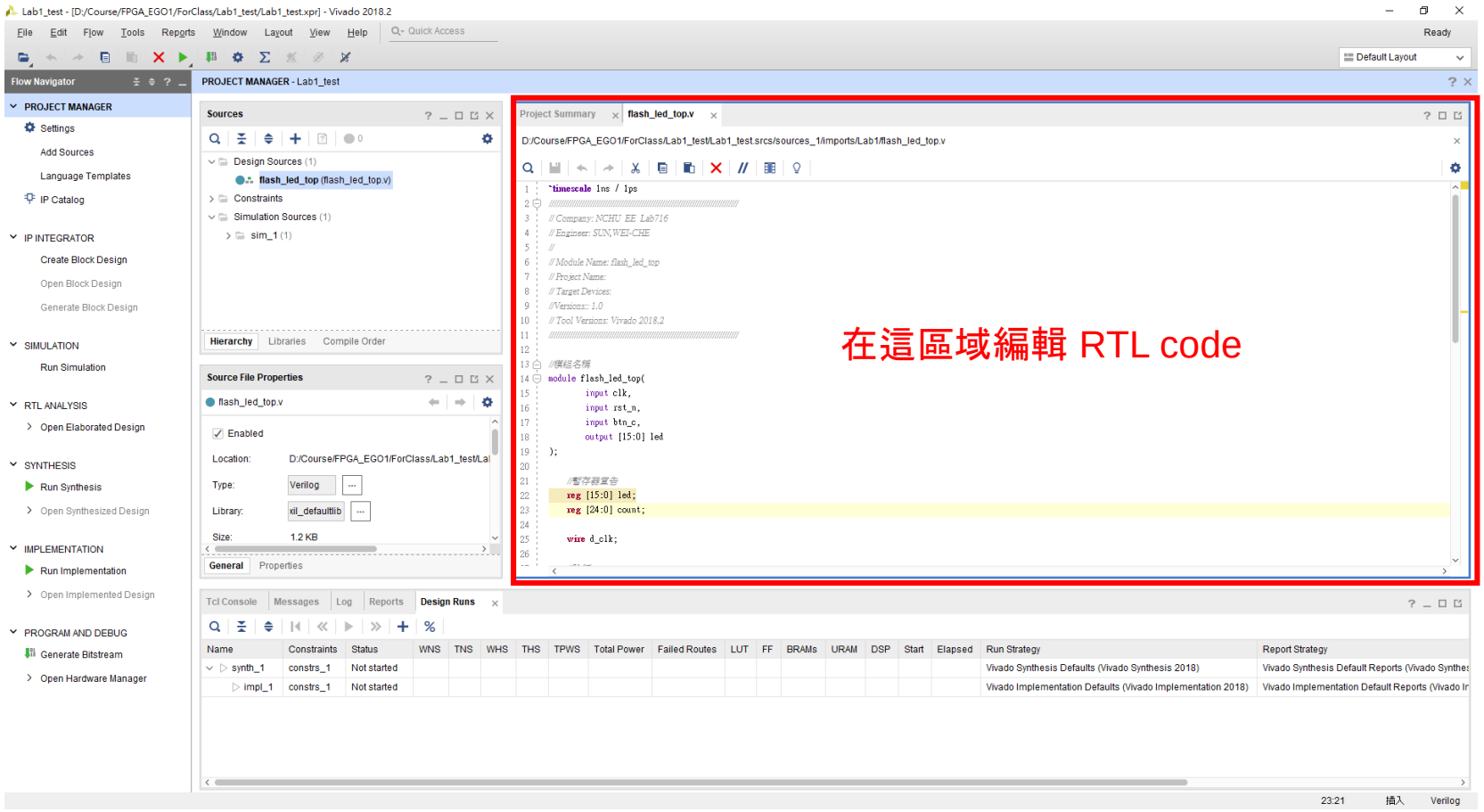
- 編輯RTL檔，必須沒有紅色底線 (若有則代表有錯誤)



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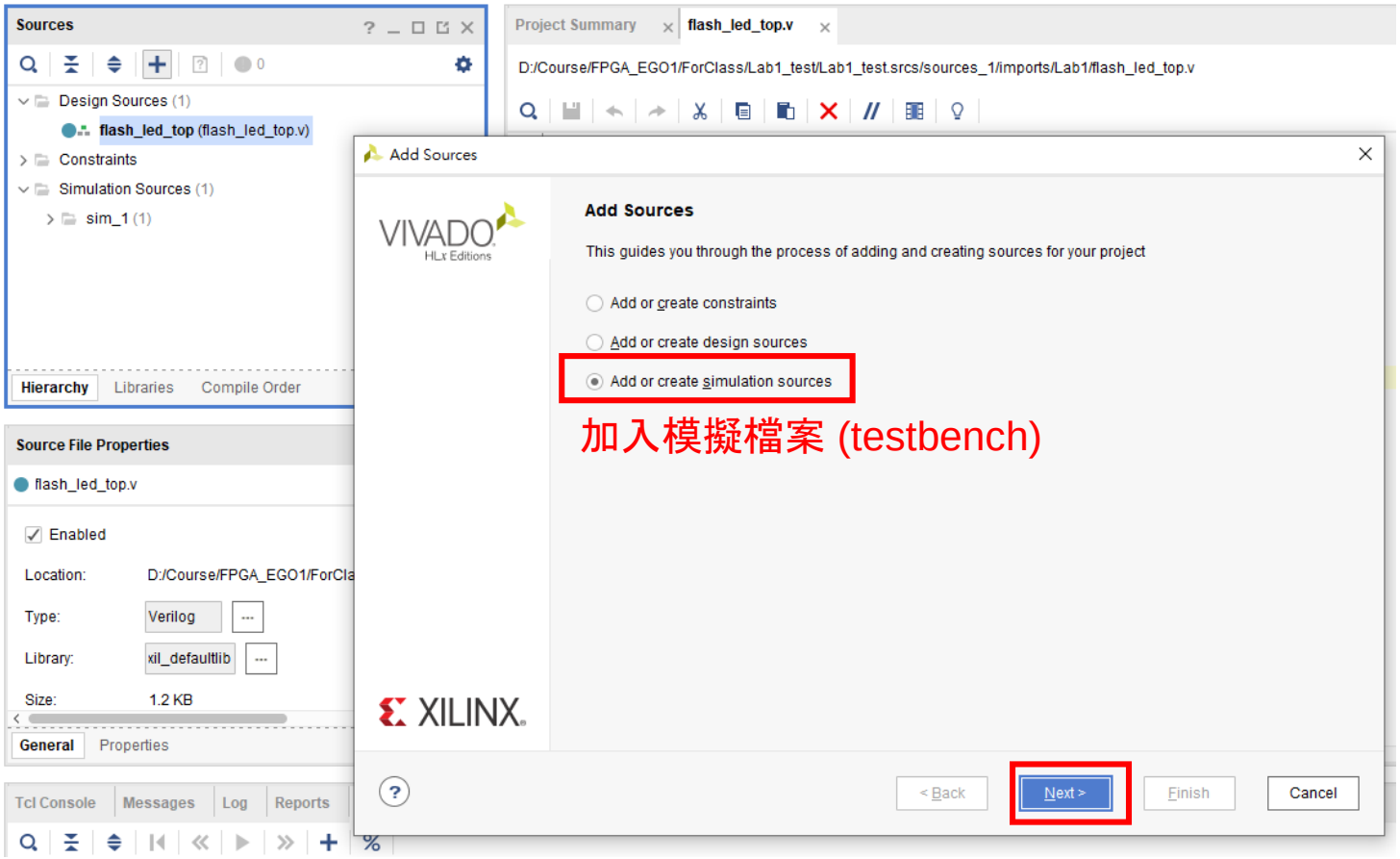
- 加入Simulation Source
- “Next”



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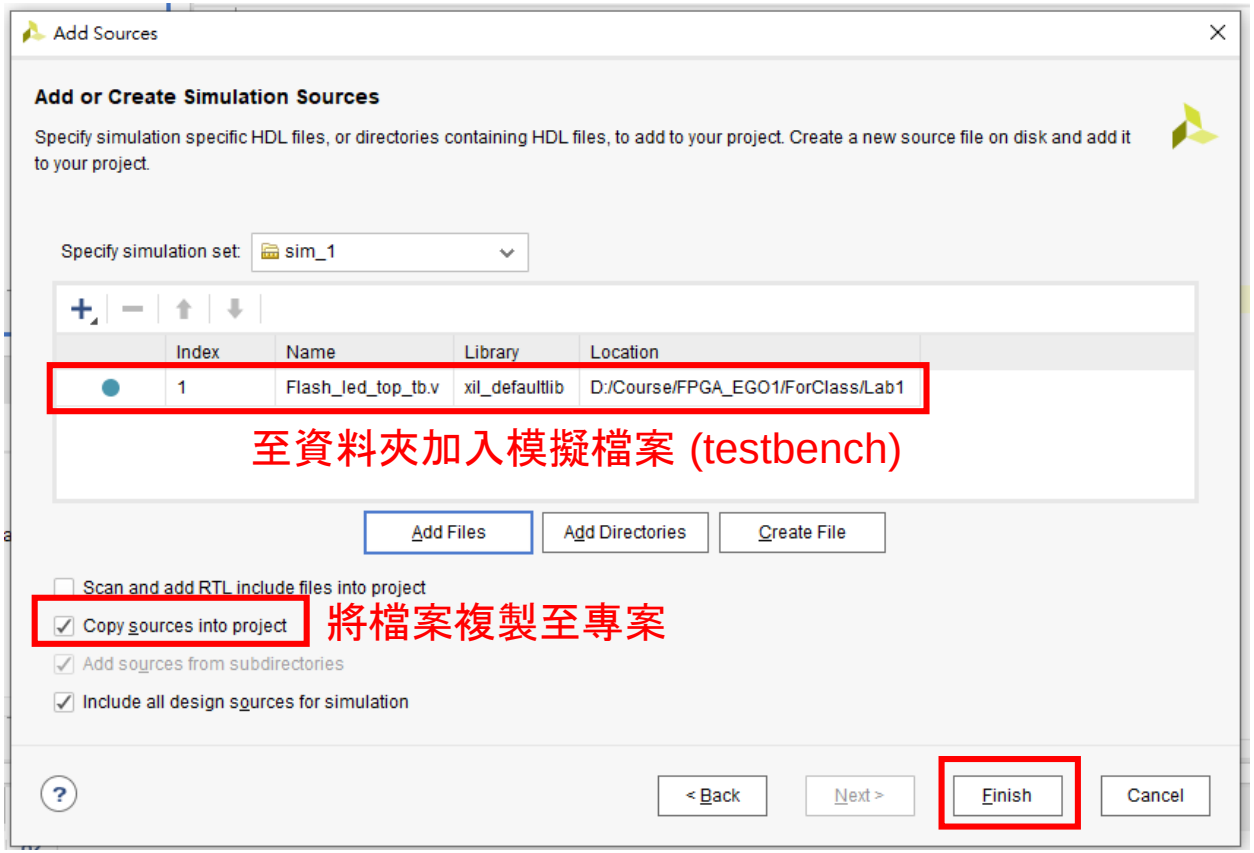
- 加入Simulation Source
- “Copy source into project”
- “Finish”



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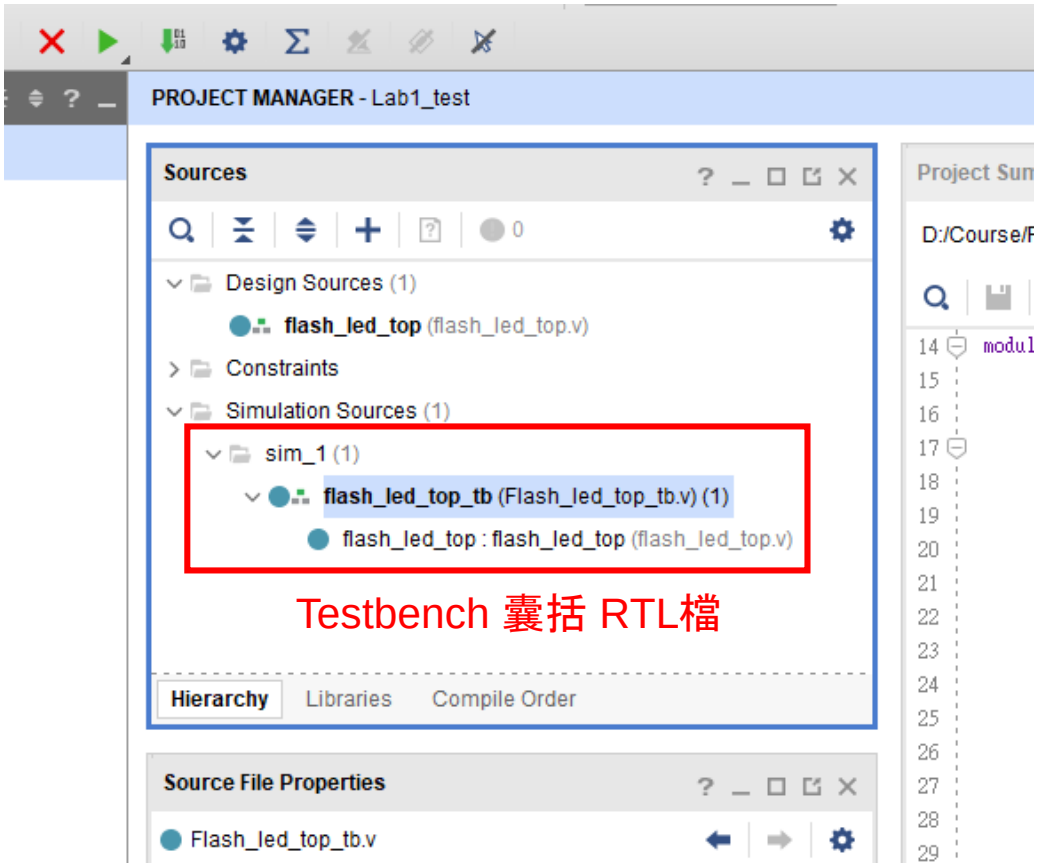
- 確認加入Simulation Source
- 並且有抓到RTL檔



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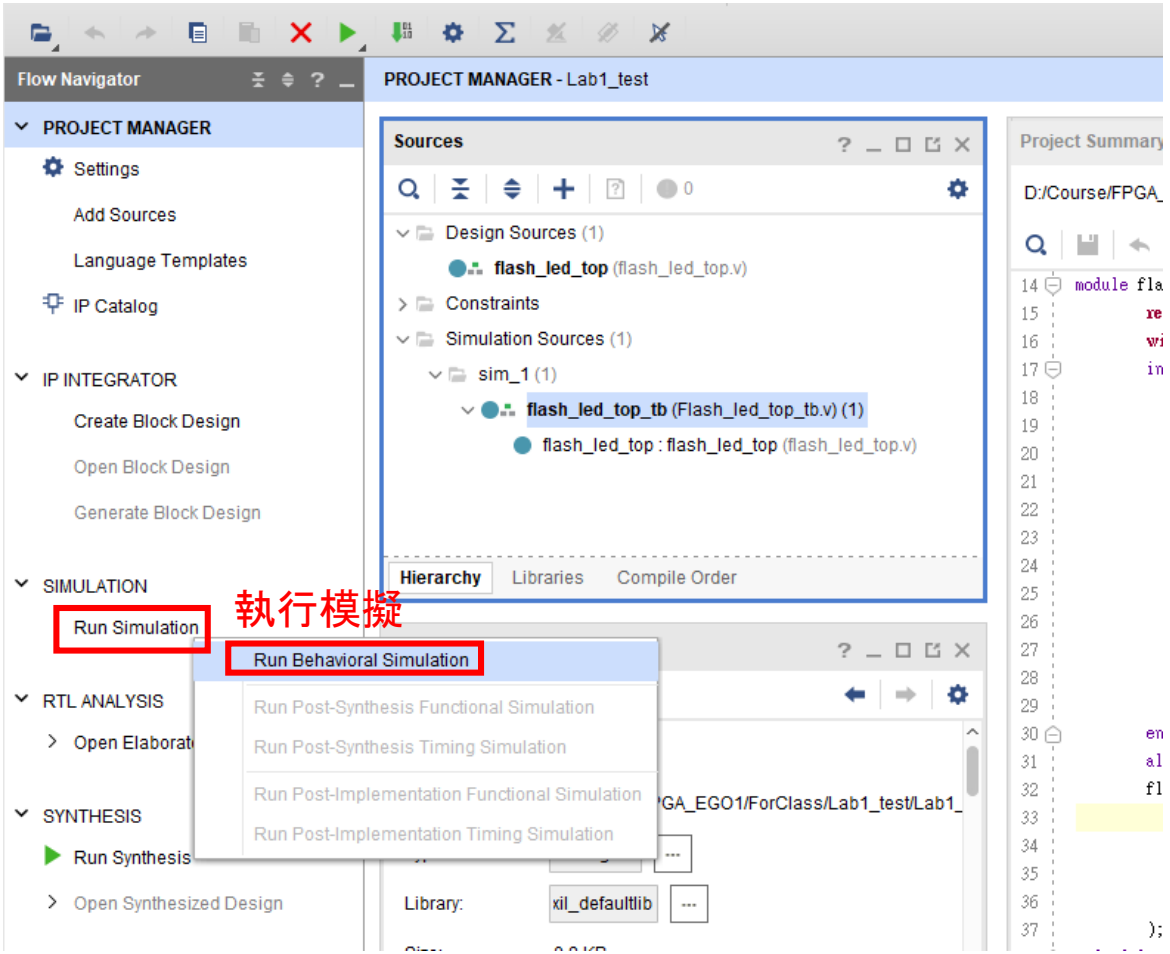
- 進行模擬
- “Run Simulation”
- “Run Behavioral Simulation”



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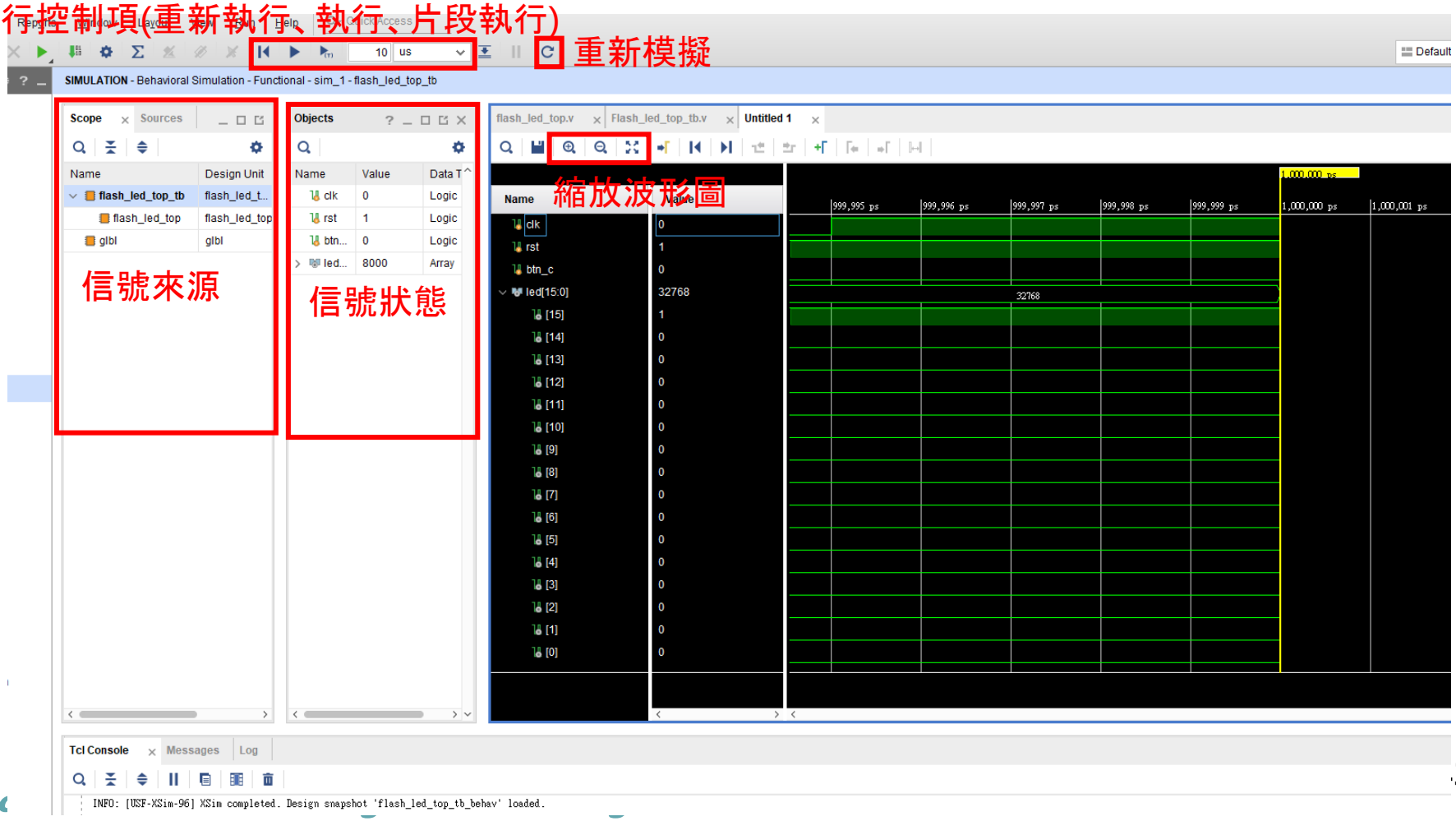
❖ 模擬版面介紹

執行控制項(重新執行、執行、片段執行)



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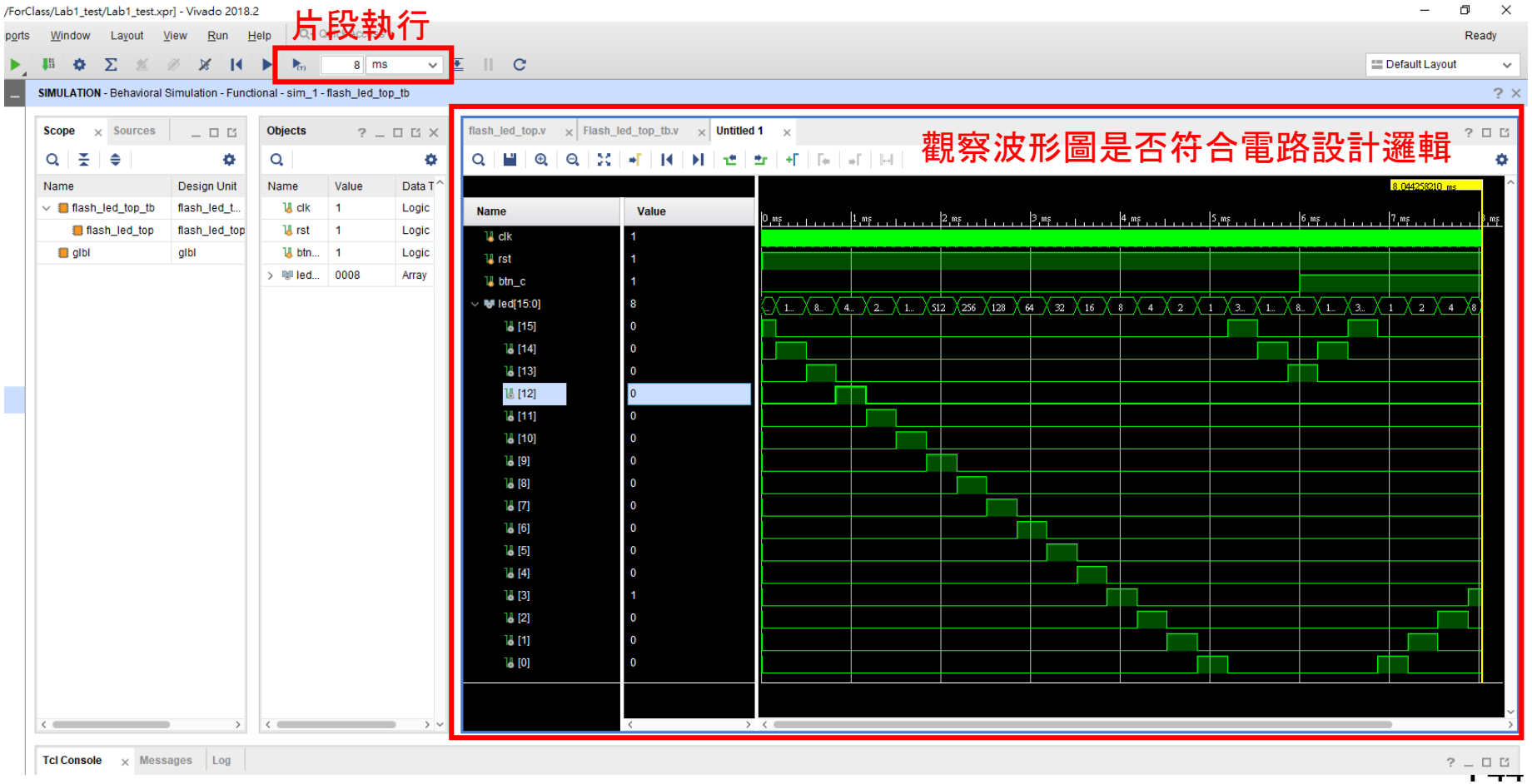
- 再往前執行8ms



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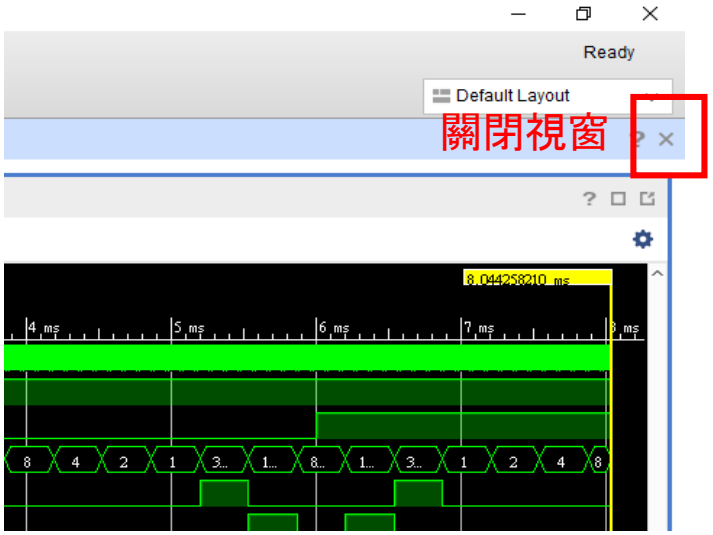
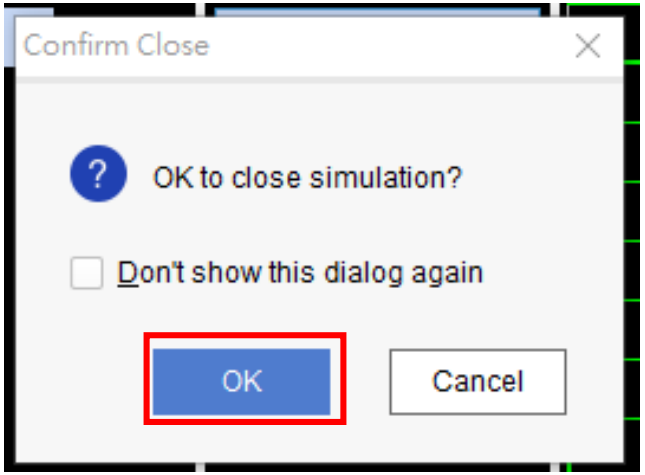
- 沒問題，關閉Simulation視窗
- “OK”





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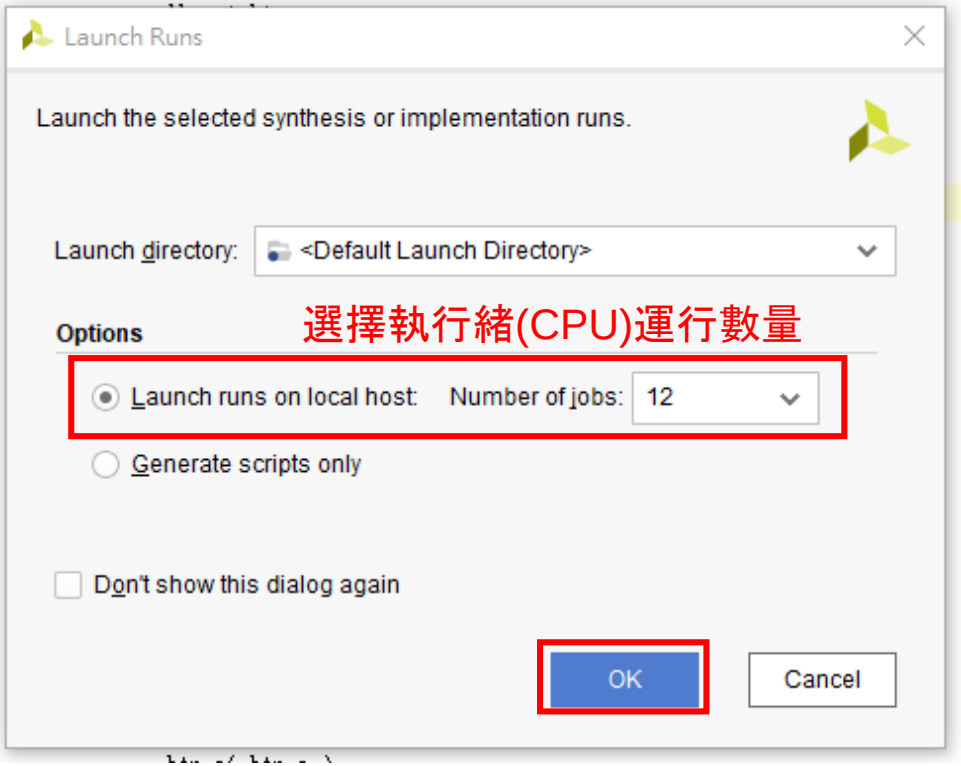
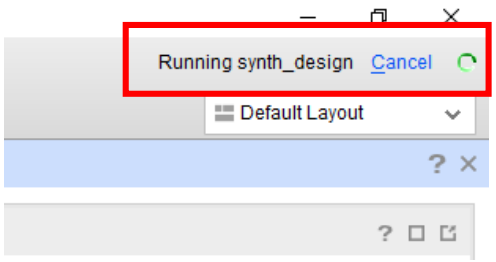
- 執行合成
- “Run Synthesis”
- “OK”





合成中 Wait……

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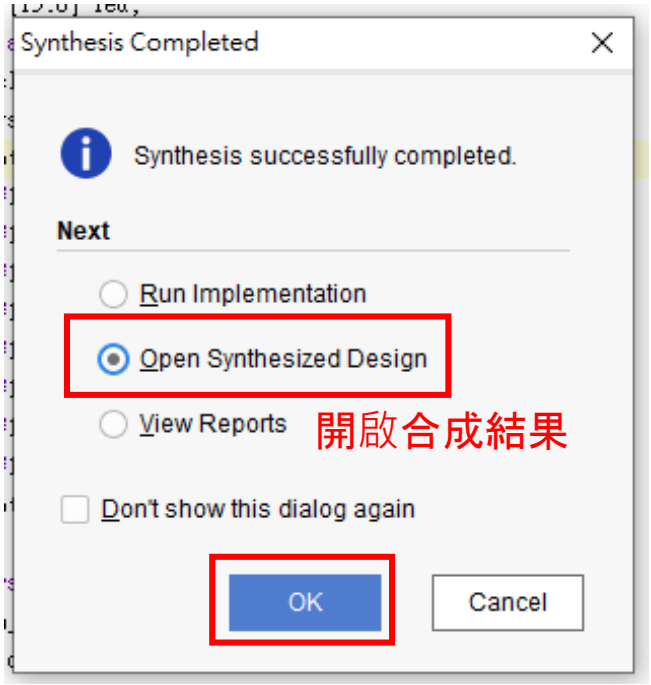
- 合成完畢，開啟合成結果
- “Open Synthesized Design”
- “OK”



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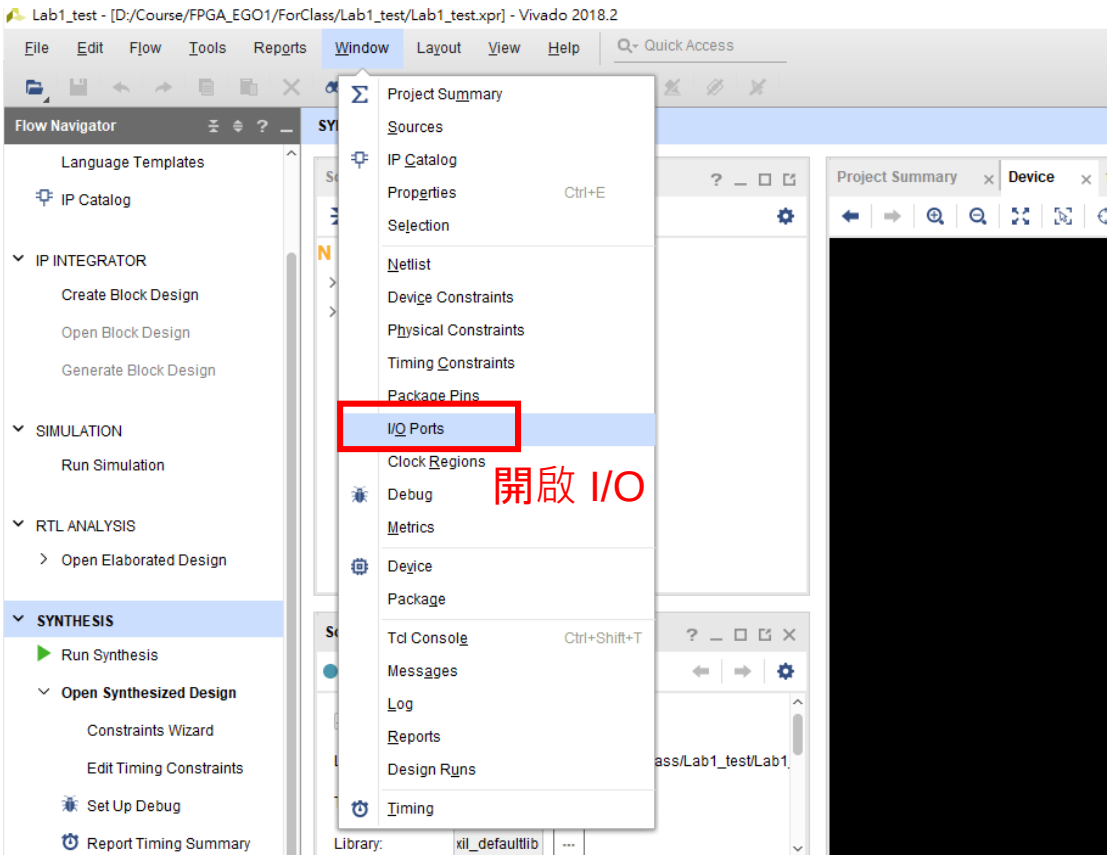
- 設定腳位資料
- “Window”→“I/O Ports”



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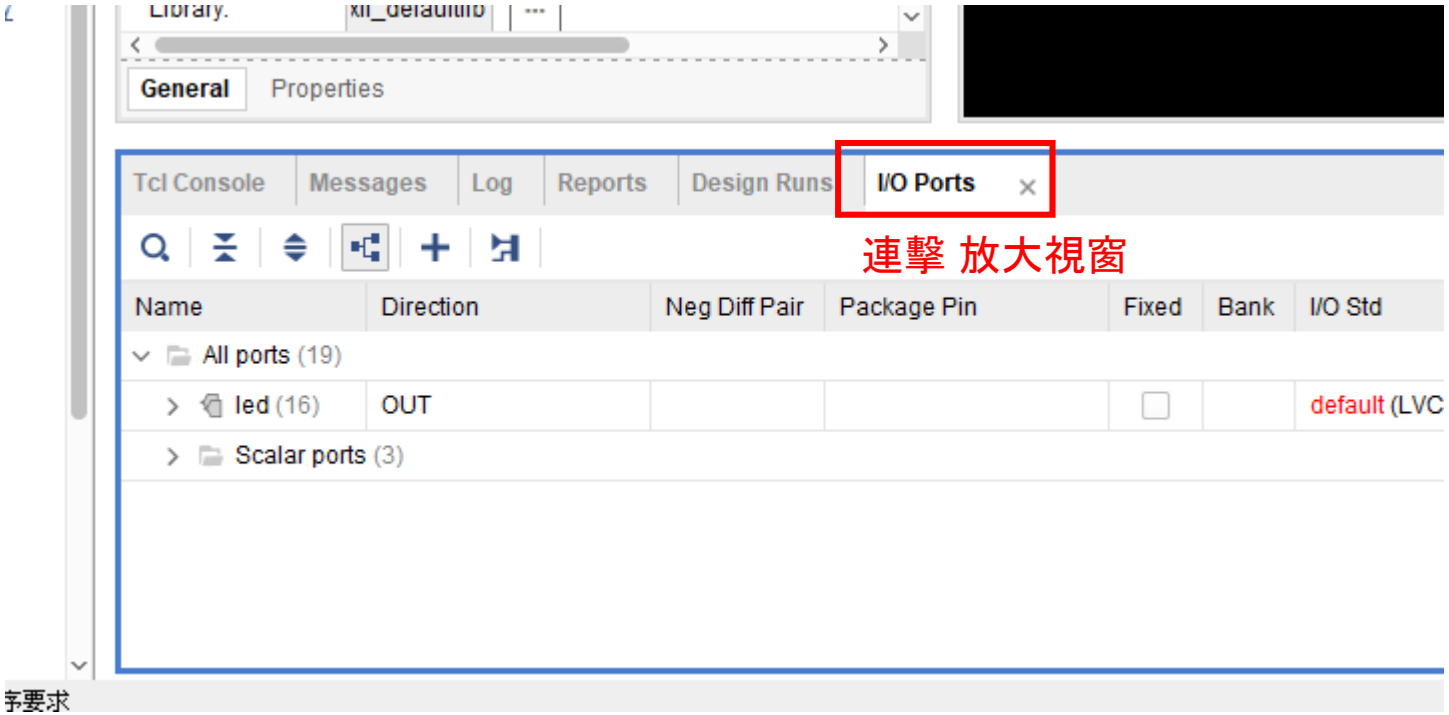
- 於下方視窗出現I/O Ports
- 連擊 I/O Ports標題放大視窗



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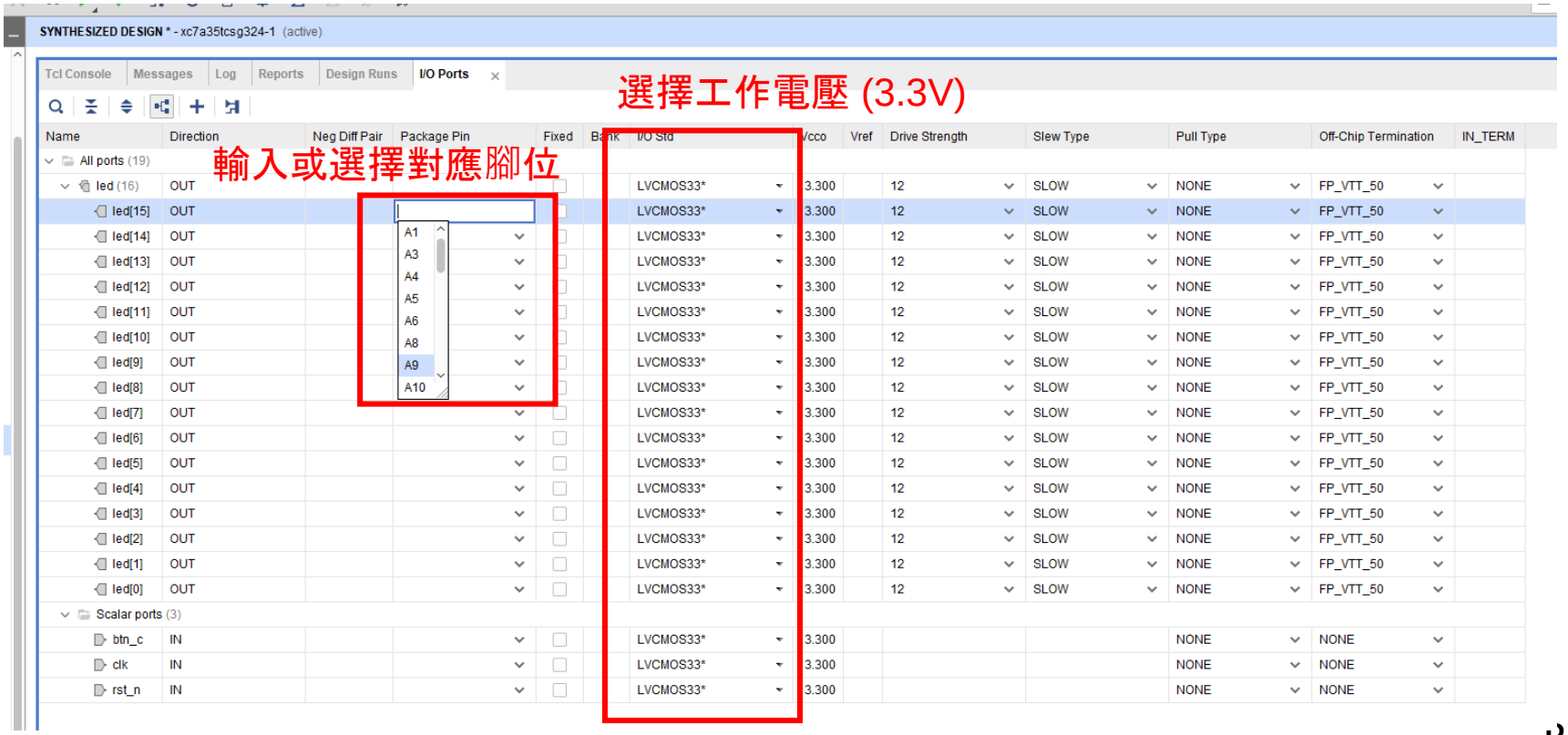
- 將I/O Ports 設定至對應的腳位、工作電壓(LVCMOS33)
- 參考前面的腳位對應表



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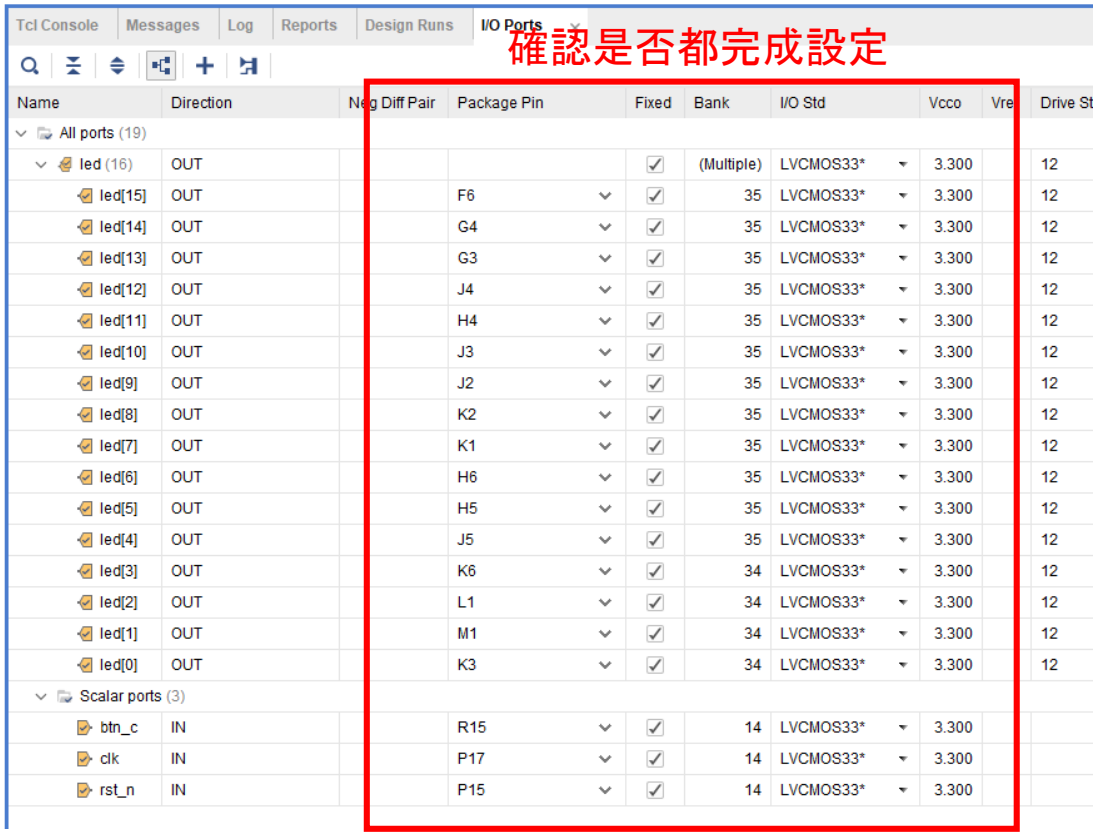
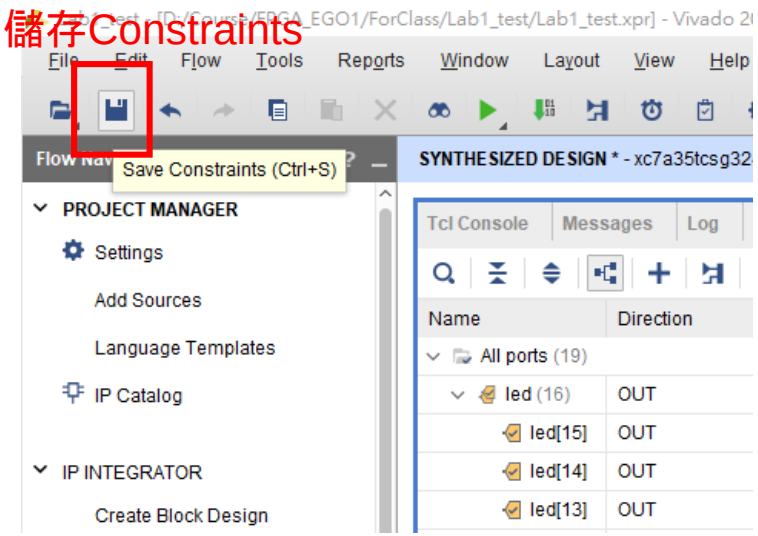
- 確認腳位設定
- 儲存約束檔案 Constraint





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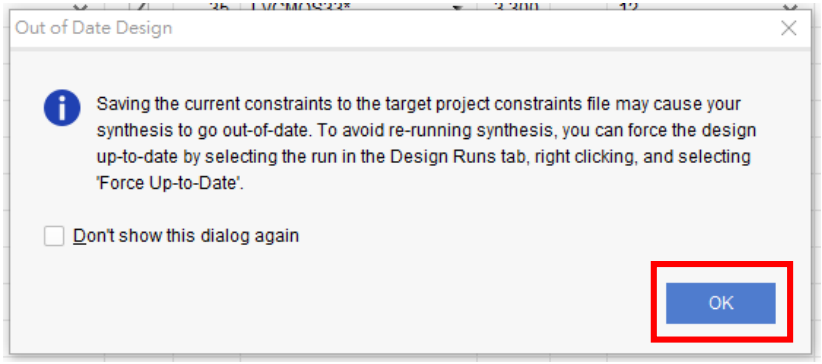
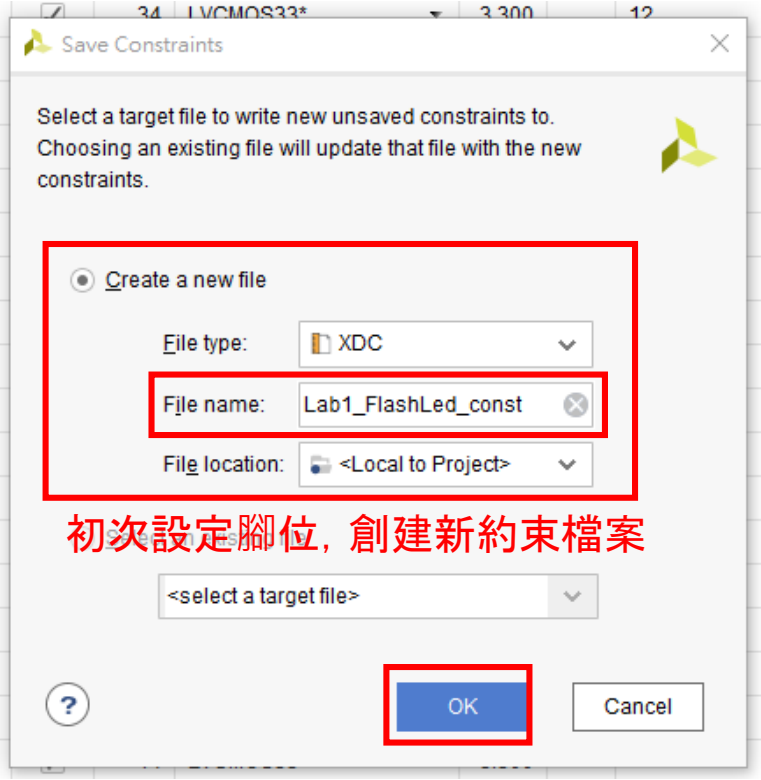
- 提醒儲存約束檔案，會導致合成結果過期，需重新合成
- “OK”
- 設定腳位檔名稱
- “OK”





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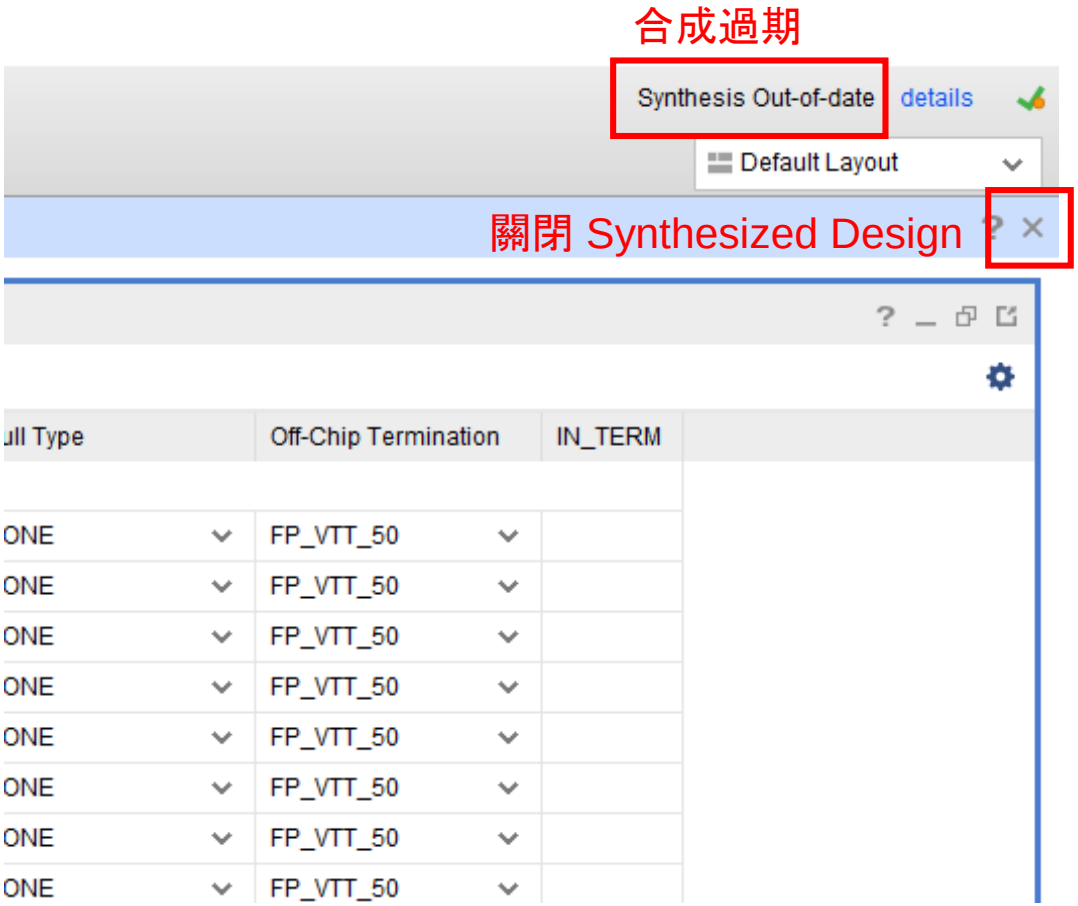
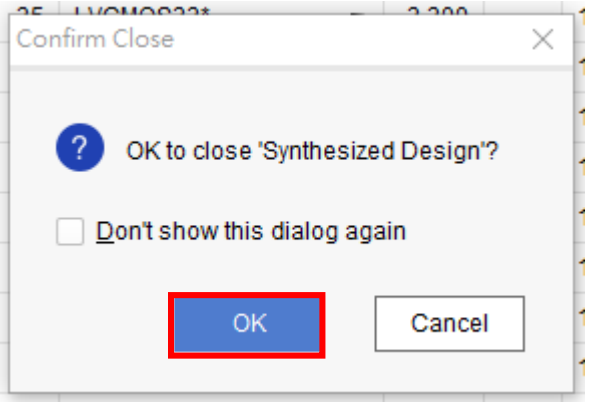
- 關閉 Synthesized Design





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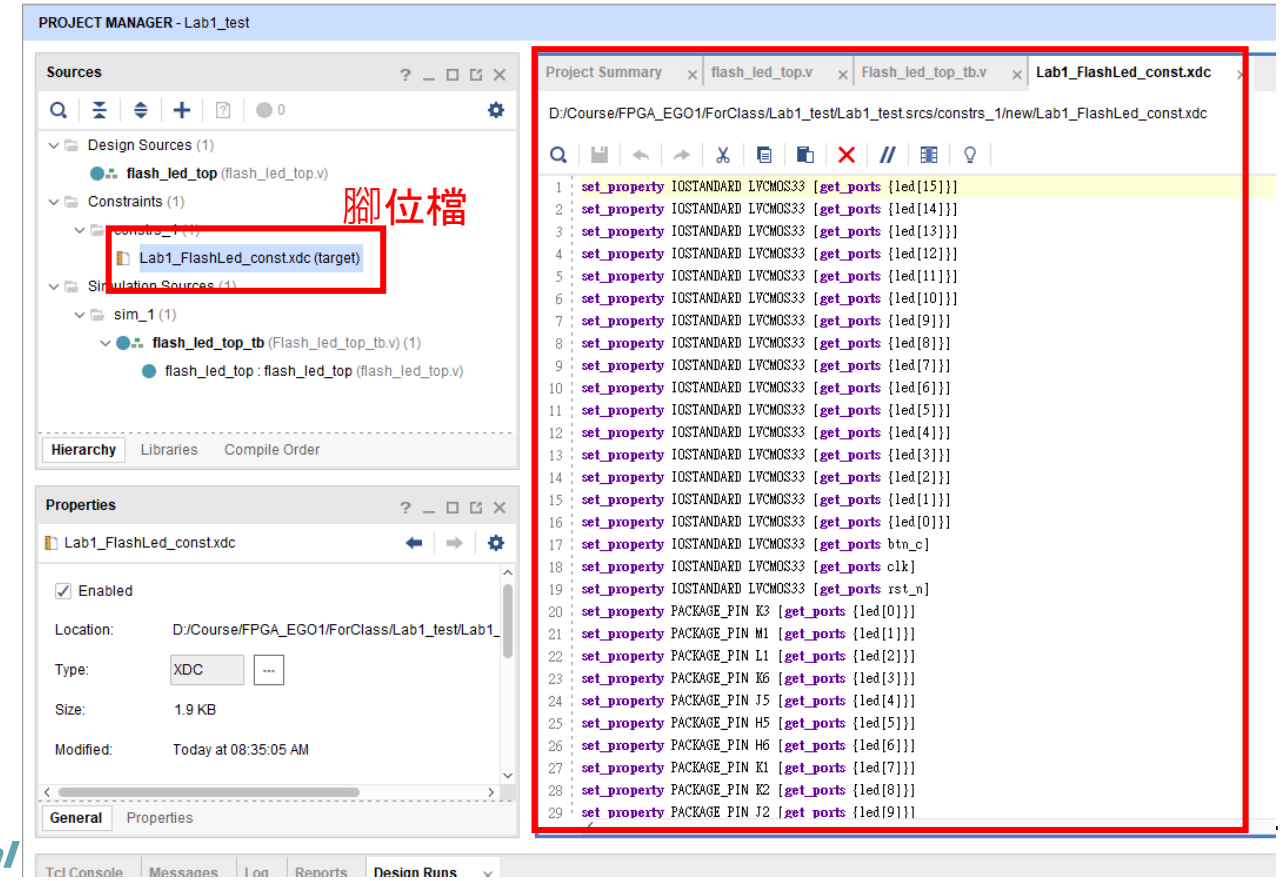
- 查看腳位檔(.xdc檔)
- 在接下來的實驗中將通過直接添加constraints的方式來對設計進行腳位分配。



Vivado 2018.2

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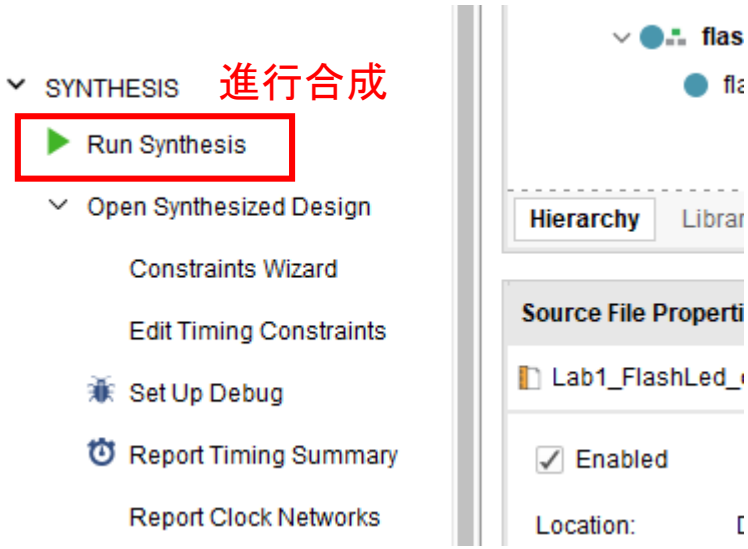
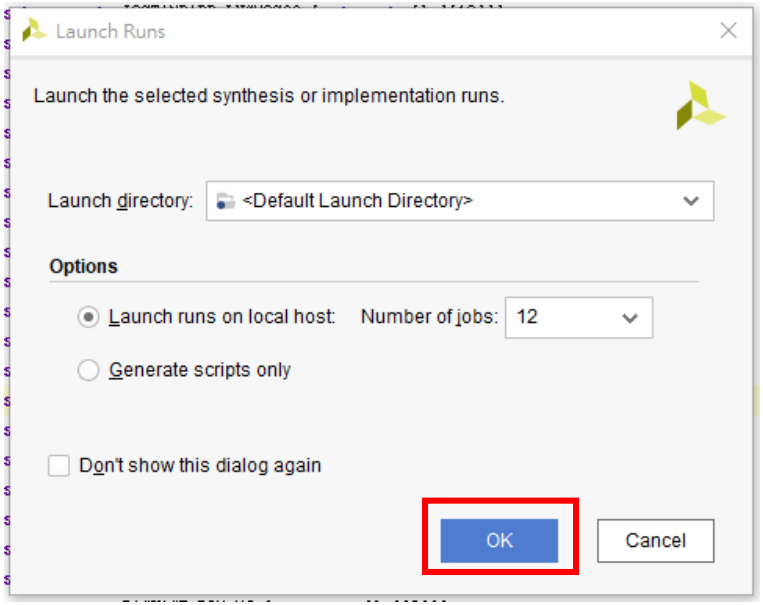
❖ 重新進行合成(Synthesis)





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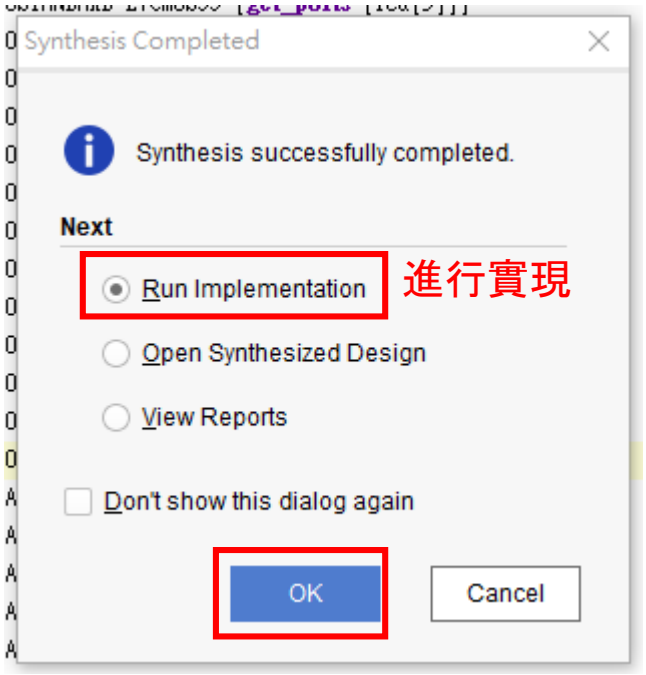
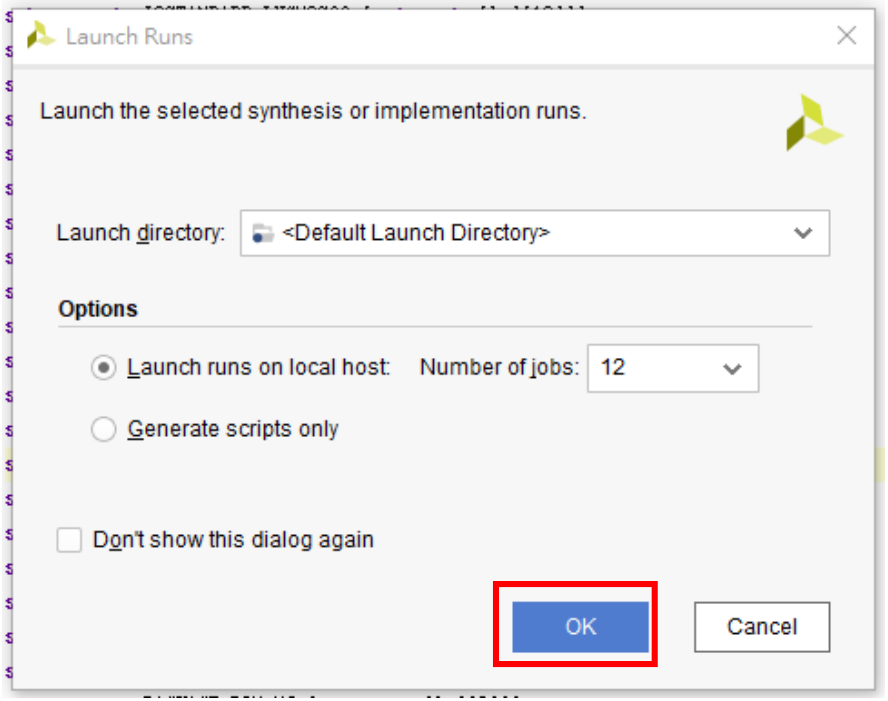
- 進行實現 (Implementation)
- “Run Implementation”
- “OK” ”OK”





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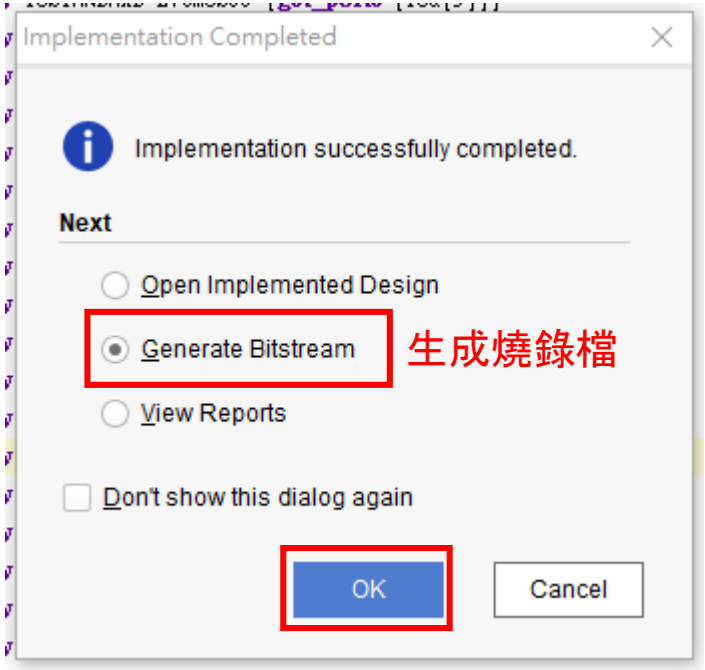
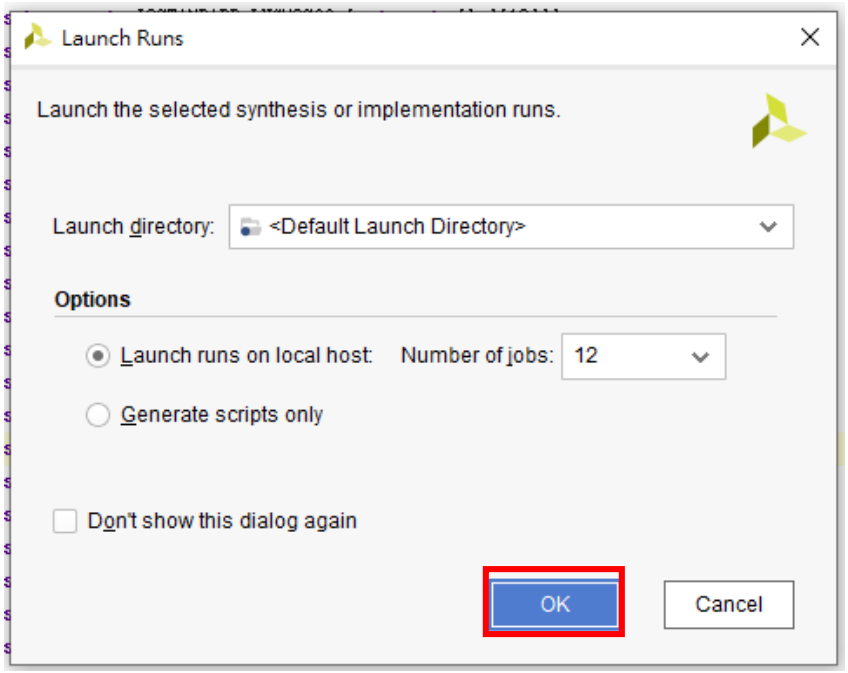
- 生成燒錄檔 (Bitstream)
- “Generate Bitstream”
- “OK” “OK”





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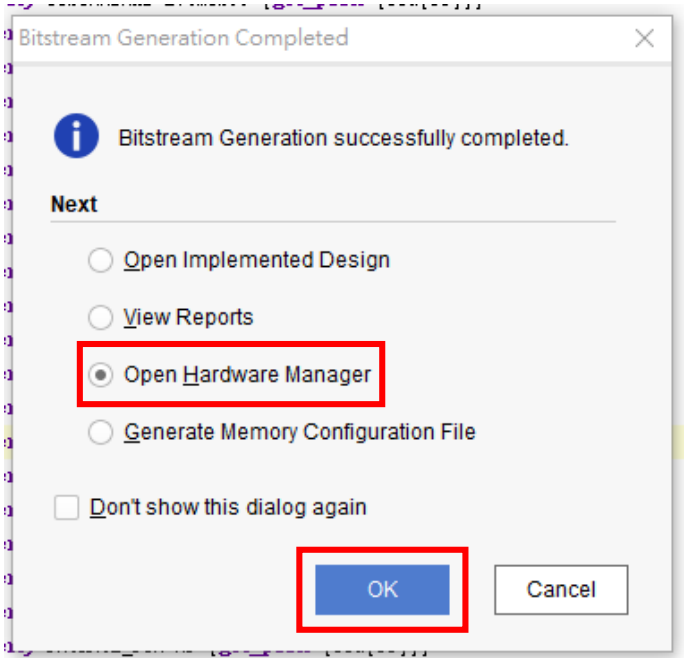
- 生成燒錄檔完成後，選擇 “Open Hardware Manager”



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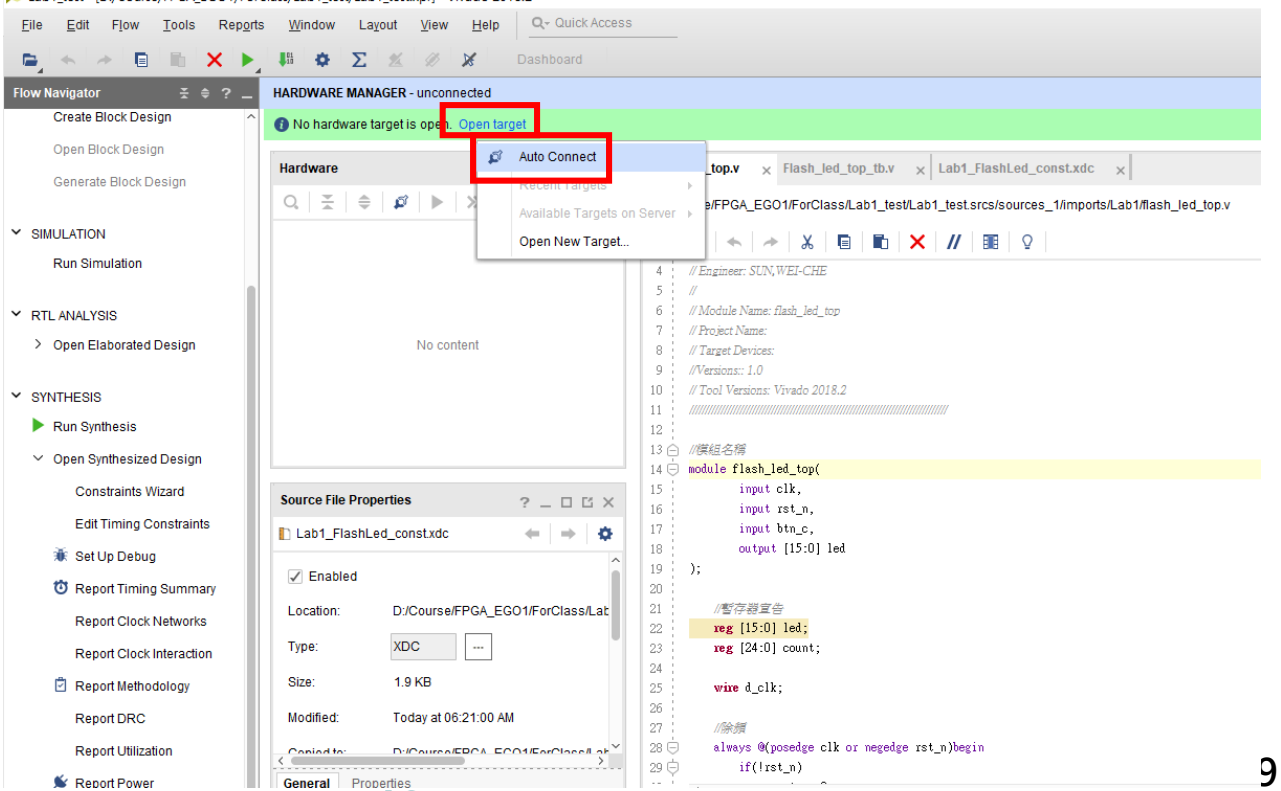
- 將FPGA板連接至電腦，並開啟電源，才能讓軟體偵測到板子
- 點擊“Open target”，選擇 “Auto Connect”



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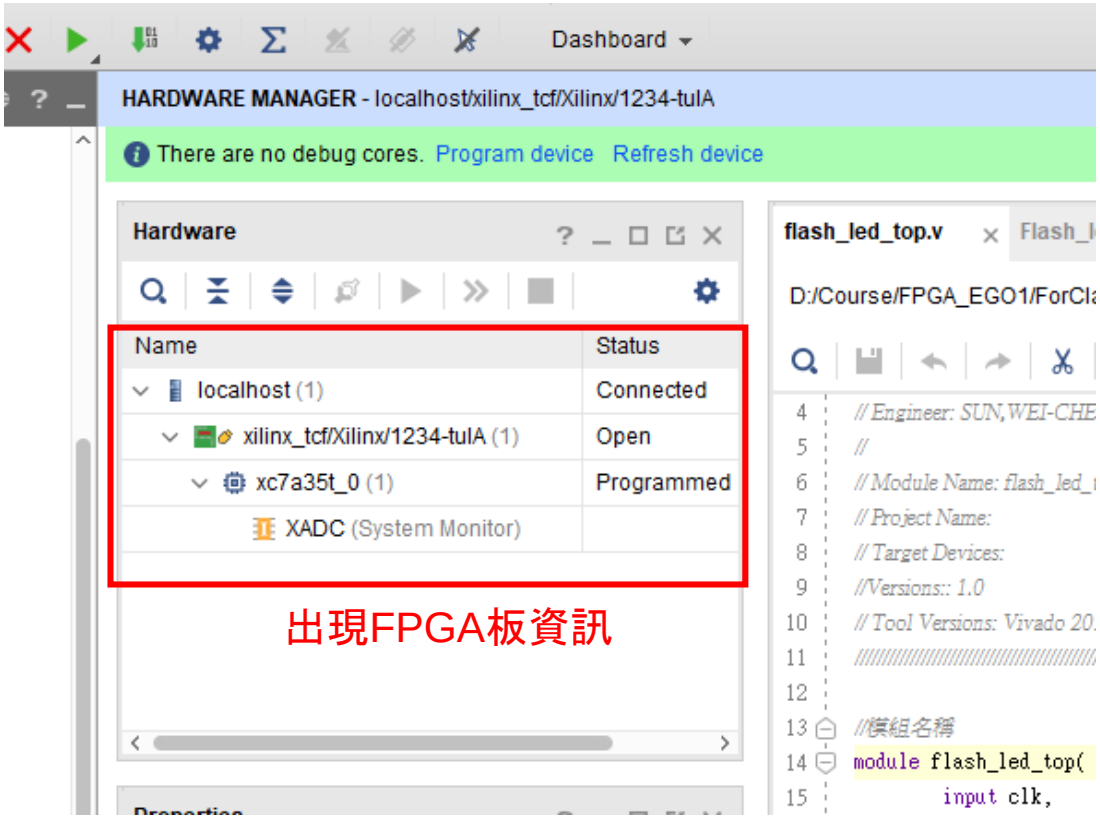
- 出現FPGA板資訊，表示成功連接至電腦



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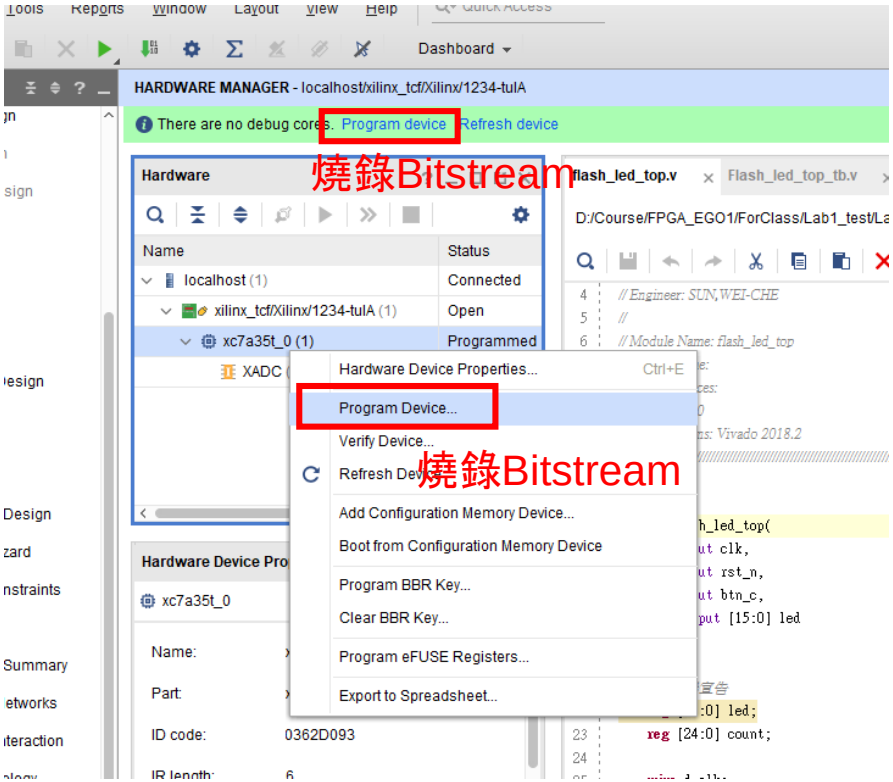
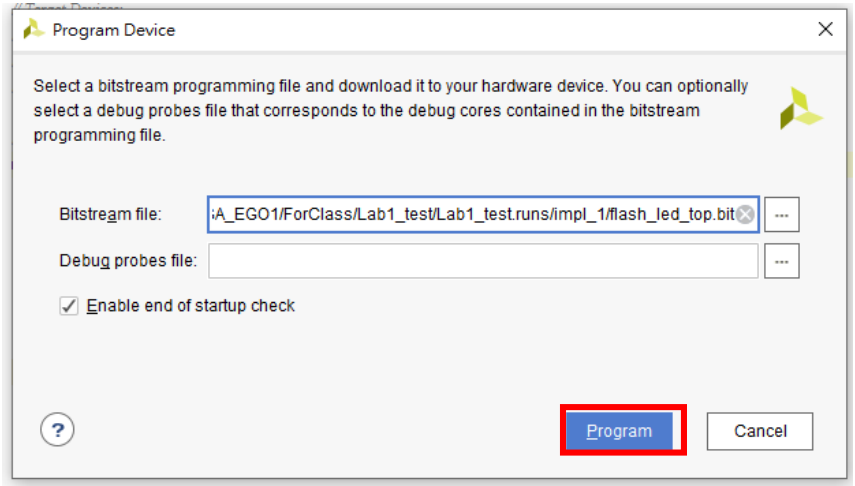
- 將Bitstrean燒錄至FPGA板
- 點擊“Program”





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- 完成燒錄！！！

Synthesis

Verilog

Implementation

Vivado

Program

.v

FPGA

Bitstream

.xdc

testbench

I/O Ports

https://www.google.com/url?sa=i&url=https%3A%2F%2Fmeteor.today%2Farticle%2FBfglq-&psig=AOvVaw12MTQsEYeQGYJoC40Q_eNB&ust=1585271687771000&source=images&cd=vfe&ved=0CAIQjRxqFwoTCKinhJu00ugCFQAAAAAdAAAAABAM

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Thank you for your attention!