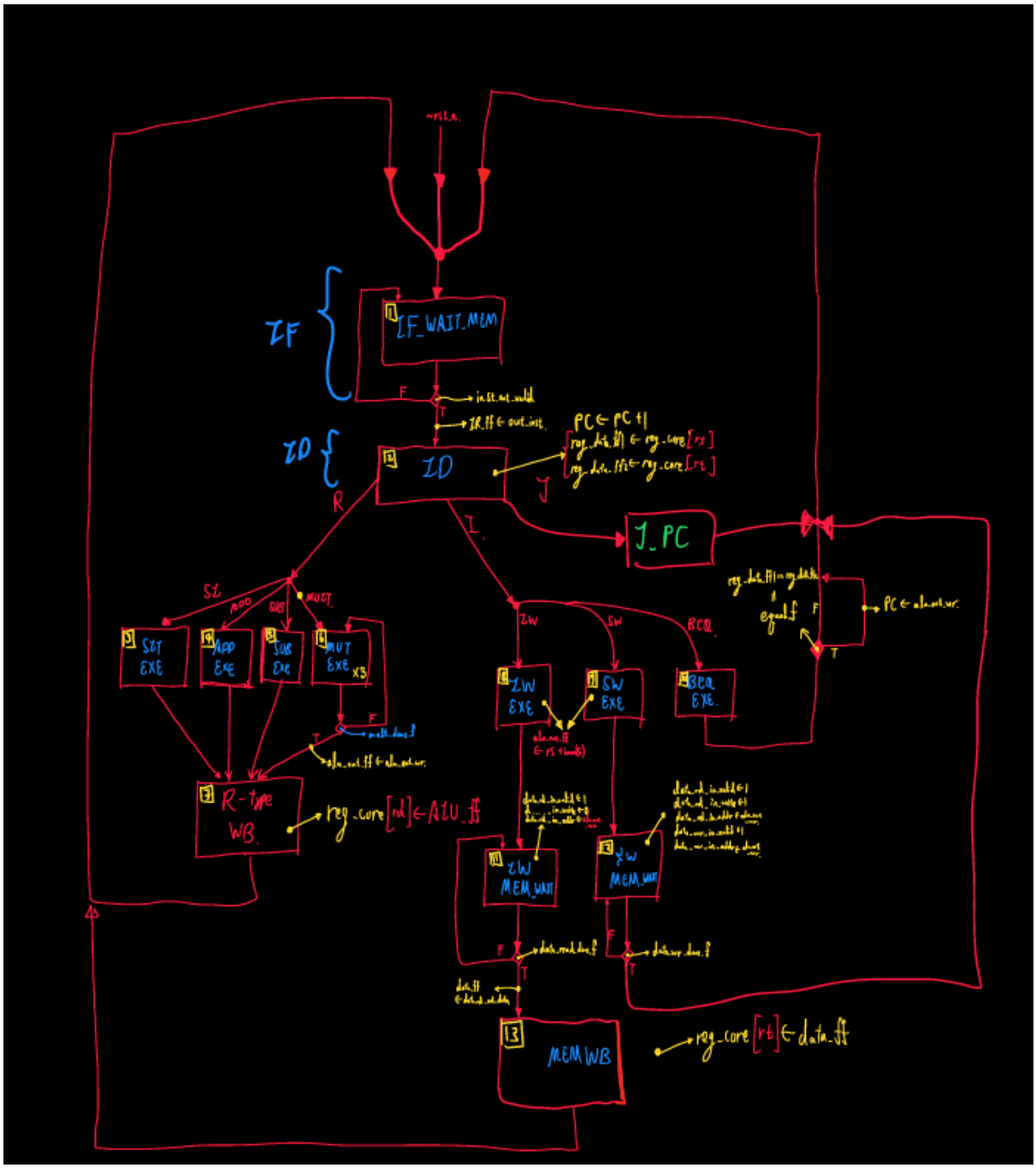
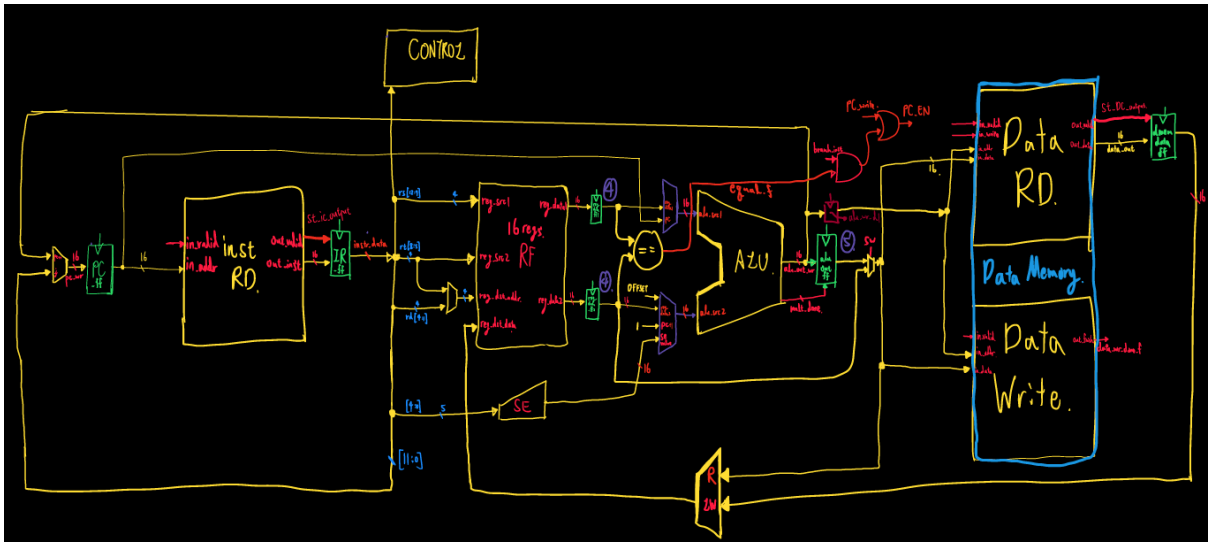
Main Control Of FSM

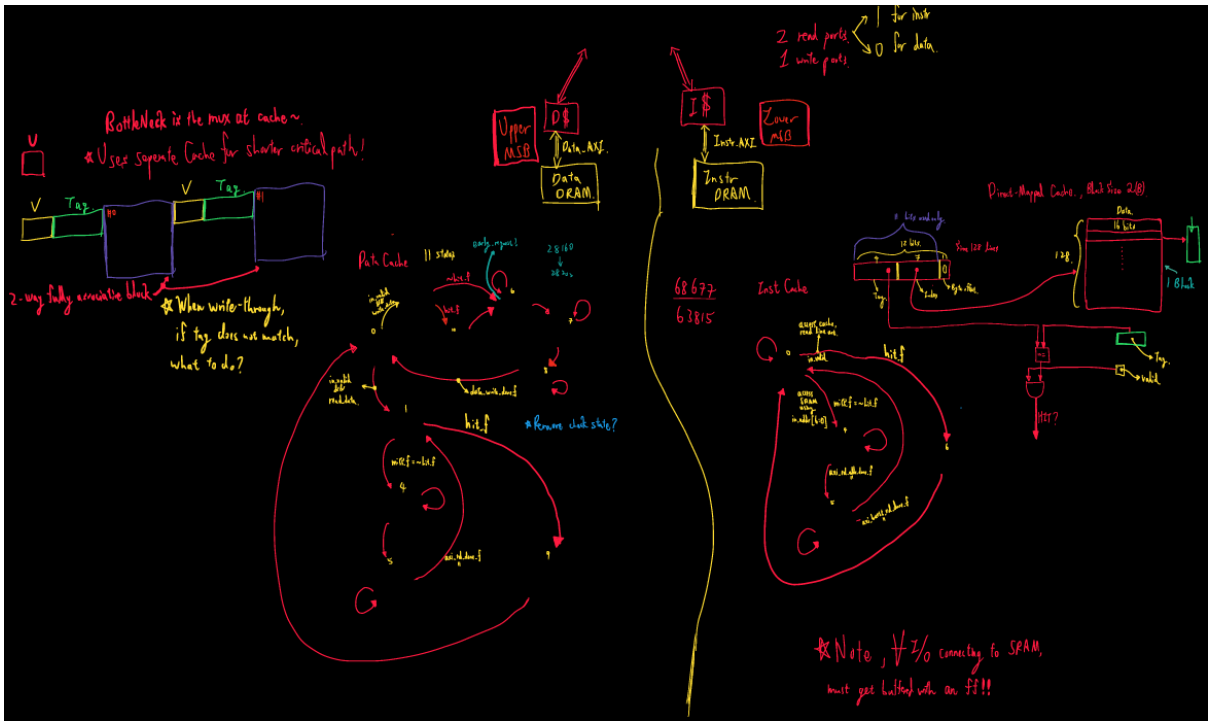


Due to the complexity of pipeline hazards, I chose to design the whole cpu in a multicycle fashion which is much easier.

Datapath Of CPU



Instruction Read and Data read interfaces to access memory, also share execution units through a single ALU.



I use 2 128x16 blocks of fully-associative block for better hit rate, which might provide great improvement when the pattern has lots of beq or j-type instruction.