



# **Lab3: Multiply Accumulation Unit Design with PA**

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Machine Learning Intelligent Chip Design  
2024 Spring

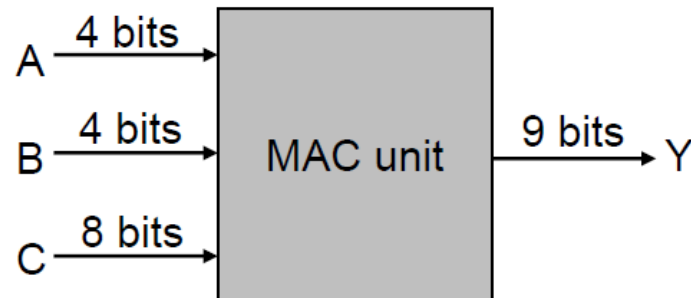




# Introduction

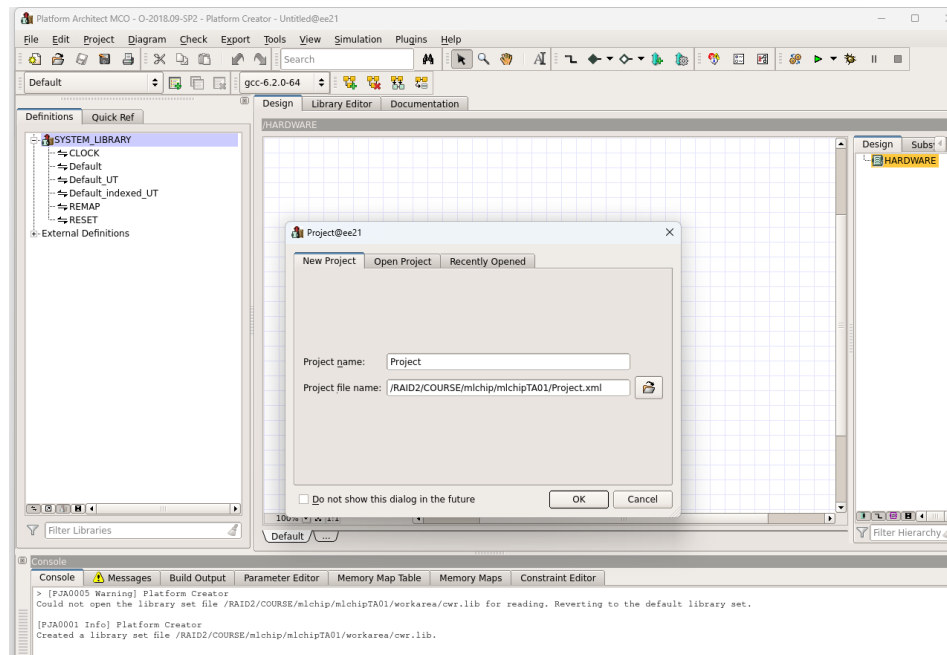
❖ Design a multiply accumulate unit

❖  $Y = A \times B + C$



## Environmental preparation

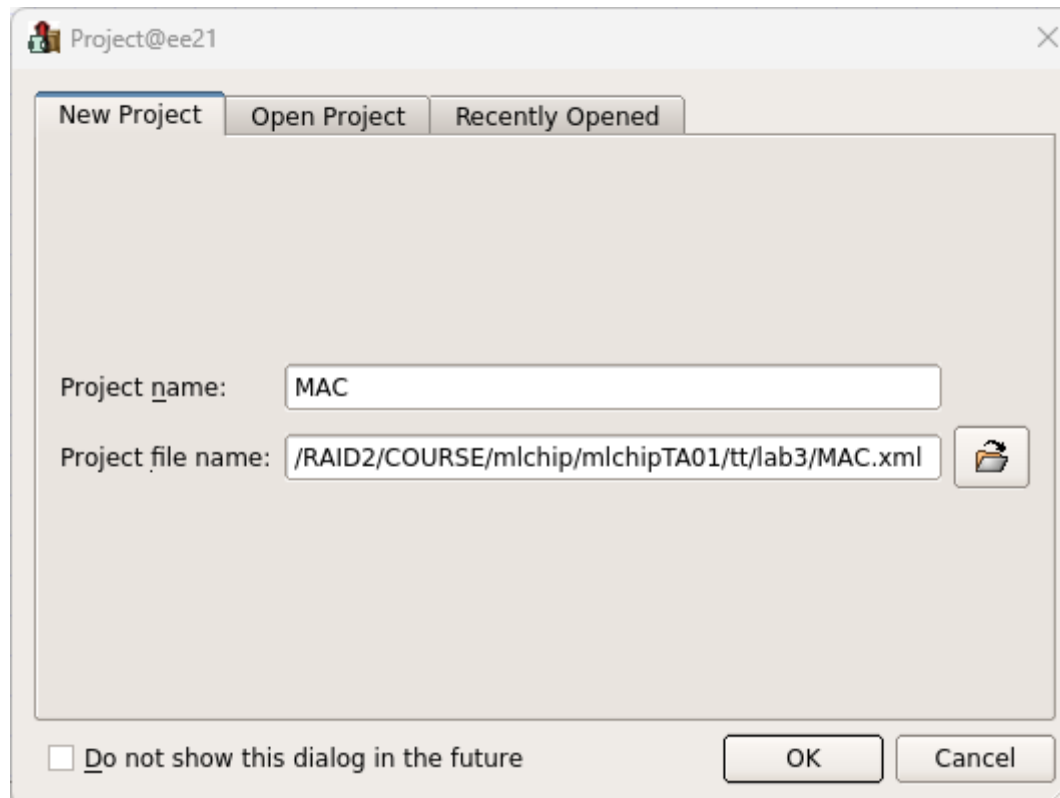
- ❖ `cp /RAID2/COURSE/mlchip/mlchipTA01/sharing/lab3.zip .`
- ❖ `unzip lab3.zip`
- ❖ `source /RAID2/cad/synopsys/CIC/vcs.cshrc`
- ❖ `source /RAID2/cad/synopsys/CIC/pa_virtualizer.cshrc`
- ❖ `pct &`





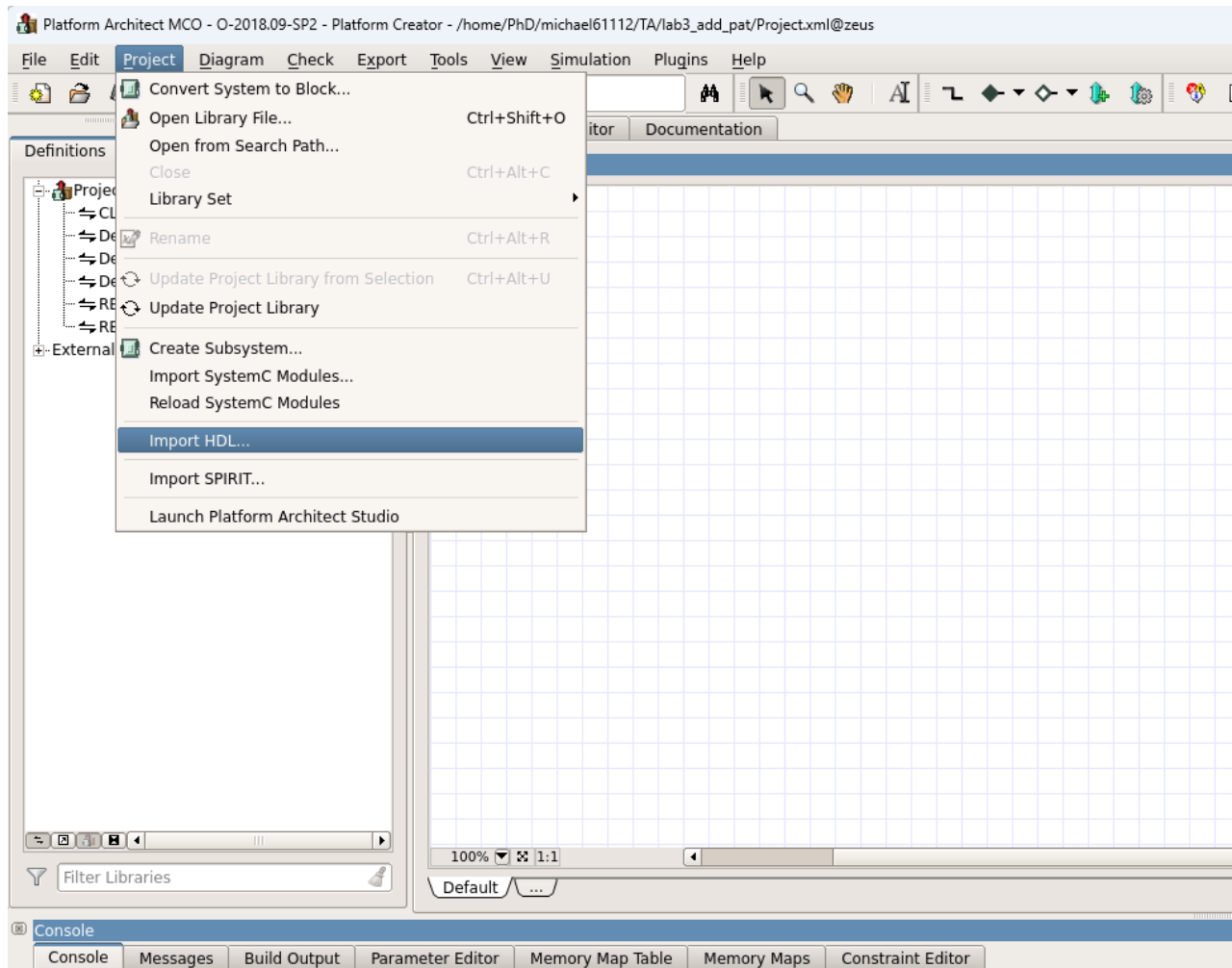
# Platform Architect

- ❖ Create project -> Project name -> Project file name -> OK





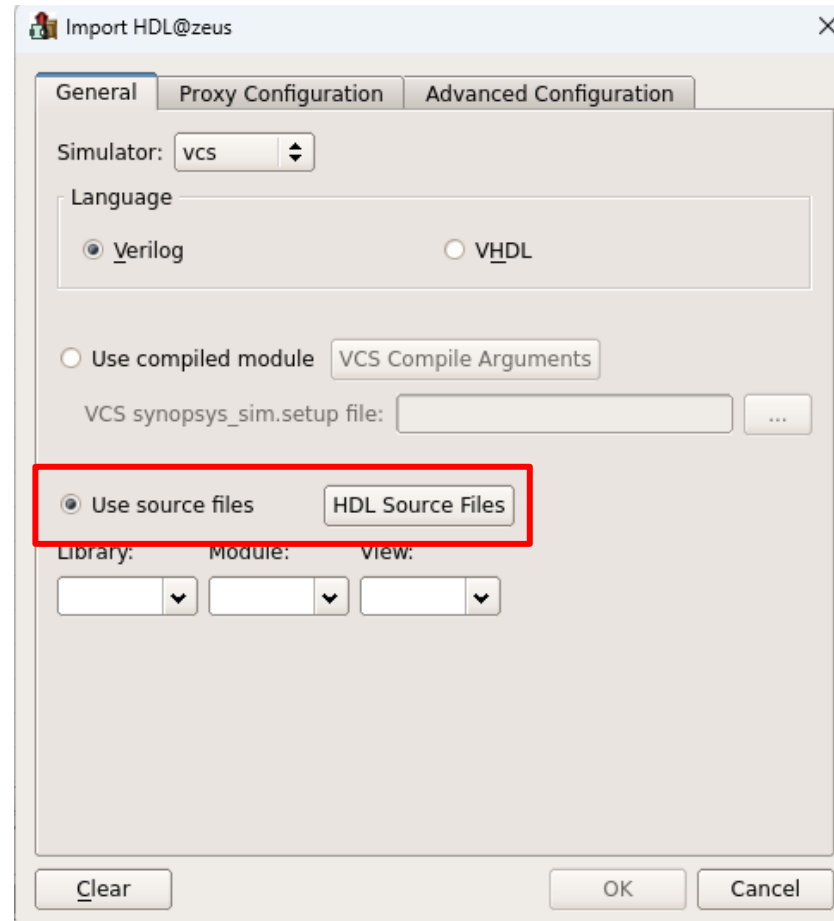
# Import HDL (1/4)





## Import HDL (2/4)

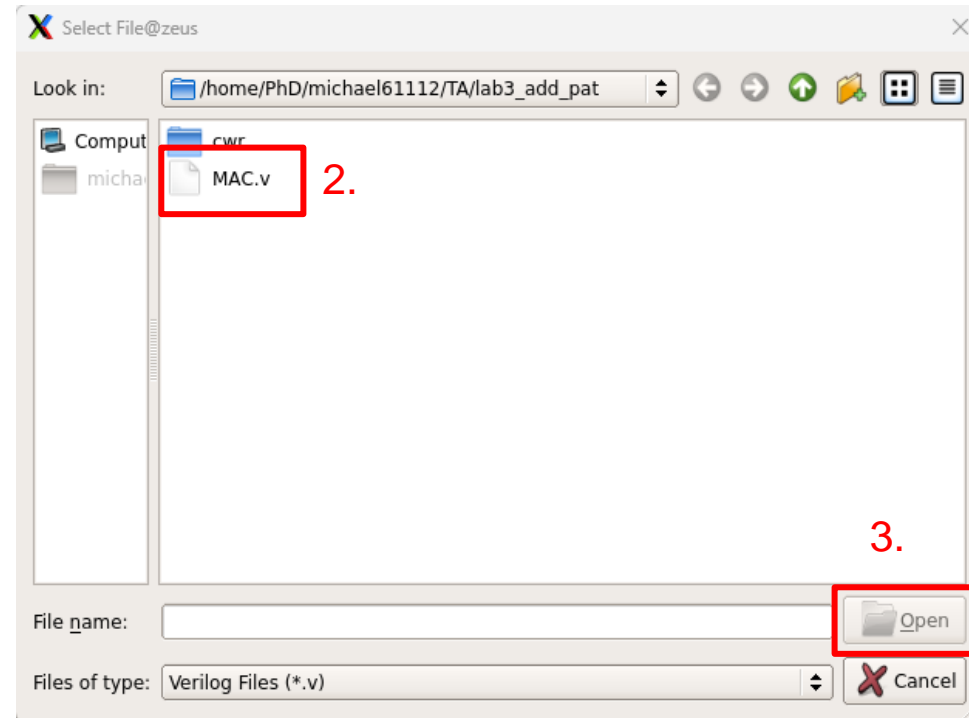
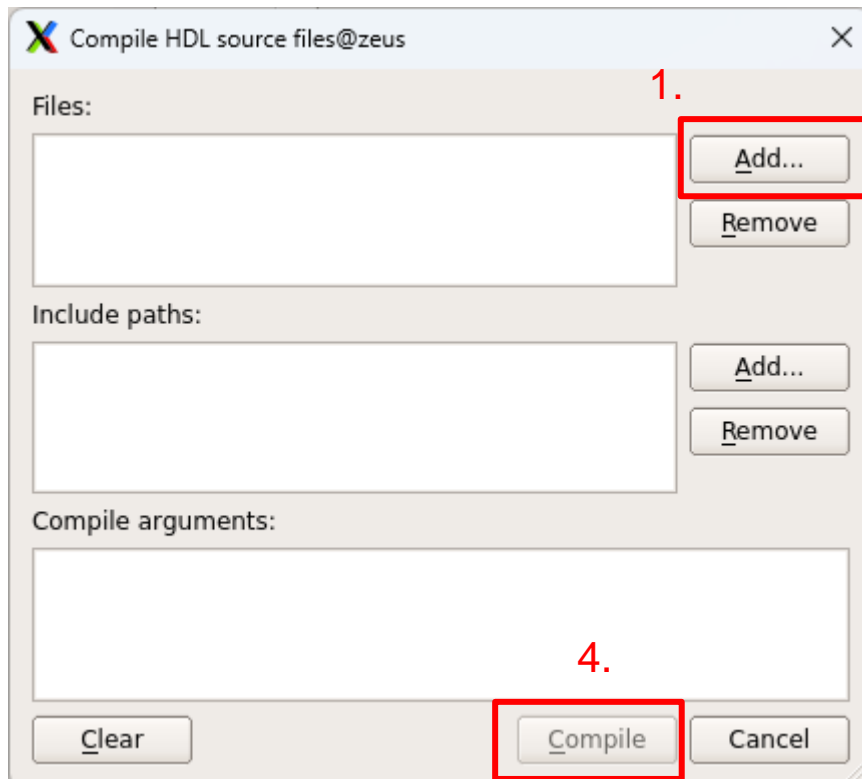
❖ General -> Use source files





## Import HDL (3/4)

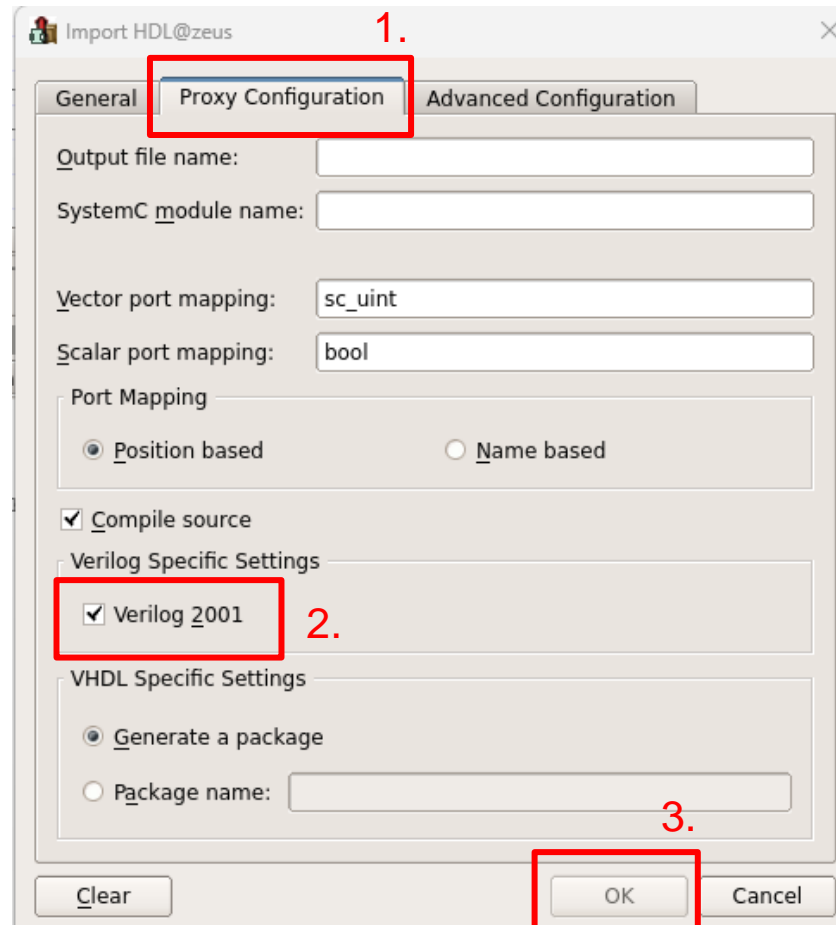
### ❖ Add MAC.v





## Import HDL (4/4)

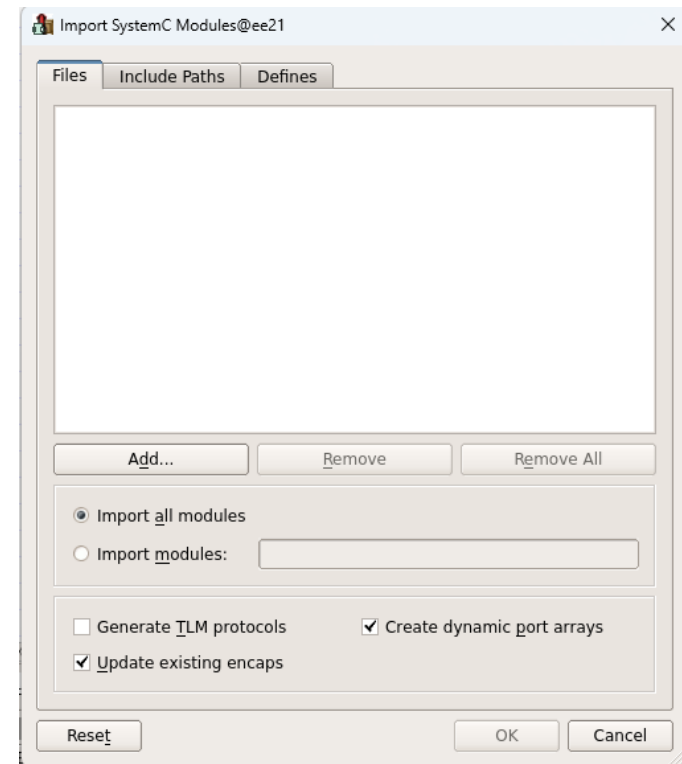
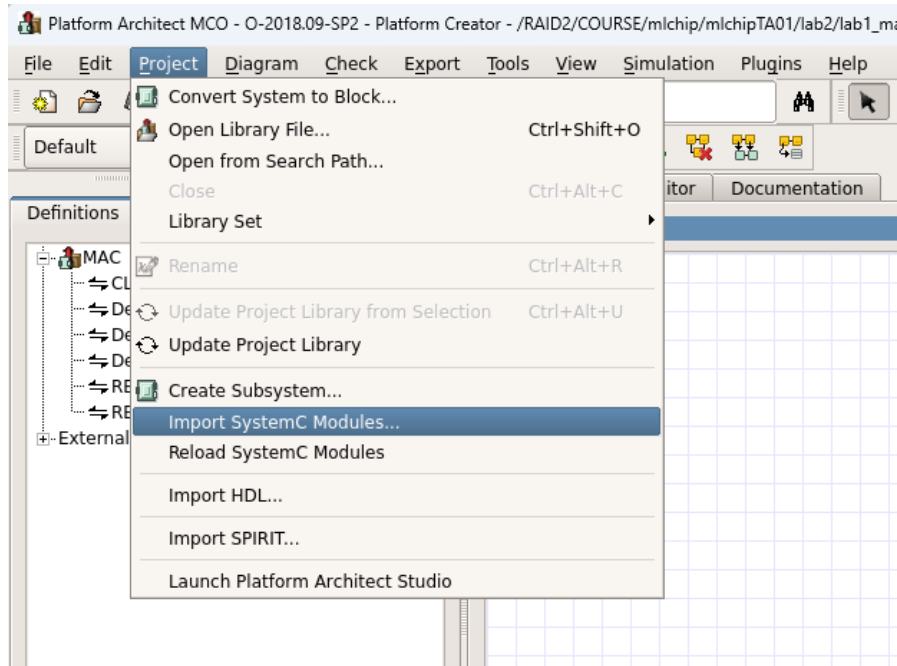
❖ General -> Use source files





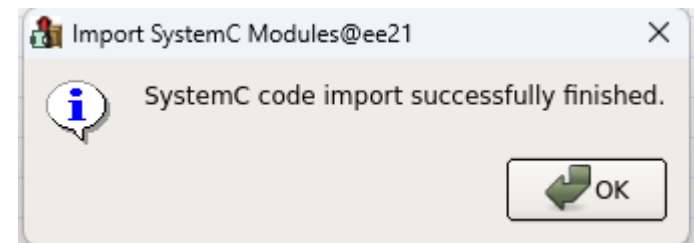
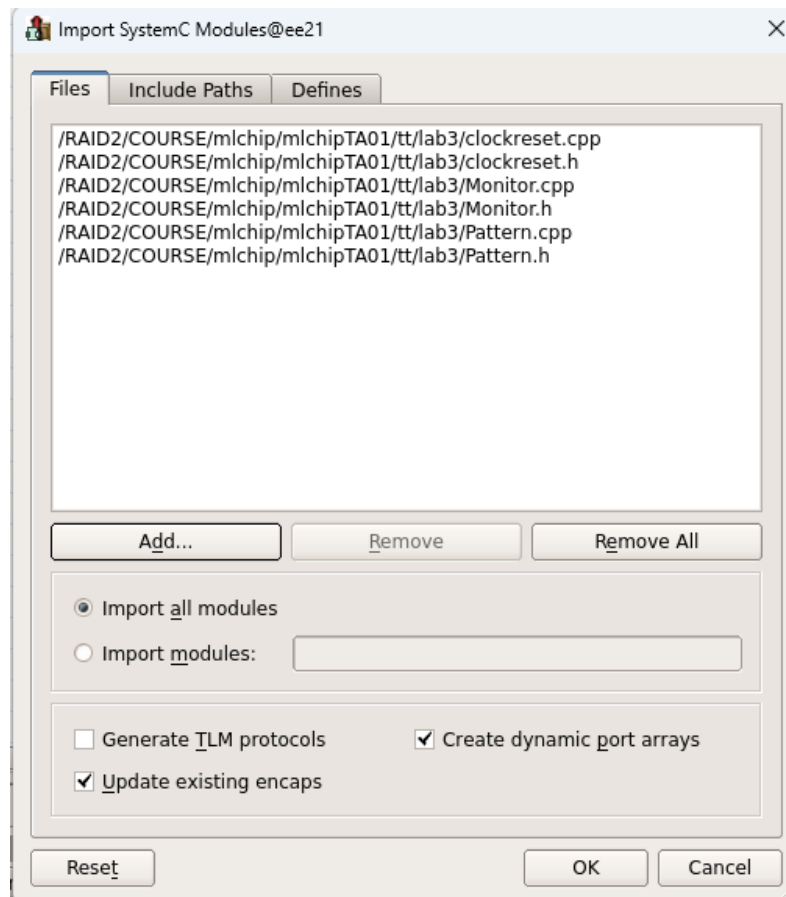
# Platform Architect

## ❖ Import SystemC Modules -> Add



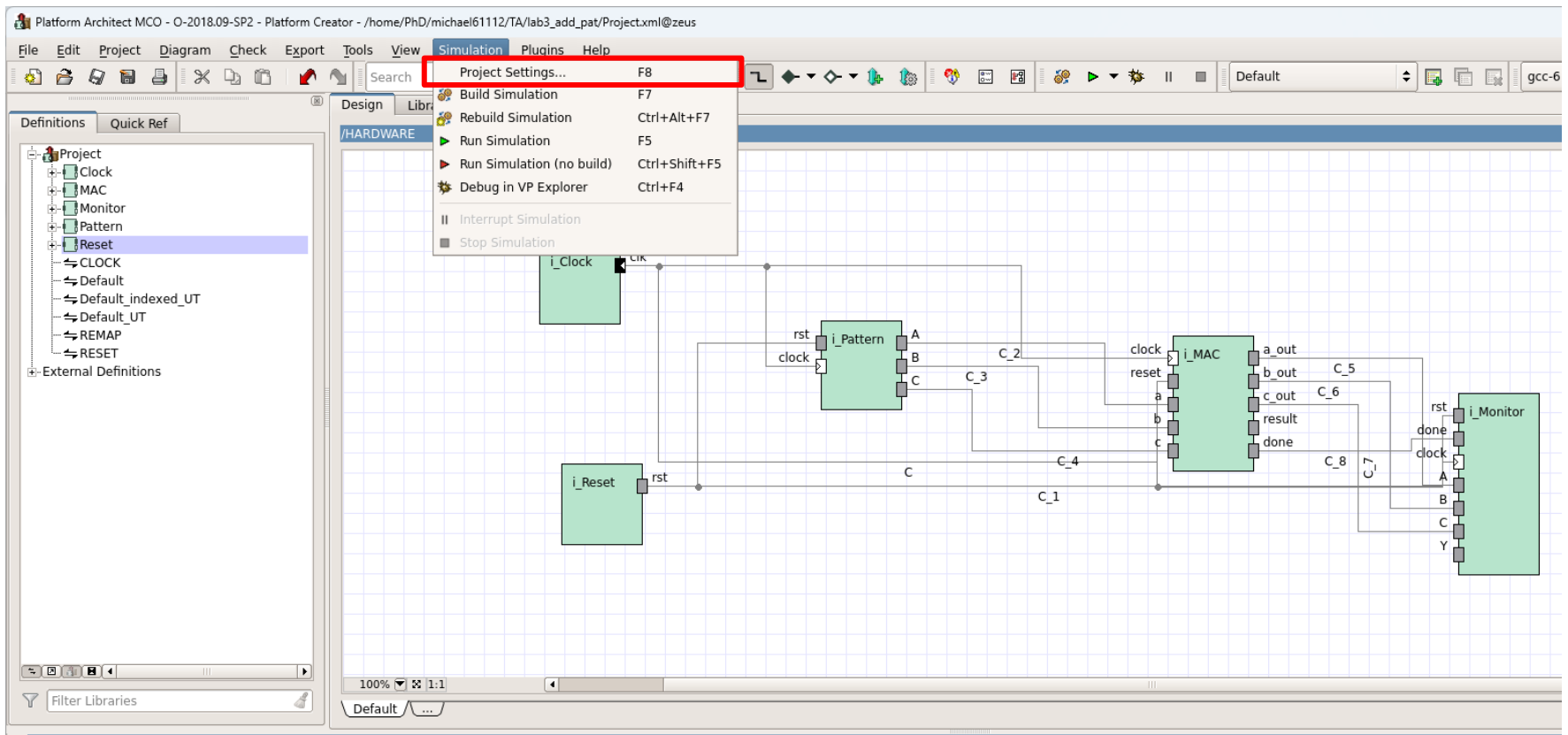
# Platform Architect

- ❖ Choose the source file -> OK



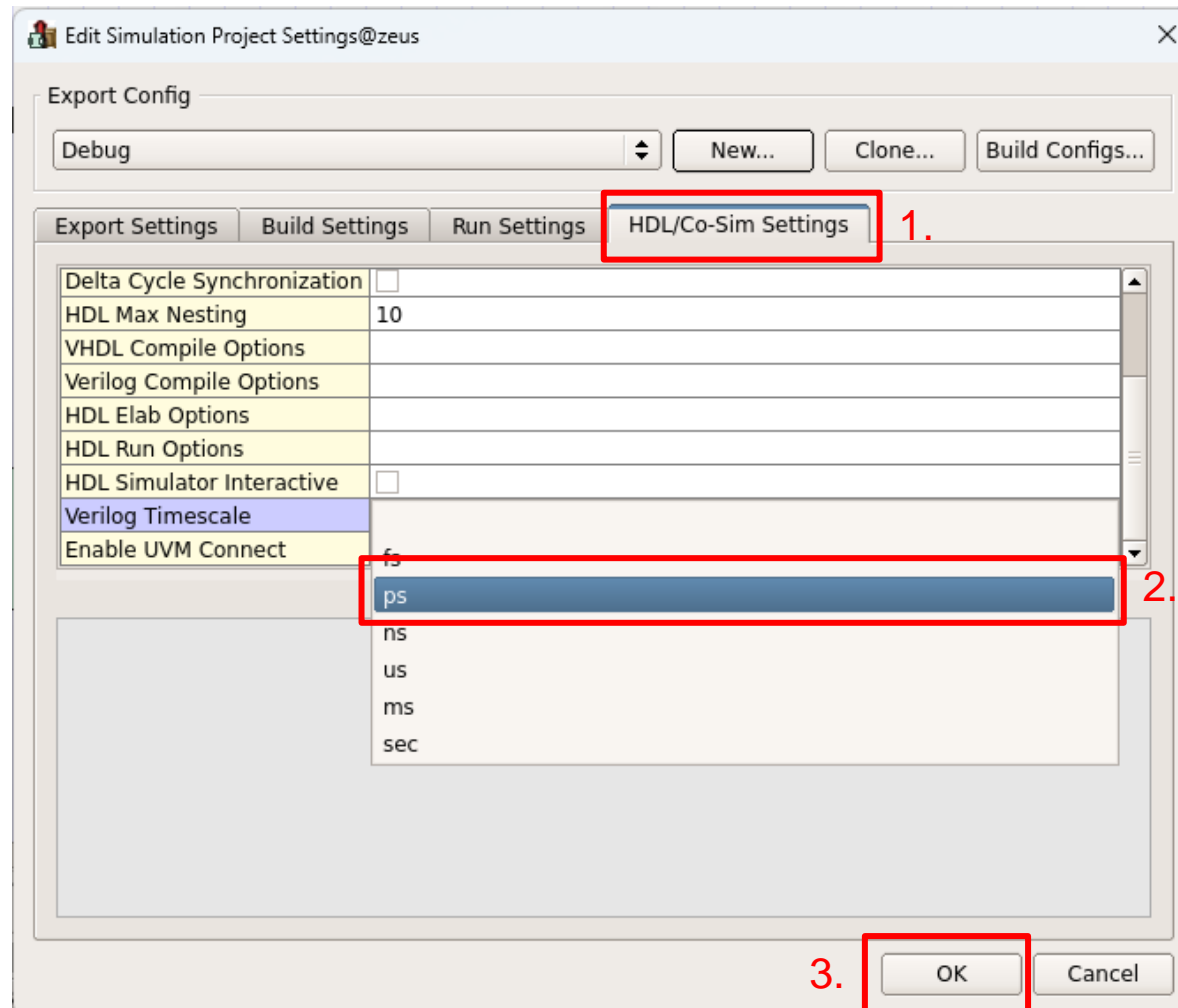
# Set Simulation Timescale (1/2)

## ❖ Simulation -> Project Settings...

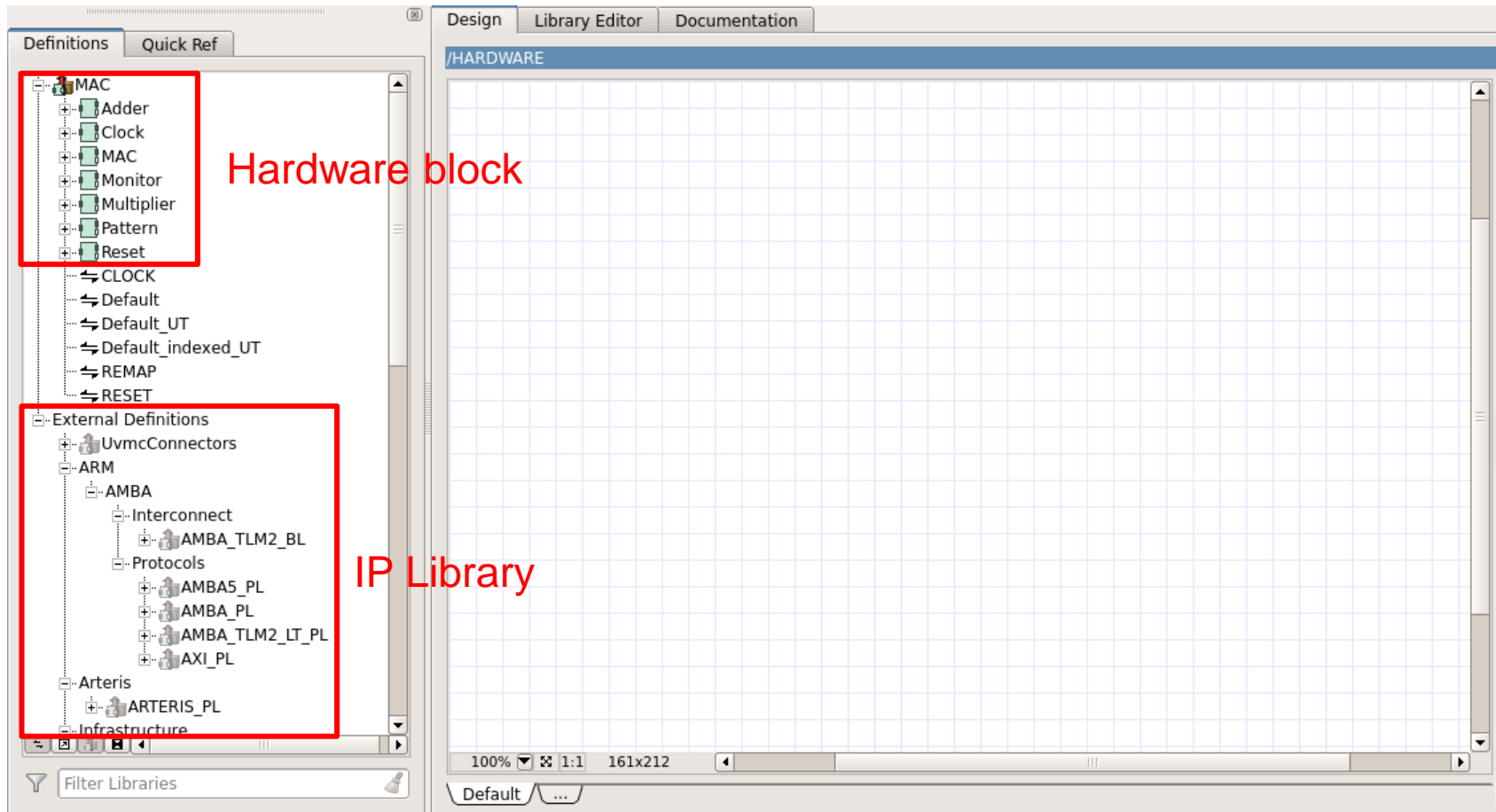




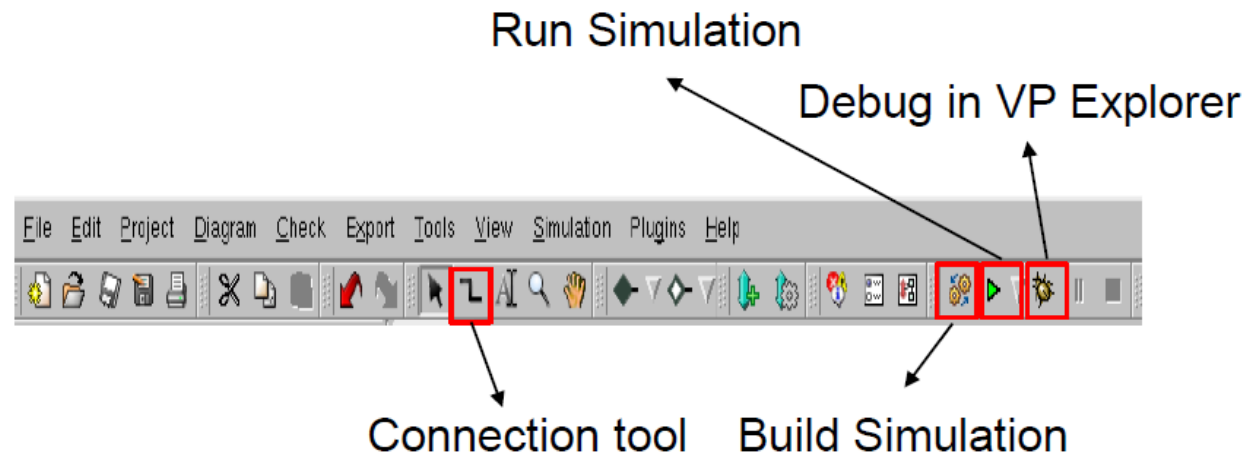
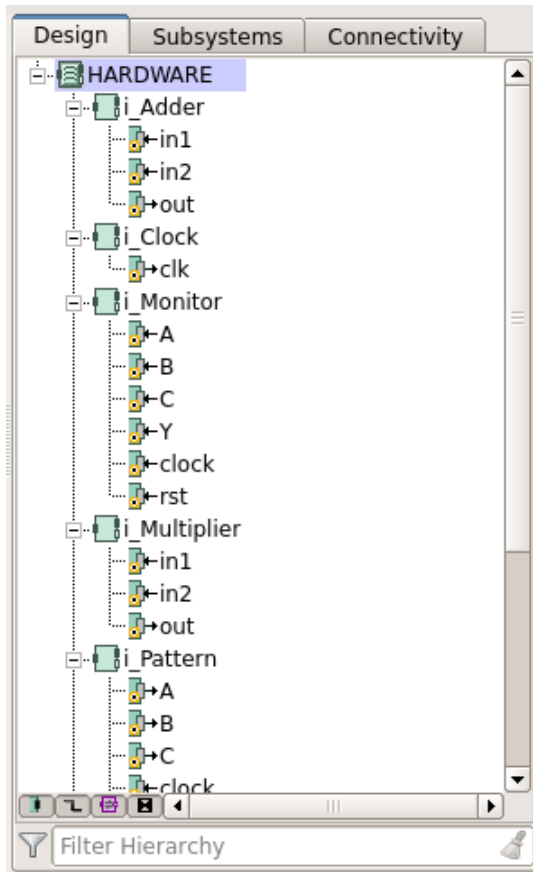
## Set Simulation Timescale (2/2)



# Platform Architect



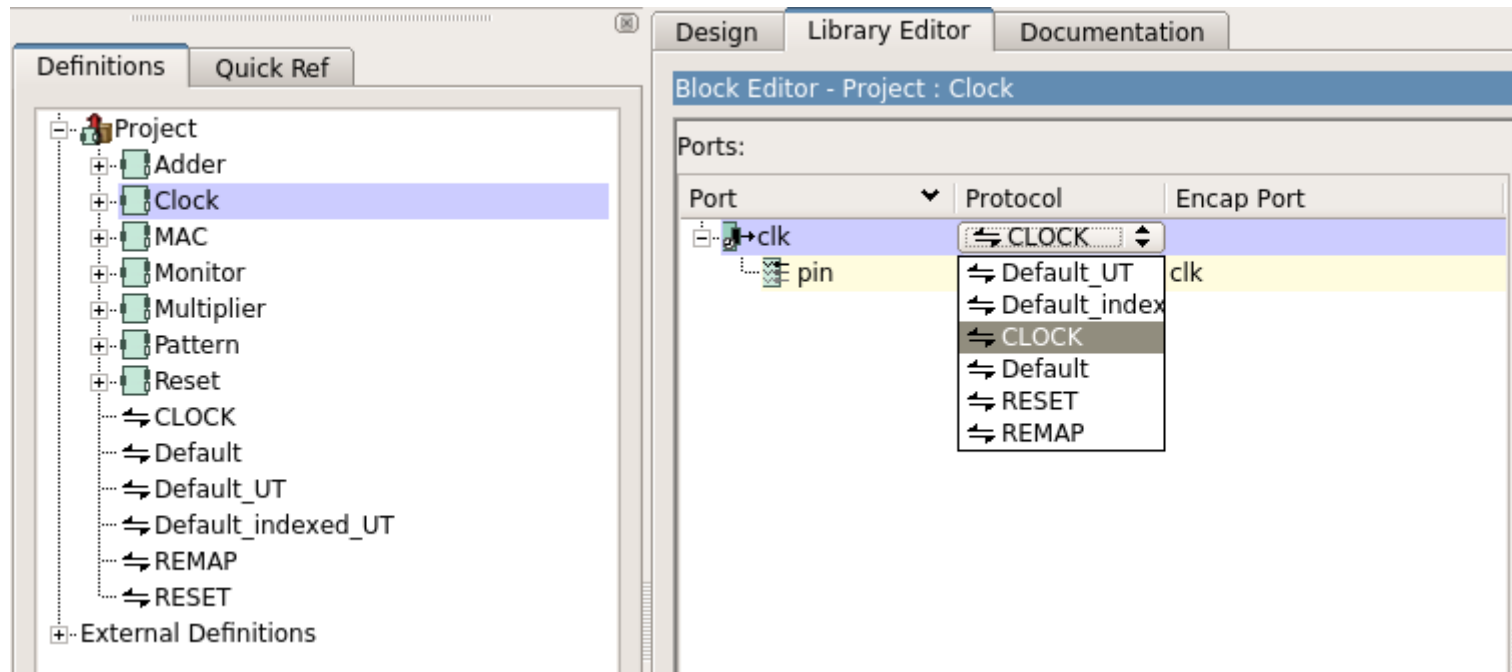
# Platform Architect





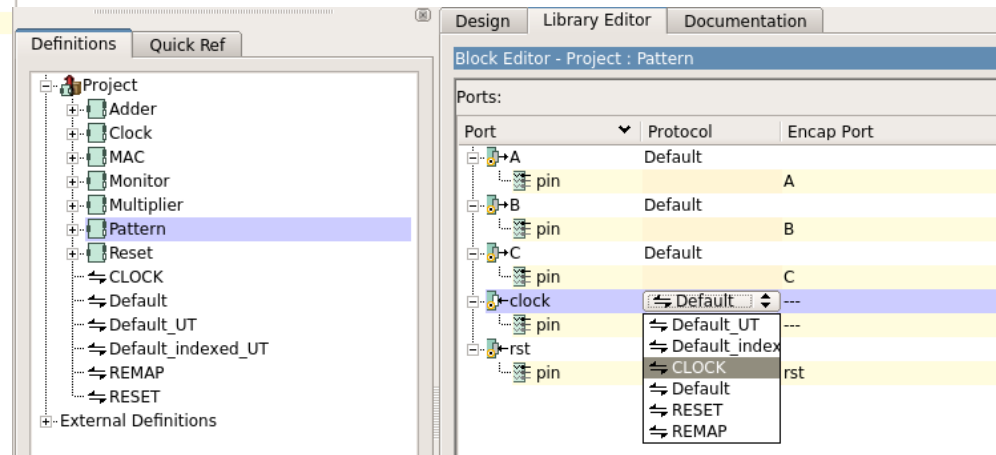
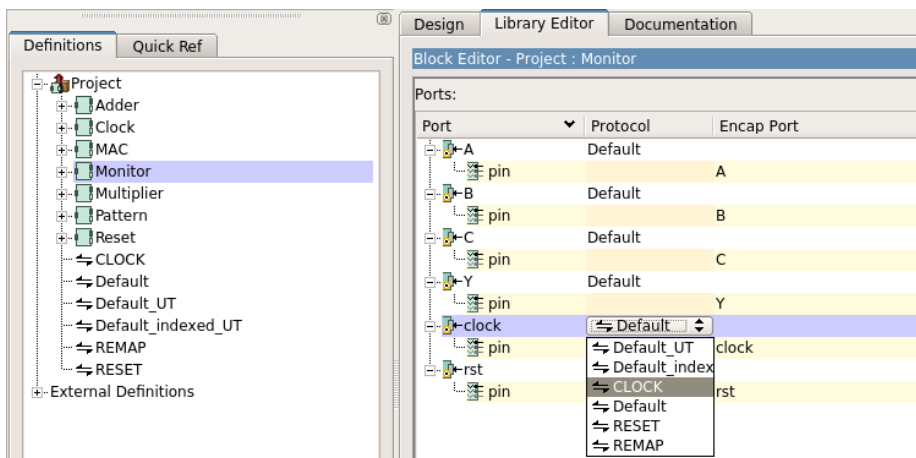
# Platform Architect

- ❖ Change protocol of clock port
- ❖ Double click Clock -> Click Default -> Choose CLOCK



# Platform Architect

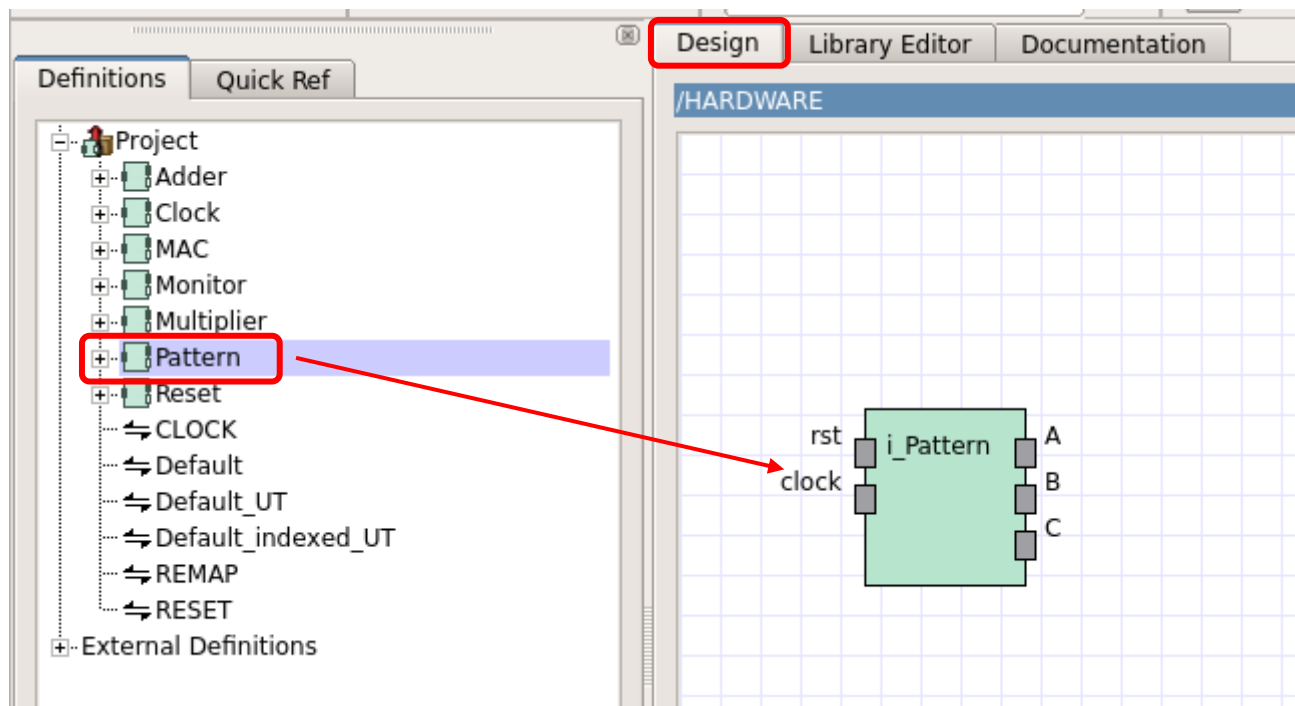
- ❖ Repeat the same action to change the clock protocol of Pattern and Monitor block





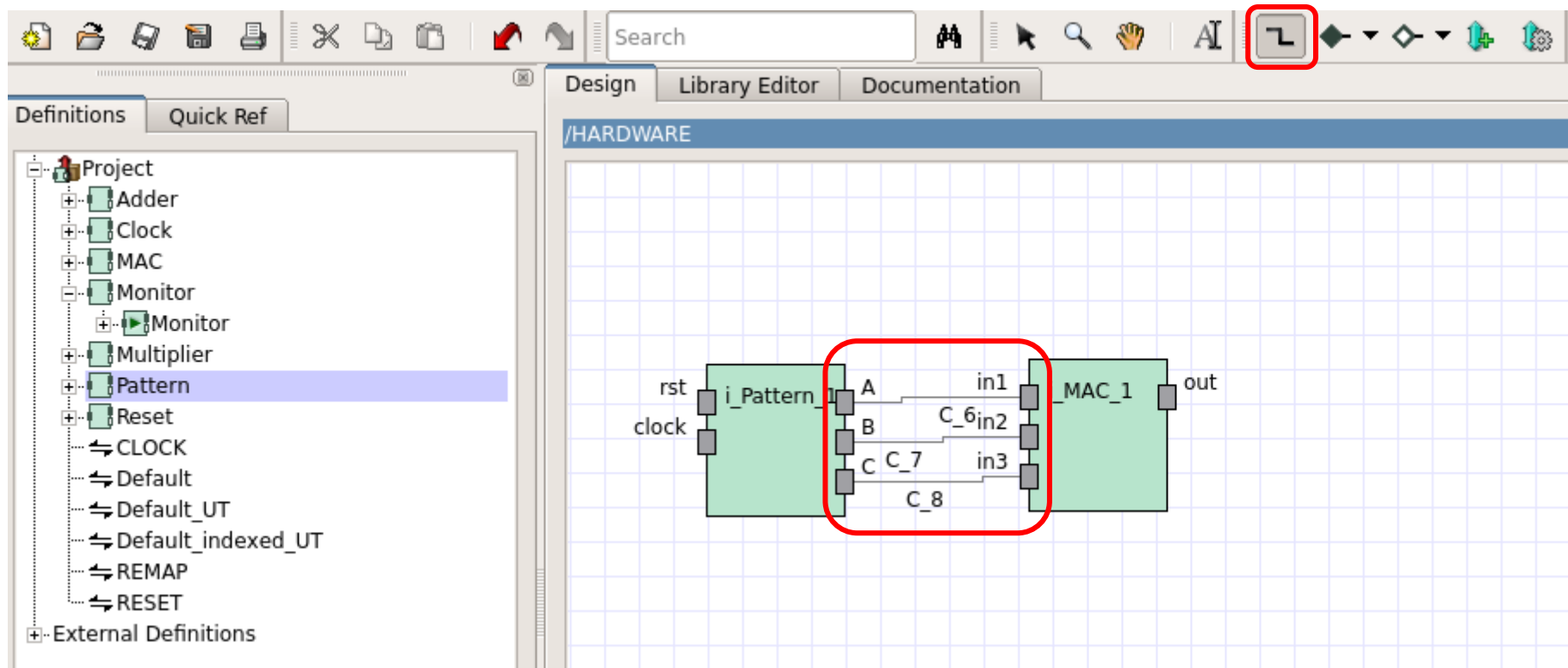
# Platform Architect

- ❖ Create the block
  - ❖ Click and drag to the design window



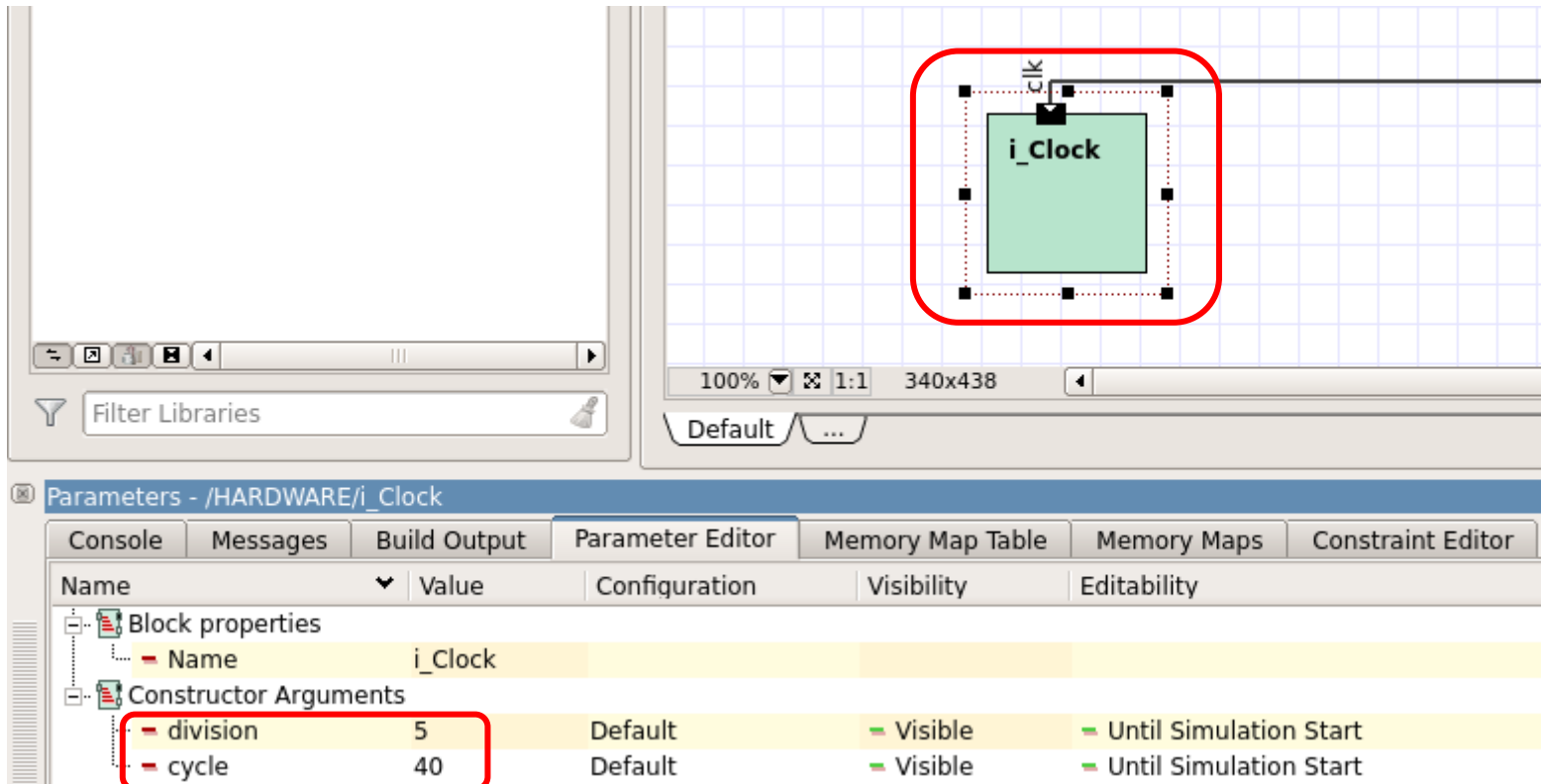
# Platform Architect

- ❖ Use connection tool to connect the block



# Platform Architect

- ❖ Click Clock block -> Set clock period
  - ❖ division -> 5
  - ❖ cycle -> 40



The screenshot displays the Platform Architect software interface. The top section shows a block diagram with a green block labeled "i\_Clock" on a grid. A red rounded rectangle highlights the "i\_Clock" block and its input port labeled "clk". Below the diagram is a toolbar with icons for zooming and a "Filter Libraries" search bar. The bottom section is the "Parameters - /HARDWARE/i\_Clock" panel, which includes tabs for Console, Messages, Build Output, Parameter Editor, Memory Map Table, Memory Maps, and Constraint Editor. The "Parameter Editor" tab is active, showing a table of parameters for the "i\_Clock" block.

Name	Value	Configuration	Visibility	Editability
<b>Block properties</b>				
Name	i_Clock			
<b>Constructor Arguments</b>				
division	5	Default	Visible	Until Simulation Start
cycle	40	Default	Visible	Until Simulation Start

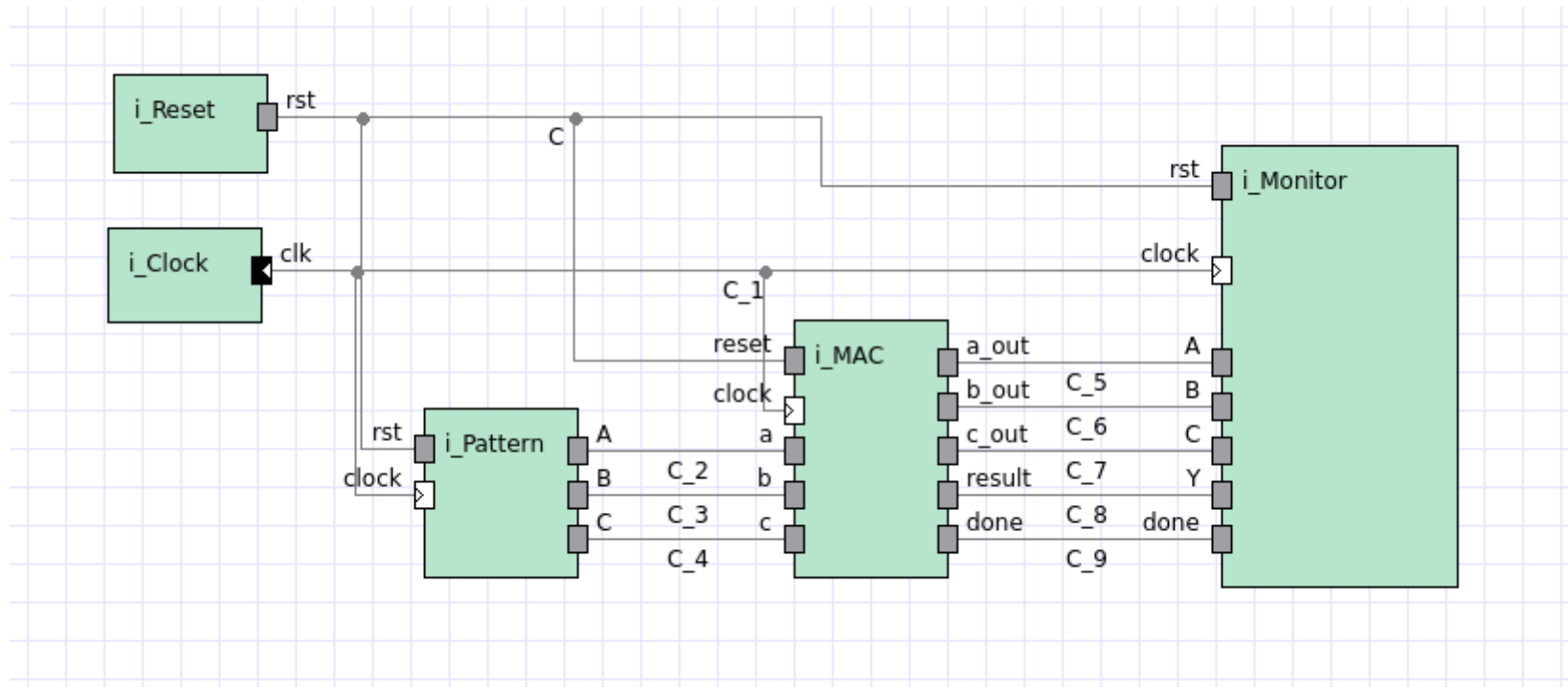


## Platform Architect

- ❖ Click Reset block -> Set reset period
  - ❖ `_ticks` -> 10

Parameters - /HARDWARE/i_Reset				
Name	Value	Configuration	Visibility	Editability
Block properties				
Name	i_Reset			
Constructor Arguments				
_ticks	10	Default	Visible	Until Simulation Start

# System Overview





# Run Simulation

```
Running Simulation
Project opened. Opening 'Debug' configuration
Info: [VCS_SAVE_RESTORE_INFO] ASLR (Address Space Layout Randomization) is de
Please use '-no_save' simv switch to avoid this.
Chronologic VCS simulator copyright 1991-2023
Contains Synopsys proprietary information.
Compiler version U-2023.03_Full64; Runtime version U-2023.03_Full64; May 21
Please enter ::scsh::c to continue
::scsh::c

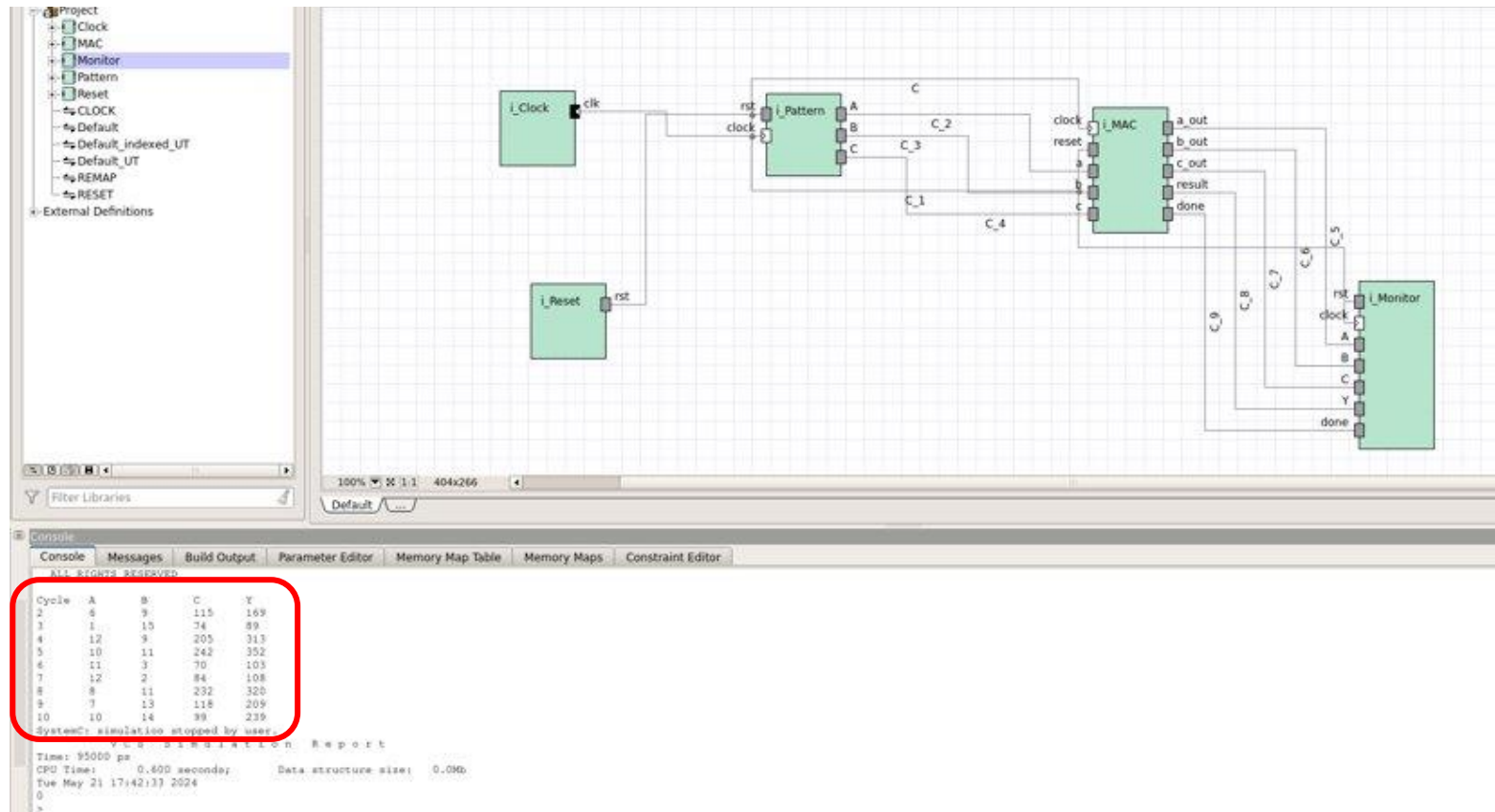
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and conditions of a written license agreement with Synopsys, Inc.
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SystemC 2.3.1 --- Dec 16 2019 20:18:59
Copyright 1996-2017 by all Contributors,
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Cycle  A      B      C      Y
2      6      9      115    169
3      1      15     74     89
4      12     9      205    313
5      10     11     242    352
6      11     3      70     103
7      12     2      84     108
8      8      11     232    320
9      7      13     118    209
10     10     14     99     239
SystemC: simulation stopped by user.
V C S   S i m u l a t i o n   R e p o r t
Time: 95000 ps
CPU Time:      0.600 seconds;      Data structure size:  0.0Mb
Tue May 21 17:42:33 2024
0
>
```

# Platform Architect

- ❖ Console
- ❖ Show the simulation result





## Lab Requirement

- ❖ Complete MAC unit.
  - ❖ Use Platform Architecture to simulate output result.
  - ❖ Upload screenshots of simulation results and module connection to E3@NYCU