# ML CHIP HW4

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# Mapping:

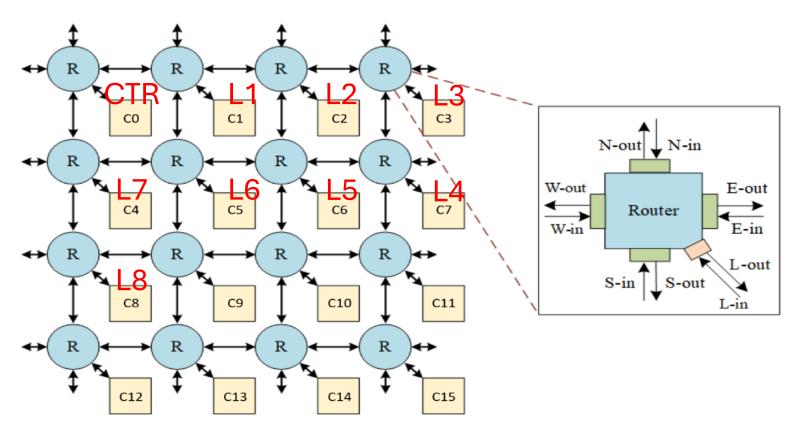
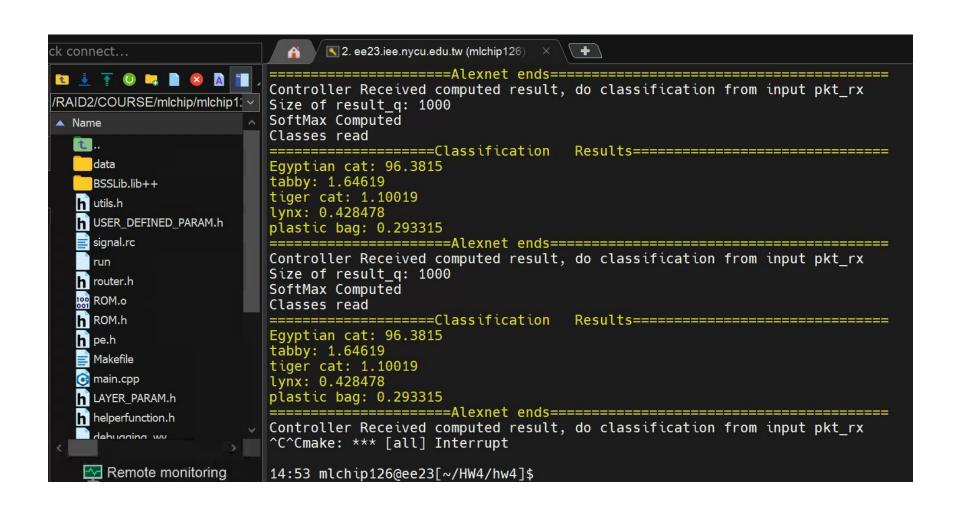


Figure 1. 4x4 mesh-based NoC architecture

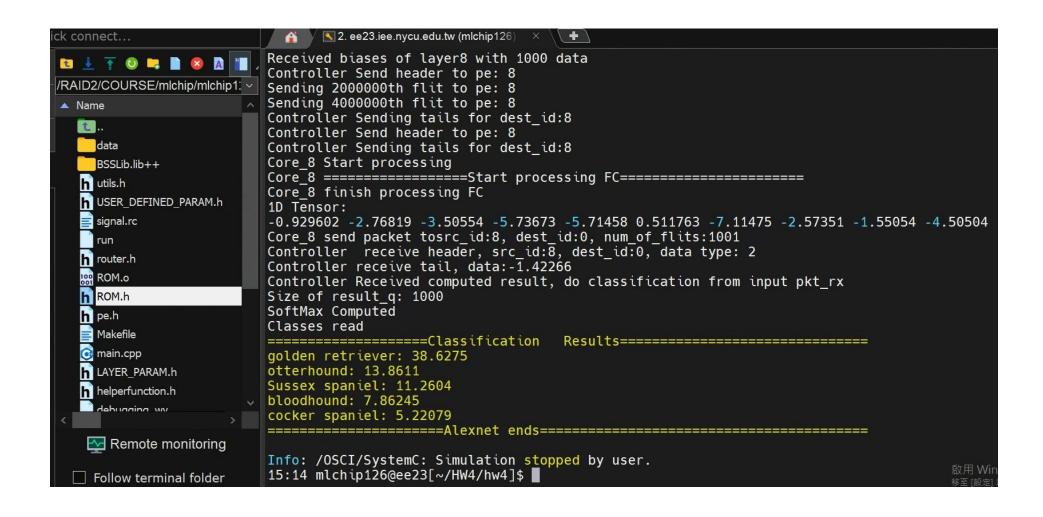
# Task of each layer

CTR	SEND WEIGHTS, BIAS	WAIT L8 RESULT	Softmax	Classification
L1	Assymetric Padding	CONV	RELU	MP
L2	CONV	RELU	MP	
L3	CONV	RELU		
L4	CONV	RELU		
L5	CONV	RELU	MP	
L6	FC	RELU		
L7	FC	RELU		
L8	FC			

#### Result(cat):



#### Result(dog):



### Simulation Specification:

- Routing algorithm: X-Y
- Scheme: Wormhole
- Implementation: Algorithmic
- Input buffer size: 1 flit
- Flow control:ACK-NACK
- Virtual Channel: Not used
- # of PE Used: 9, 1 for controller 8 for layers

#### Operations:

• Sends weights and biases to each need Pes then send input feature to the pe of first layer, after first layer finishes its calculation, send out the result of first layer to second layer, vice versa. Controller at the same time waits for the result of the last layer(PE8) which is the result of the fully connected layer8.

#### Remark:

- Requires tons of time to send the weights and biases, especially weights for fully connected layer. 9216x4096 datas needed to be sent from Controller to PE.
- To speedup the simulation process, waveform generation should be turned off, release the unneeded tensor memory also adding flags -03 to the C++ compiler directive in the Makefile is also useful.

```
all:

g++ -03 - I · · - I · $(INC_DIR) - L · · - L · $(LIB_DIR) - o · $(0) · $(C) · $(LIB) · $(RPATH)

./run
```

 Spyder IDE with Python code of AlexNet can aids the debugging process for each layer result