# 2D Discrete Wavelet transform design on ZYNQ

SOC System On Chip Lab

Final Project Proposal

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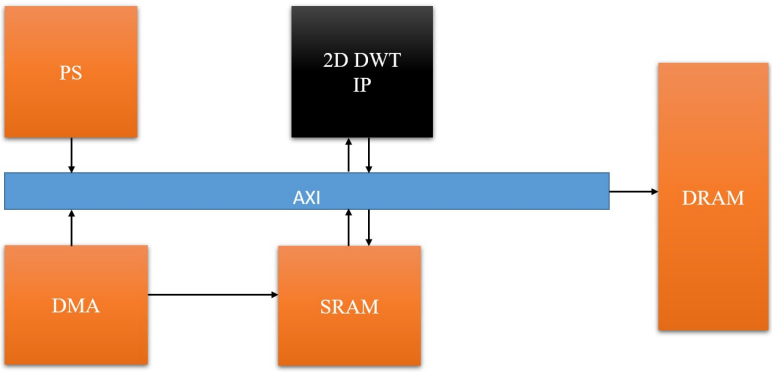
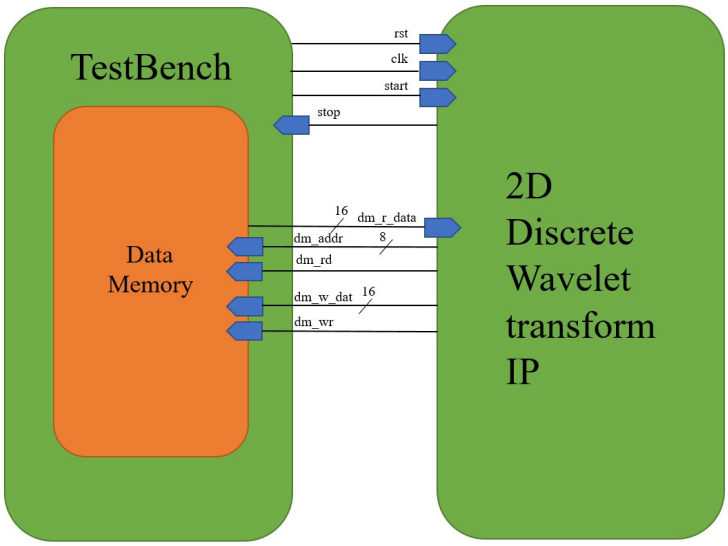
# I. System Diagram

## Main system diagram




- I plan to design a 2D-DWT IP utilizing the Systolic array architecture on to the ZYNQ board. The data flow would be controlled by the PS. Data extracted from DRAM using AXI DMA to On-Chip SRAM, later PS would send the data stream into the main IP block for signal processing. After processing the image, it would be write back to the DRAM.

# II. System Specifications




| Signal Name | Directio n | Width(bit) | description |
|---|---|---|---|
| rst | Input | 1 | 非同步系統重置訊號。當此訊號為1時表示系統重置。 |
| clk | Input | 1 | 系統時脈訊號。 |
| start | Input | 1 | 資料有效信號。當此訊號為1時表示輸入資料為有效。 |
| stop | Output | 1 | 程式處理完成終止信號 |
| dm_r_dat | Input | 16 | 指令讀取資料 |
| dm_addr | Output | 8 | 指令記憶體位置訊號 |
| dm_w_dat | Output | 16 | 資料寫入訊號 |
| dm_wr | Output | 8 | 資料寫入位置訊號 |

- The planned IP block before connecting to the AXI stream, I would first develop an 2D DWT IP block and test it using testbenches, later try to connect the I/O port onto the ZYNQ AXI interfaces.

Goal

- Being able to successfuly connect the IP onto the AXI interface and run full system integration.
- Being able to run real-time DWT processing with minimum area, high speed and high hardware ultilization efficiency.
- Show the result onto onto VGA through the I/O interface of ZYNQ.

# III. References

[1] T. C. Denk and K. K. Parhi, "Systolic VLSI architectures for 1-D discrete wavelet transforms," Conference Record of Thirty-Second Asilomar Conference on Signals, Systems and Computers (Cat. No.98CH36284), Pacific Grove, CA, USA, 1998, pp. 1220-1224 vol.2, doi: 10.1109/ACSSC.1998.751521.

[2] VLSI DIGITAL SIGNAL PROCESSING SYSTEMS DESIGN AND IMPLEMENTATION, CH7 Systolic Archtiecture design, exercises 14, Prof. Keshab Parhi, p219

[3] ZYNQ Training Playlist for AXI stream, Mohammad S. Sadri, 2014

[4] Computer Architecture - Lecture 27: Systolic Arrays (ETH Zürich, Fall 2020), Prof. Onur Mutlu