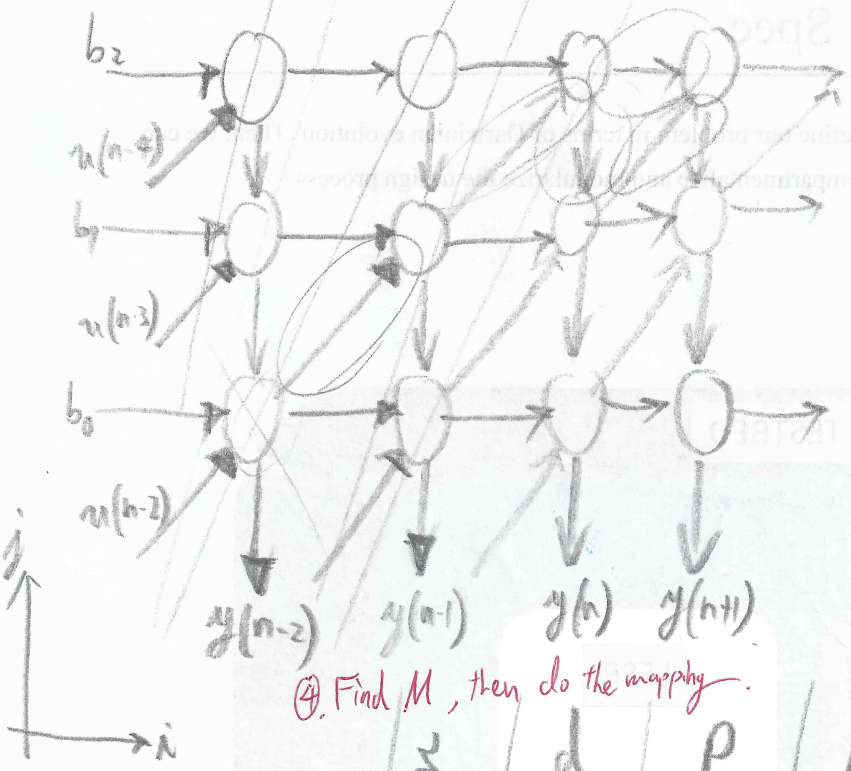
c)

① Derive the DG.



② find suitable $\vec{s}$, $\vec{d}$, s.t. $\langle \vec{s}, \vec{d} \rangle \neq 0$

let $\vec{s} = \begin{pmatrix} 1 \\ 2 \end{pmatrix}$, $\vec{d} = \begin{pmatrix} 1 \\ 0 \end{pmatrix}$

$\langle \vec{s}, \vec{d} \rangle = 1 \neq 0$ ✓

③ Check $\forall e \in DG$, $\langle \vec{s}, e \rangle \geq 0$.

$\langle \vec{s}, e \rangle = -2 \times \leq 0$

Try $\vec{s} = \begin{pmatrix} 2 \\ -1 \end{pmatrix}$, $\vec{d} = \begin{pmatrix} 1 \\ 0 \end{pmatrix}$, $e = \begin{pmatrix} 0 \\ -1 \end{pmatrix}$

$\langle \vec{s}, \vec{d} \rangle = 2 \neq 0$ ✓

$\langle \vec{s}, y \rangle = 1 \geq 0$ ✓

$\langle \vec{s}, u \rangle = 1 \geq 0$ ✓ , i.e. $\langle \vec{s}, e \rangle \geq 0, \forall e$

$\langle \vec{s}, b \rangle = 2 \geq 0$ ✓

④ Find M, then do the mapping.

$\vec{s}$	$\vec{d}$	P	M	$y = \begin{pmatrix} 0 \\ -1 \end{pmatrix}$	$u = \begin{pmatrix} 1 \\ 1 \end{pmatrix}$	$b = \begin{pmatrix} 1 \\ 0 \end{pmatrix}$
$\begin{pmatrix} 2 \\ -1 \end{pmatrix}$	$\begin{pmatrix} 1 \\ 0 \end{pmatrix}$	$\begin{pmatrix} 0 \\ 1 \end{pmatrix}$	$\begin{pmatrix} 2 & -1 \\ 0 & 1 \end{pmatrix}$	$\begin{pmatrix} 1 \\ -1 \end{pmatrix}$	$\begin{pmatrix} 1 \\ 1 \end{pmatrix}$	$\begin{pmatrix} 2 \\ 0 \end{pmatrix}$

c.

Pipeline ⑤ from mapping Result, (② → Delay, ① → Processor Index) derive the systolic High level design.