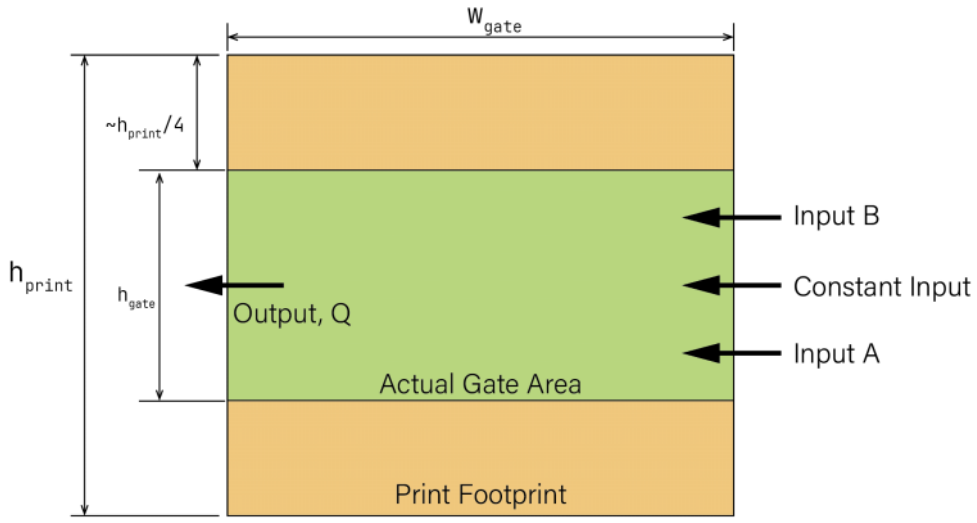
Notes for Design Synthesis

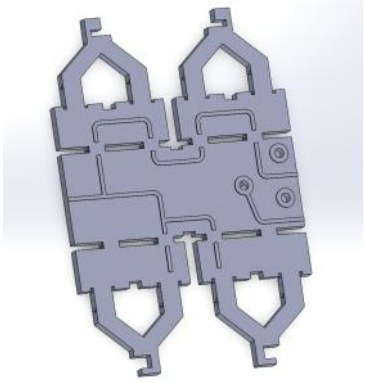
Friday, September 5, 2025 1:13 AM

Single-Function Logic Gates



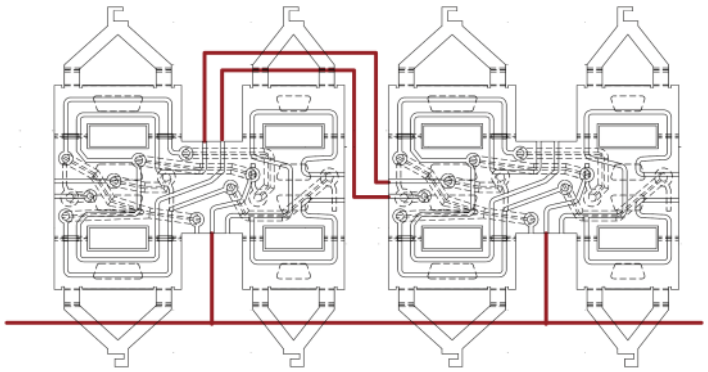
Footprint

Example of a logic gate printed in the "flattened" form, which occupies the print footprint:

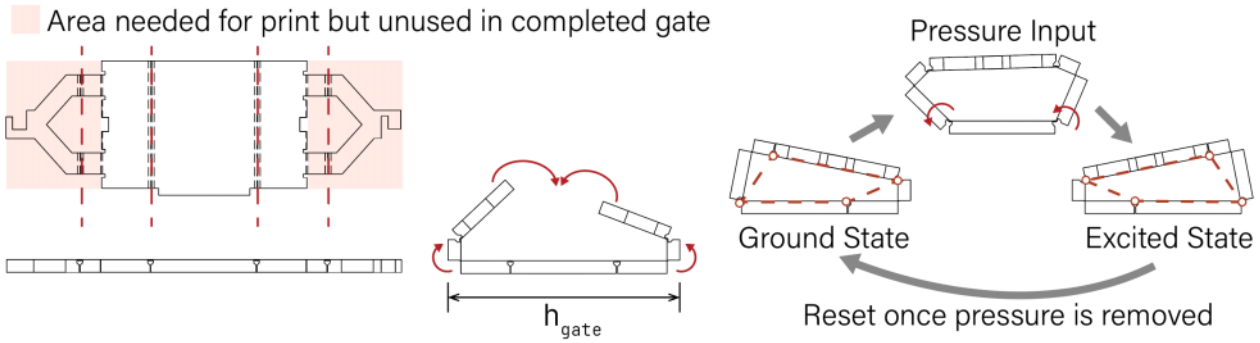


After pneumatic channels are added to the printed structure, the prints are folded to form a set of two 4-bar mechanism. Each 4-bar mechanism changes between two states under actuation and occupies half of the actual gate area above.

We may consider utilizing the bottom side of the print-only area for wire routing, e.g.



Let's take the footprint of a basic logic gate as an area of 1. For larger footprints, assume the gates will have a larger w_gate by the area factor.



The change in dimension when the gate is folded up creates an empty area that we might want to utilize in the future.

I/O

Each gate has the sequence of inlet/outlets (equivalent of leads of an electronic component) listed in the illustration above

Functions

The following logic gates can be produced with the above gate design (and the truth table here for convenience). A high signal "1" is a pressure input and "0" indicates ambient pressure

Gate	Area Factor	Truth Table
AND	1	A B Q 1 1 1 1 0 0 0 1 0 0 0 0
OR	1	A B Q 1 1 1 1 0 1 0 1 1 0 0 0
NAND	1	A B Q 1 1 0 1 0 1 0 1 1 0 0 1
NOR	1	A B Q 1 1 0 1 0 0 0 1 0 0 0 1
XNOR	1.5	A B Q 1 1 1 1 0 0 0 1 0

		0	0	1
XOR	1.5	A	B	Q
		1	1	0
		1	0	1
		0	1	1
		0	0	0

Operations that are not commutative, i.e., the output depends on whether the input occurs at A or B, is also possible.

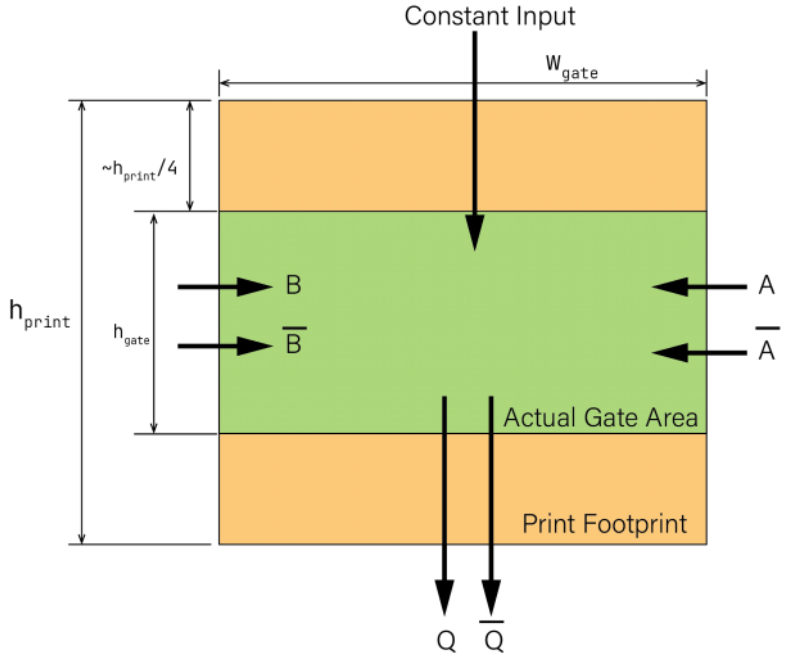
Note XOR/XNOR operation requires more footprint to complete.

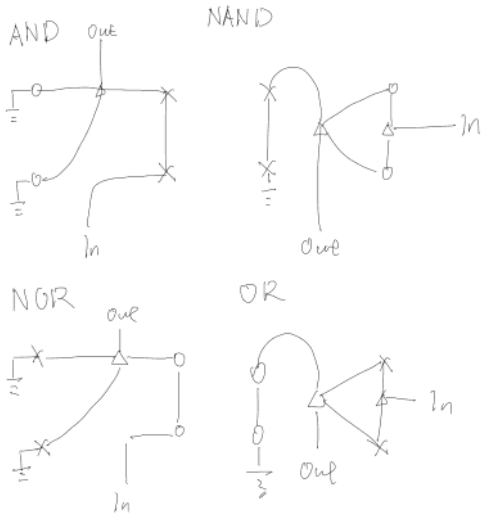
Multi-Function Logic Gates

Area factor: 1.5

The mono-stable behavior (i.e., the state of the) requires some energy storage element that releases strain energy to resets the gate once the actuating pressure is removed. Due to the characteristics of elastomeric elements this is usually much slower than the forward motion driven by pressure (~100-200ms vs ~1s). This motivates using pressure input for both paths between the ground/excited state, to have a sharp response but comes with the cost of supplying both the signal and its complement.

The gate will therefore take (A, A), (B, B) and output (Q, Q).

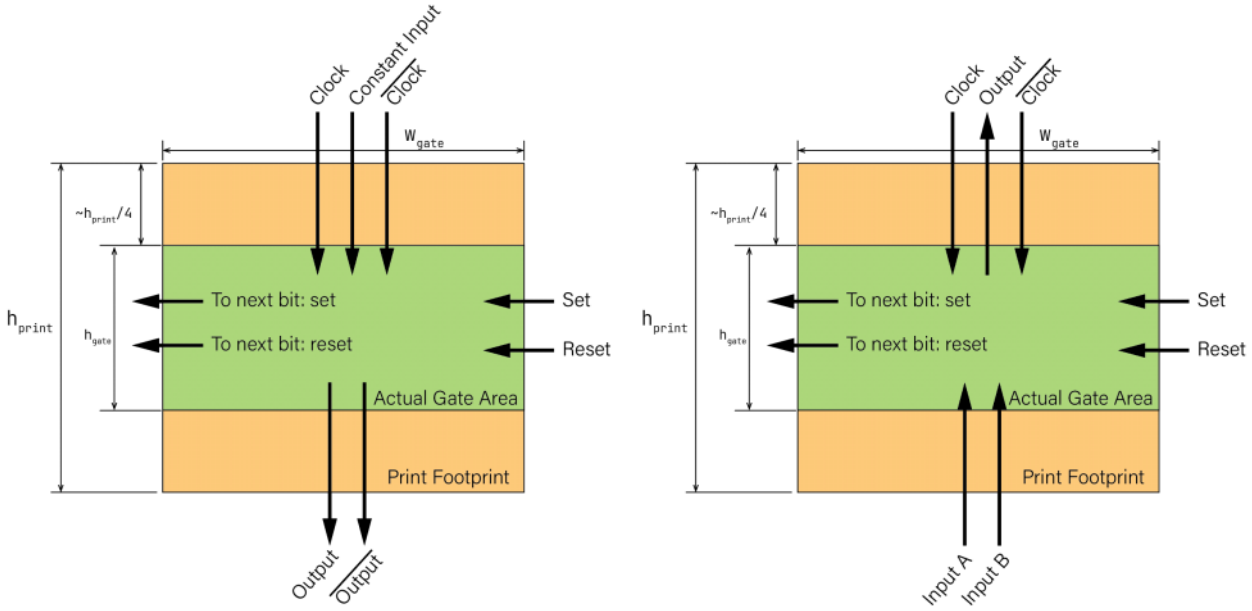




Having Q and Q requires a logic gate and its complement to be built superposed on the same footprint. This implies superposing the AND and OR topology on the same footprint. By selecting which port to be *the* input/ *the* output and its complement for A, B, and Q, we can toggle between the basic logic functions (AND through NOR in the table above) for the same gate.

(Will have more on this later)

(Non-volatile)Memory Units



Area factor: 1.5

Shift register passes down information one bit at a time at each clock cycle.

There are two configurations with the shift register: outputting "1, 0" or "0, 1", or choose from two input signals based on the state of the bit