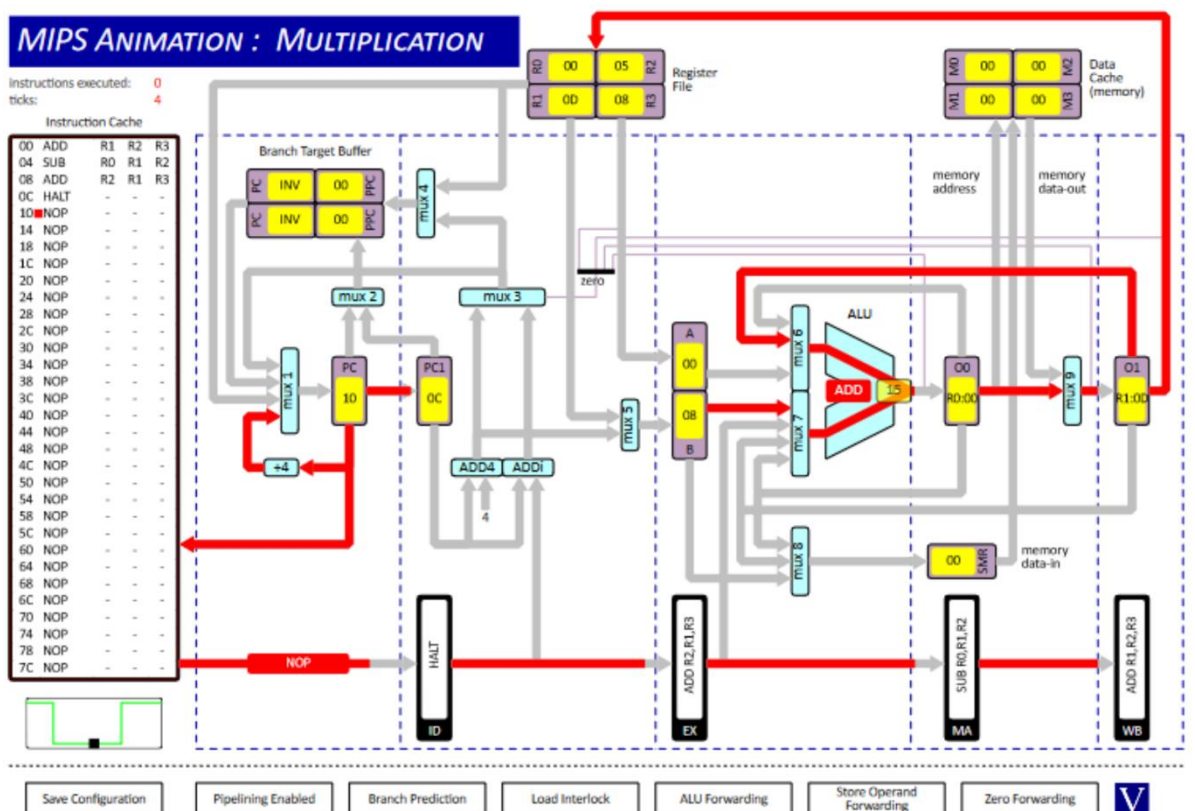
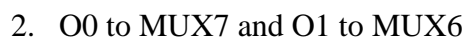
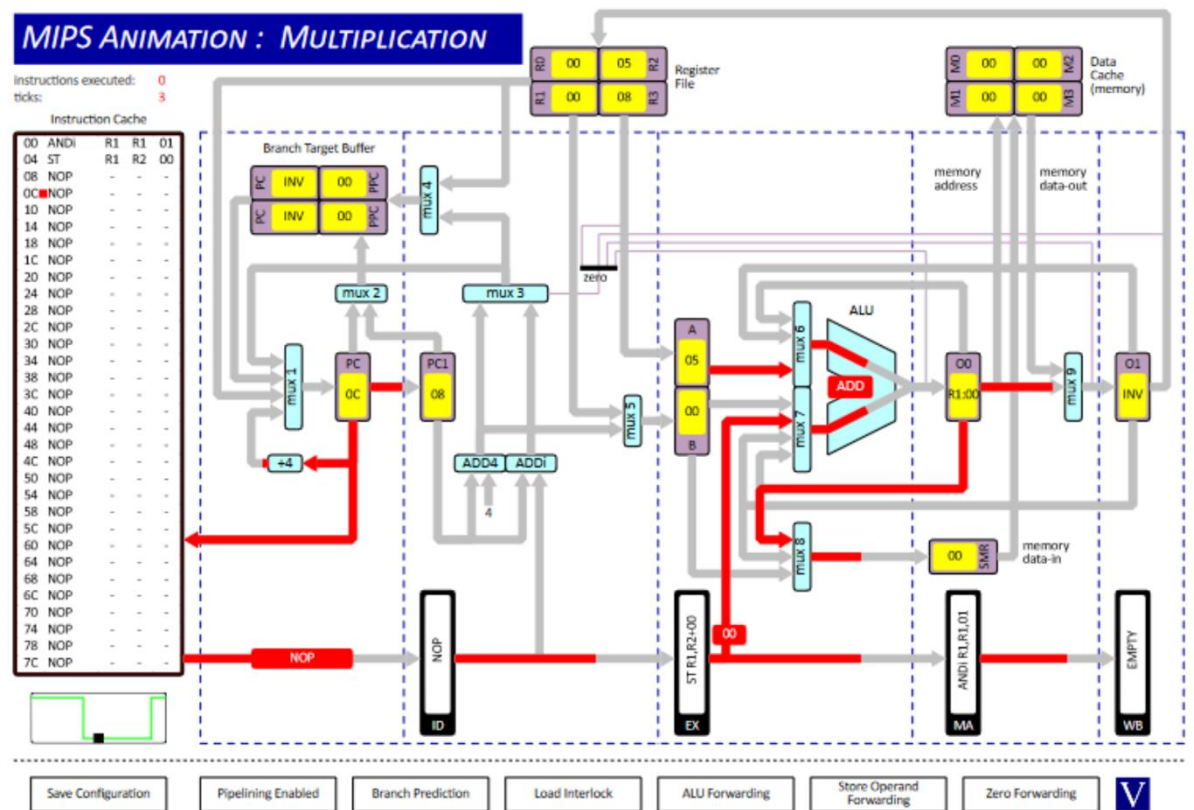


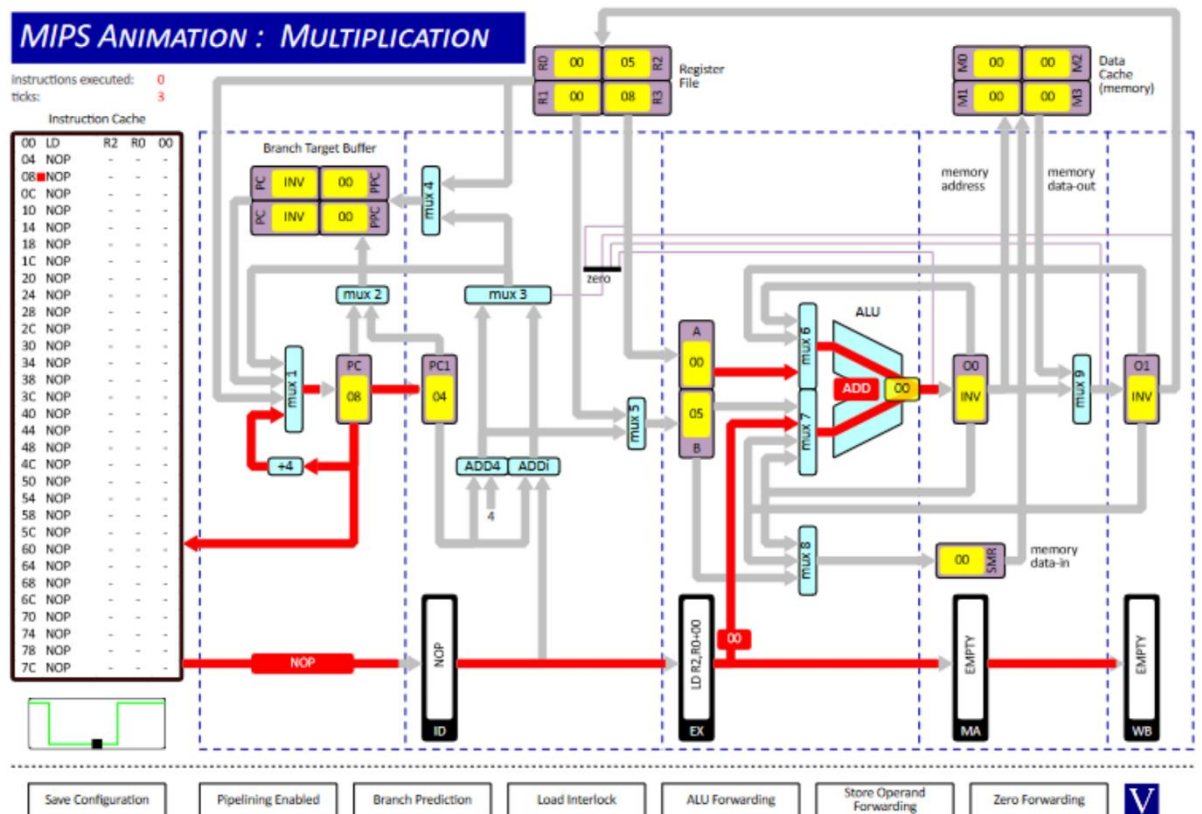
1. O1 to MUX6



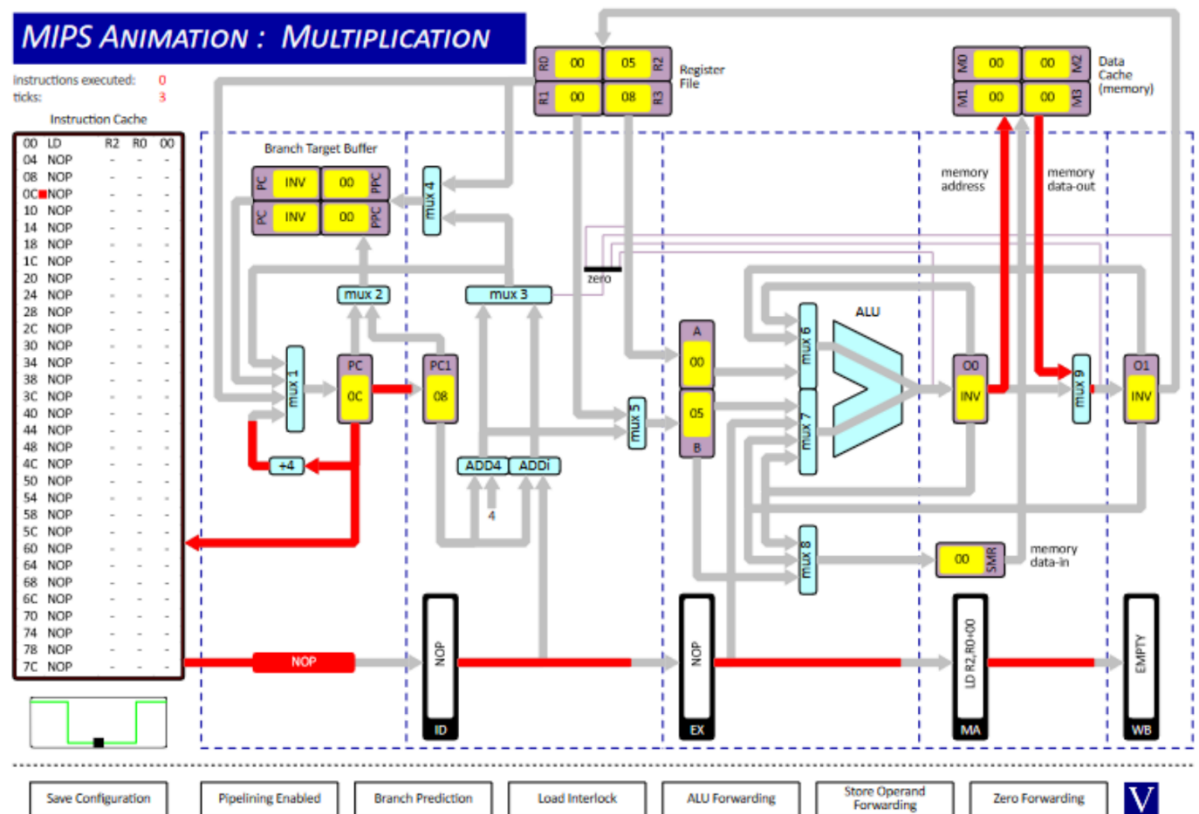
3. O0 to MUX8



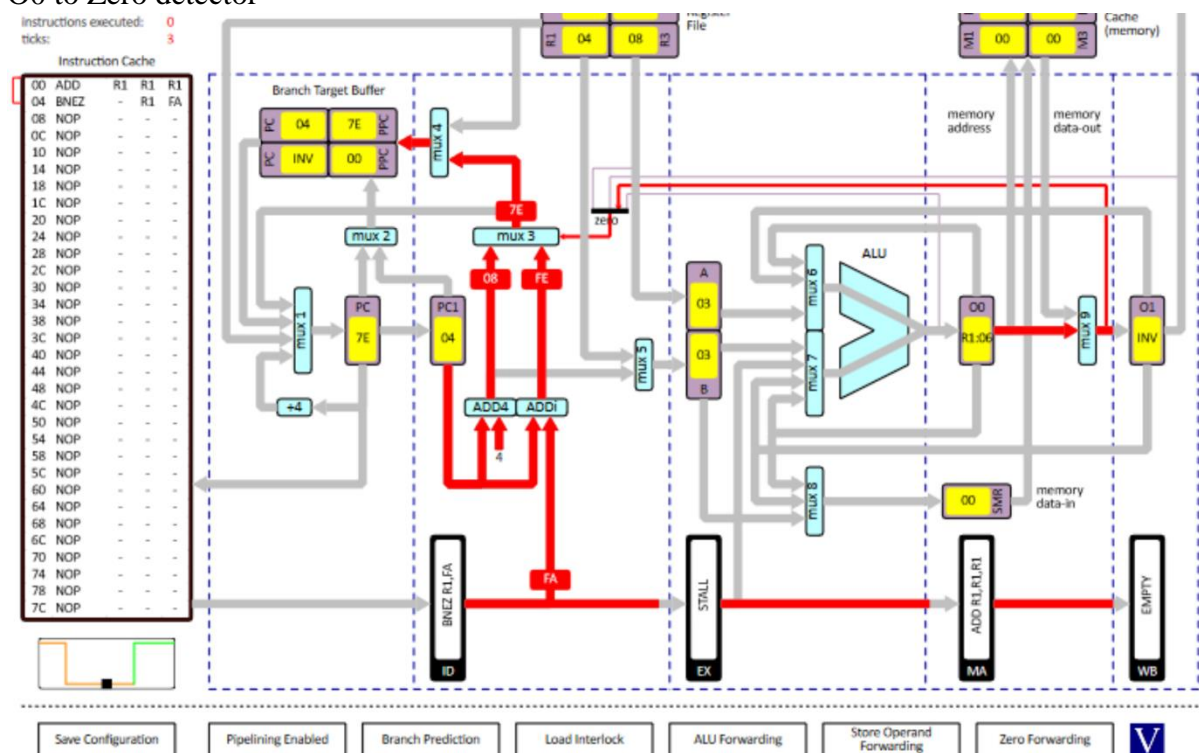
4. EX to MUX7



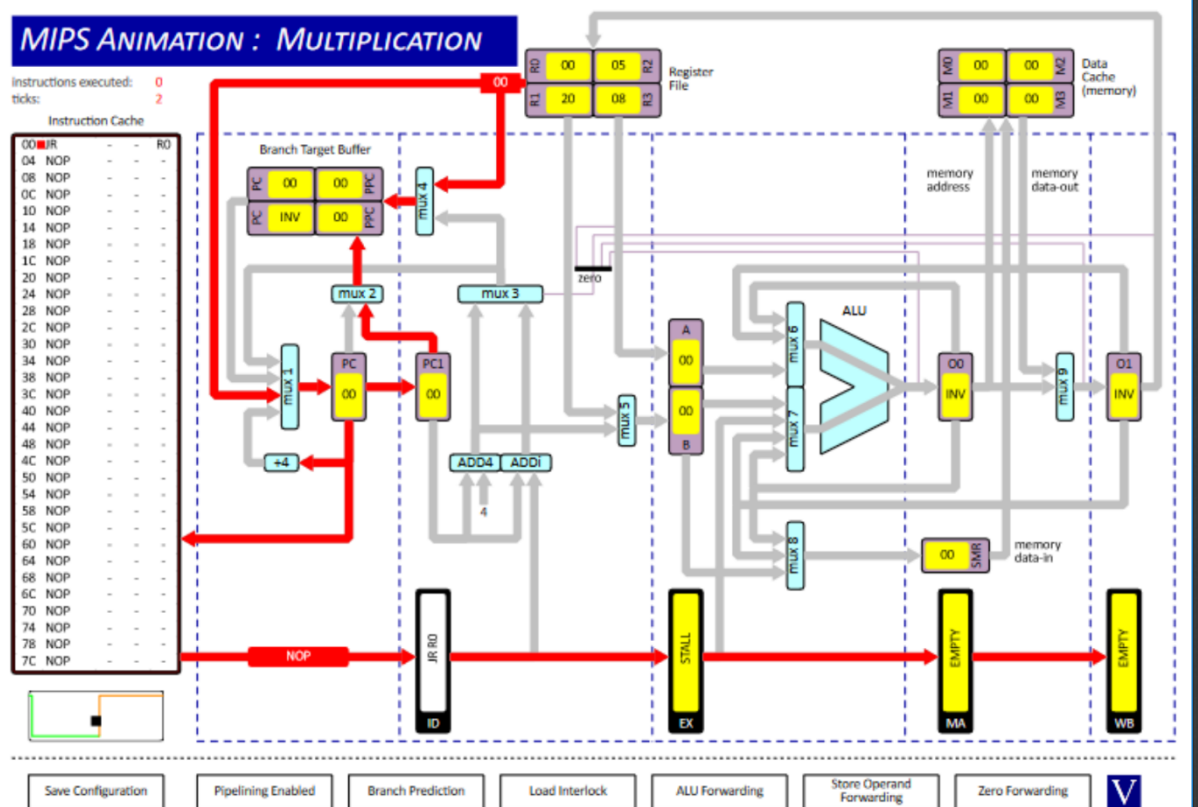
5. Data cache to MUX9



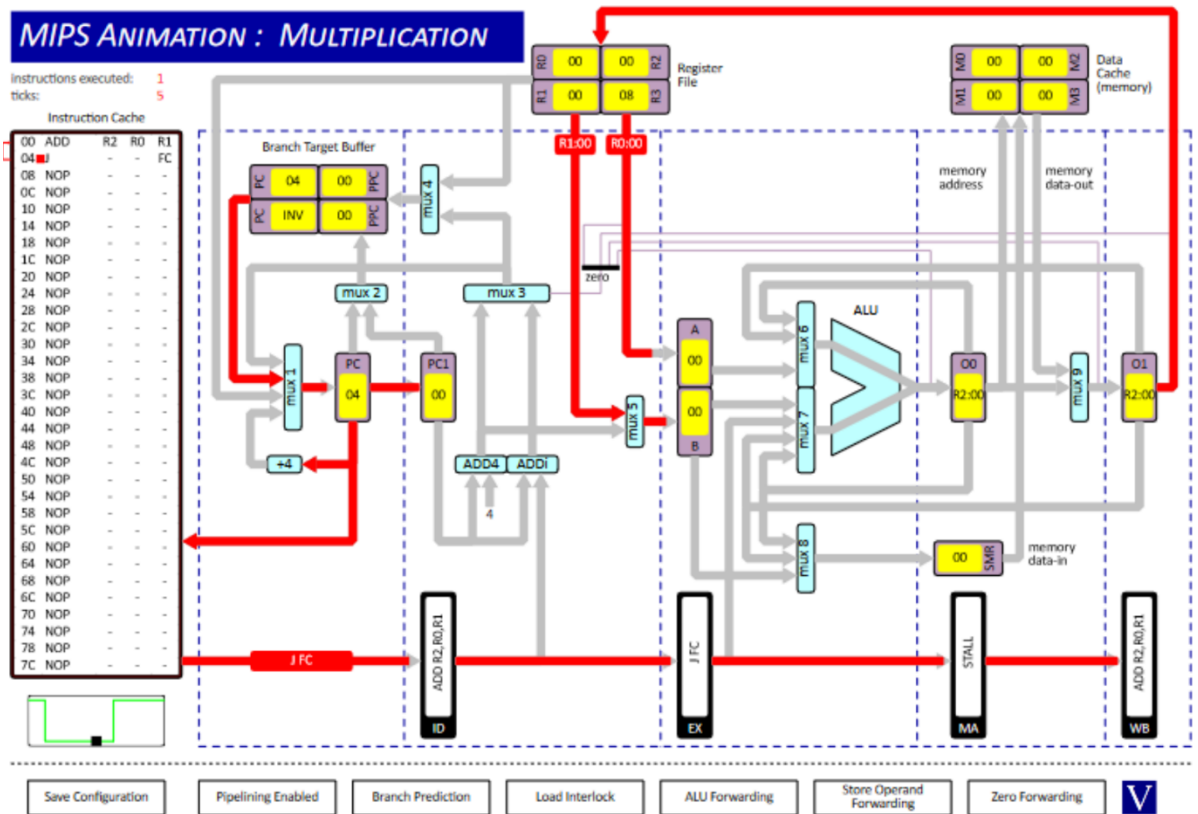
6. O0 to Zero detector



7. Register File to MUX1



8. Branch Target Buffer to MUX1



Q2.

- i) Clock cycles with ALU Forwarding Enabled = 10
Result of r1 = 15



- ii) Clock cycles with Interlocks = 18
Result of r1 = 15



- iii) Clock cycles with No ALU Interlock = 10
Result of r1 = 6



Q3.

- i) Clock cycles until halt = 51
Instructions executed = 39

Instructions executed: 39
ticks: 51

Instruction Cache

00	XOR	R1	R1	R1
04	BEQZ	-	R2	24
08	ST	R2	R0	00
0C	ANDI	R2	R2	01
10	BEQZ	-	R2	08
14	ADD	R1	R1	R3
18	LD	R2	R0	00
1C	SRLI	R2	R2	01
20	SLLI	R3	R3	01
24	J	-	-	E0
28	ST	R1	R0	00
2C	HALT	-	-	-
30	NOP	-	-	-
34	NOP	-	-	-
38	NOP	-	-	-
3C	NOP	-	-	-
40	NOP	-	-	-

These 2 numbers aren't equal because the first instruction requires 4 clock cycles.
There are 2 ST instructions every jump and there are 4 jumps.

ii) Clock cycles with Branch Interlock = 53

Instructions executed: 39
ticks: 53

Instruction Cache

00	XOR	R1	R1	R1
04	BEQZ	-	R2	24
08	ST	R2	R0	00
0C	ANDI	R2	R2	01
10	BEQZ	-	R2	08
14	ADD	R1	R1	R3
18	LD	R2	R0	00
1C	SRLI	R2	R2	01
20	SLLI	R3	R3	01
24	J	-	-	E0
28	ST	R1	R0	00
2C	HALT	-	-	-
30	NOP	-	-	-
34	NOP	-	-	-
38	NOP	-	-	-
3C	NOP	-	-	-
40	NOP	-	-	-

This number differs from part (i) as with branch interlock, there is a lack of Branch target buffer and a 1 tick delay is added instead, 2 clock cycles are needed because of this.

iii) With Branch Prediction with 2 shift instructions swapped.

Instructions executed: 30
ticks: 38

Instruction Cache

00	XOR	R1	R1	R1
04	BEQZ	-	R2	24
08	ST	R2	R0	00
0C	ANDI	R2	R2	01
10	BEQZ	-	R2	08
14	ADD	R1	R1	R3
18	LD	R2	R0	00
1C	SLLI	R3	R3	01
20	SRLI	R2	R2	01
24	J	-	-	E0
28	ST	R1	R0	00
2C	HALT	-	-	-
30	NOP	-	-	-
34	NOP	-	-	-
38	NOP	-	-	-
3C	NOP	-	-	-
40	NOP	-	-	-

This time, there is 9 less instructions executed and 2 less jumps as there is a difference of 8 between instructions executed and clock cycles. Execution time is quicker as less instructions.