CS1026

Lab #7

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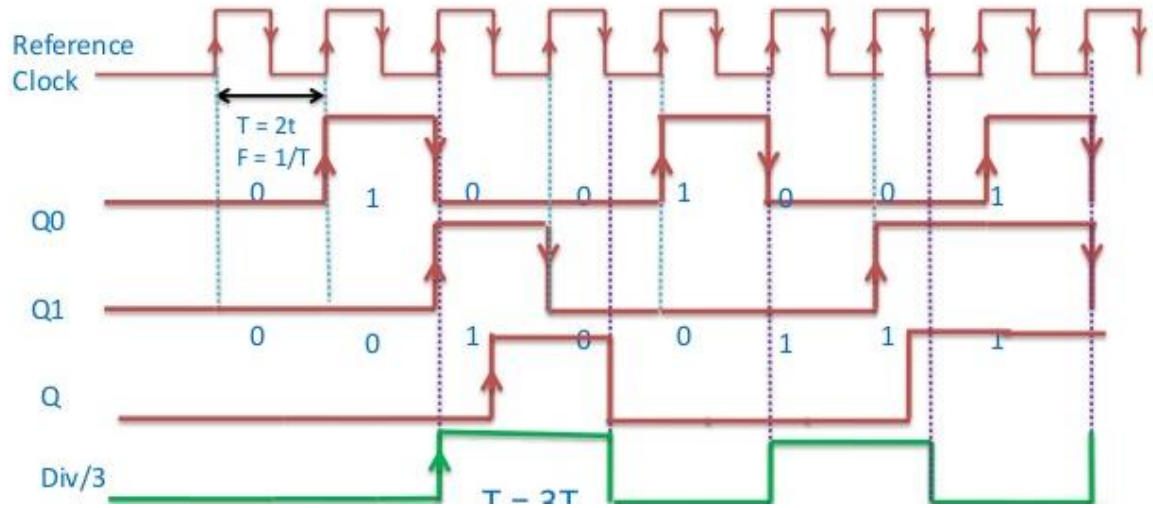
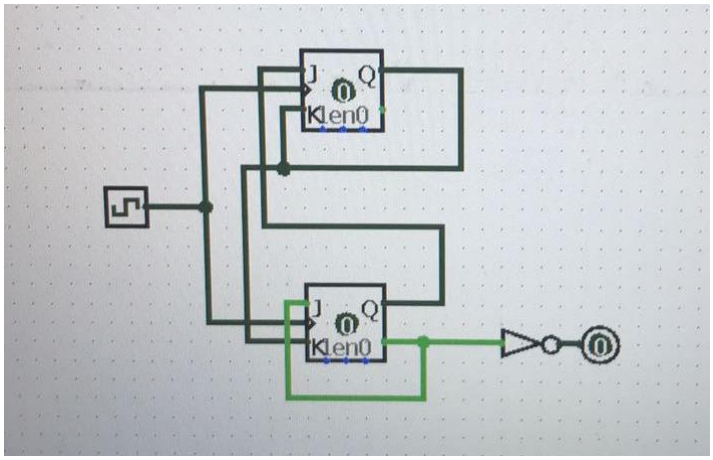
Design a synchronous sequential circuit called “Div-by-3”

JK flip-flop truth table:

| J | K | clock | Q |
|---|---|---|---|
| 0 | 0 | 1 | Q0(no change) |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | Q’0(toggles) |




This divides a system clock frequency by3.