CS2022 Computer Architecture

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Project 1 -Datapath Design -Part B

19 February 2018

Description:

Expand the *register·file* from PROJECT lA by adding a *B-Data Bus* and a *Functional Unit* to the *eight registers* in order to obtain 16-bit version of the *Datapath* shown in Figure 1 on page 3. Figure 1 is taken from Figure 7-19 in Mano and Kime.

You should write a *gate-level VHDL models* for the *Functional Unit.* The architecture should use a *16-bit ripple adder.* The *Functional Unit* should have the functionality defined on the Table 1 on page 2. Set all gate propagation delays to 1 ns and simulate arithmetic operations.

Discuss your simulation results. The CS2022 lecture notes provide the necessary information to complete the project.

DUE: Friday, 9th March 2016

Please submit a copy of your VHDL-code and test-benches including all simulation results (screenshots) for every "Entity" to Blackboard.

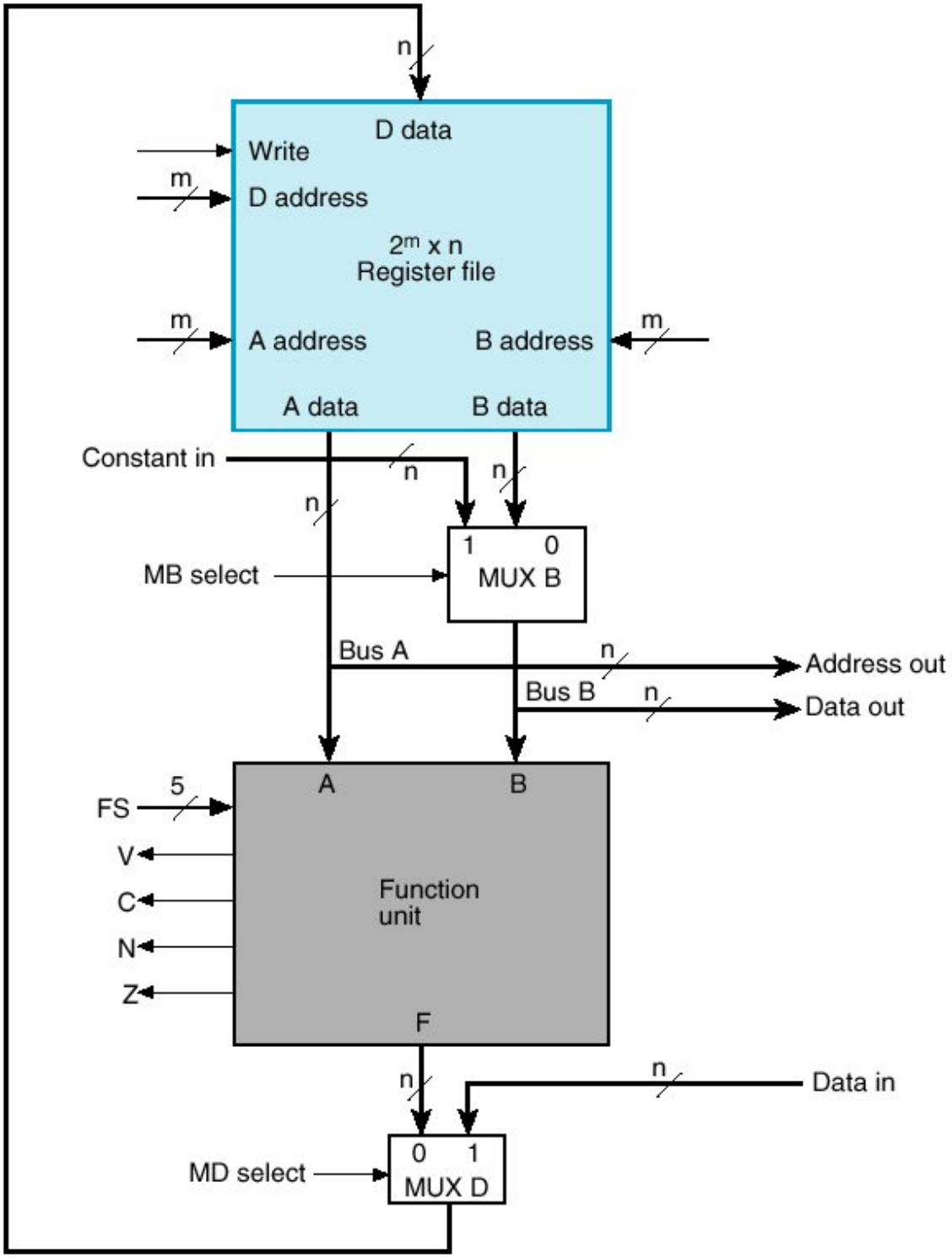

Figure 1: Register File and Functional Unit

Table 1: FS code definition

FS	MF Select	G Select	H Select	Micro-operation
00000	0	0000	00	$F = A$
00001	0	0001	00	$F = A + 1$
00010	0	0010	00	$F = A + B$
00011	0	0011	00	$F = A + B + 1$
00100	0	0100	01	$F = A + \bar{B}$
00101	0	0101	01	$F = A + \bar{B} + 1$
00110	0	0110	01	$F = A - 1$
00111	0	0111	01	$F = A$
01000	0	1000	00	$F = A \wedge B$
01010	0	1010	10	$F = A \vee B$
01100	0	1100	10	$F = A \oplus B$
01110	0	1110	10	$F = \bar{A}$
10000	1	0000	00	$F = B$
10100	1	0100	01	$F = srB$
11000	1	1000	10	$F = slB$