SPLL LIB Release Notes

<table>
<tr><td>V1_03_00_00</td><td>Add support for 3-phase modules
- Decoupled double synchronous reference frame (DDRF)
- Synchronous reference frame (SRF)</td></tr>
<tr><td>V1_02_00_00</td><td>Updates to support EABI output format based CCS projects</td></tr>
<tr><td>V1_01_00_00</td><td>Major update to library interface to comply with coding standard for C2000 SW. Following are the changes required in a typical application for SPLL Lib usage when migrating from an older version to this new library at init time as we now have reset and config function that will do all the settings.

SPLL_1PH_SOGI
Previous:
<pre>SPLL_1PH_SOGI_init(AC_FREQ,
                  ((float)(1.0/CONTROL_ISR_FREQUENCY)),
                   &spll1);
SPLL_1PH_SOGI_coeff_calc(((float)(1.0/CONTROL_ISR_FREQUENCY)),
                         (float)(2*PI_VALUE*AC_FREQ),
                          &spll1);

spll1.lpf_coeff.b0=(float)(222.2862);
spll1.lpf_coeff.b1=(float)(-222.034);</pre>New:
<pre>SPLL_1PH_SOGI_reset(&spll1);
SPLL_1PH_SOGI_config(&spll1,
                     AC_FREQ,
                     CONTROL_ISR_FREQUENCY,
                    (float32_t)(222.2862),
                    (float32_t)(-222.034));</pre>SPLL_1PH_SOGI_FLL
Previous:
<pre>SPLL_1PH_SOGI_FLL_init(AC_FREQ,
                       ((float)(1.0/CONTROL_ISR_FREQUENCY)),
                       &spll3);
spll3.k=0.5;
spll3.gamma=20000;</pre></td></tr>
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	SPLL_1PH_SOGI_FLL_coeff_calc(&spll3);
	spll3.lpf_coeff.b0=(float)(222.2862);
	spll3.lpf_coeff.b1=(float)(-222.034);
	
	New:
	
	SPLL_1PH_SOGI_FLL_reset(&spll3);
	
	SPLL_1PH_SOGI_FLL_config(&spll3,
	AC_FREQ,
	CONTROL_ISR_FREQUENCY,
	(float32_t)(222.2862),
	(float32_t)(-222.034),
	(float32_t) 0.5,
	(float32_t) 20000);
	
	SPLL_1PH_NOTCH
	
	Previous
	SPLL_1PH_NOTCH_init(AC_FREQ,
	((float)(1.0/CONTROL_ISR_FREQUENCY)),
	&spll2);
	SPLL_1PH_NOTCH_coeff_calc((float)(CONTROL_ISR_FREQUENCY),
	(float)(AC_FREQ*2.0),
	0.25,
	0.00001,
	&spll2);
	spll2.lpf_coeff.b0=(float)(222.2862);
	spll2.lpf_coeff.b1=(float)(-222.034);
	
	New:
	SPLL_1PH_NOTCH_reset(&spll2);
	SPLL_1PH_NOTCH_config(&spll2,
	AC_FREQ,
	CONTROL_ISR_FREQUENCY,
	(float32_t)(222.2862),
	(float32_t)(-222.034),
	(float32_t) 0.25,
	(float32_t) 0.00001);

V1_00_00_00 or previous releases	• First release in Digital Power SDK.