# CMPE 140 – Laboratory Assignment 6

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(This lab is created by Prof. Donald Hung)

## Processor Design (2) – Processor Hardware Validation

**Purposes:**

1) Learn the basic technique for processor validation using FPGA devices
2) Practice processor hardware validation using the ten-instruction 32-bit single-cycle MIPS processor functionally verified in Assignment 5

**Preparation:**

1) Download the archive "*basys3_single_cycle_mips_validation*" from the class Canvas site and retrieve all the archived files, including:
   - File "*mips_fpga.v*" containing Verilog source code for FPGA validation of the single-cycle MIPS processor, which has been functionally verified in Assignment 5.
   - Verilog source code of all utility modules you will need to setup the validation environment.
   - A Xilinx design constraint file "*mips_fpga.xdc*" specifying signal-pin constraints
2) Carefully study the source code you obtained from the archive and based on which, set up the validation environment on the Basys3 board, for the 10-instruction single-cycle MIPS processor. The program shown below will be executed by the MIPS processor during the validation (Note: the same program has been tested using MIPS debugger in Assignment 2, and then used for processor functional verification in Assignment 5). To do so a copy of the memory file containing machine code of this test program should be placed in the project directory for this assignment, so that the program will be loaded into the processor's instruction memory.

| Label | Assembly | Address (hex) | Machine Code (hex) |
|---|---|---|---|
| main: | addi $2, $0, 5 | 0 | 20020005 |
| | addi $3, $0, 12 | 4 | 2003000c |
| | addi $7, $3, -9 | 8 | 2067fff7 |
| | or $4, $7, $2 | c | 00e22025 |
| | and $5, $3, $4 | 10 | 00642824 |
| | add $5, $5, $4 | 14 | 00a42820 |
| | beq $5, $7, end | 18 | 10a7000a |
| | slt $4, $3, $4 | 1c | 0064202a |
| | beq $4, $0, around | 20 | 10800001 |
| | addi $5, $0, 0 | 24 | 20050000 |
| around: | slt $4, $7, $2 | 28 | 00e2202a |
| | add $7, $4, $5 | 2c | 00853820 |
| | sub $7, $7, $2 | 30 | 00e23822 |
| | sw $7, 68($3) | 34 | ac670044 |
| | lw $2, 80($0) | 38 | 8c020050 |
| | j end | 3c | 08000011 |
| | addi $2, $0, 1 | 40 | 20020001 |
| end: | sw $2, 84($0) | 44 | ac020054 |
| | j main | 48 | 08000000 |

**Task:**

Use a push button generated clock, let the MIPS processor under validation execute the test program one instruction at a time, and verify contents of the relevant registers as well as signals applied to the data memory displayed on the 7-segment LEDs. Compare these values with your test log obtained from Assignment 2.

**Report Contents:**

As the essential elements of your lab report, you should include

a) A diagram that illustrates your validation environment setup, and
b) A validation record table that lists your observations on each instruction execution, and comparison with the log file you have completed in Assignment 2.