CS 247 - Project 2

1) The following circuit contains two gates. Independent of time, it would functionally produce a constant output of C = 0. However, as this problem demonstrates, timing is a critical design parameter which must be factored into account by computer architects. The issue being examined in this problem is that of a Race or Glitch Condition. The tell-tale sign that a circuit may exhibit a timing glitch is a situation where one input path to a gate is longer that of the other. The existence of this condition is obvious and easy to spot in the circuit below; however, for complex circuits with multiple computation paths and large fan-in/fan-out between gates, the potential for hidden glitches can be quite high. It is in this area that computer-aided design tools, such as VHDL, can offer valuable assistance to the engineer in terms of predicting actual performance of the circuit as a function of time.

Simulate the circuit using a structural architecture to determine its output response for various combinations of delay values for each gate. For example, try all four combinations of NOT delay = (2ns or 4ns) and AND delay = (1ns or 3ns). Run a sufficient number of simulations while permuting the delay values on each of the gates so that you can answer (and provide documentation) for the questions below.

In particular, assume the actual purpose of the circuit is to deliberately produce a pulse (glitch) at output C whenever input A has a positive (0 to 1) transition. [40 pts]

a) If both gates have non-zero inertial delay values, what relationship must exist between the delay time of the INVERTER and the delay time of the AND gate in order for the circuit to produce a pulse ?

b) Assuming the constraint in (a) above is satisfied and that a positive transition of A occurs at time T, at what time will the beginning of the pulse occur at output C ?

c) Assuming the constraint in (a) above is satisfied, determine an equation which will predict the width of the pulse at output C.

2) Because of space and power constraints, satellites often only use dual processors instead of triple processors for increased reliability. Describe various ways in which detection and/or correction can be accomplished under this architecture. Under these situations, is real-time correction of faults possible ? Specify how you define “real-time” in your answer. [15 pts]

3) Explain the flaw in this statement: "A system with built-in TMR redundancy is always more reliable than a simplex system with no redundancy". Sketch any graphs that may be appropriate. Provide an intuitive explanation for why the graph is shaped the way it is. [15 pts]

4) Newer generation cars often have adaptive cruise control (ACC). Like ordinary cruise control, it allows the driver to set a constant speed for the car without having to continually press on the gas pedal; however, it is more intelligent. A radar/laser/camera unit located behind the grille determines the speed and distance of the vehicle in front. If necessary, ACC will automatically slow down the car to maintain a safe following distance should the car in front slow. When the distance to the vehicle in front is computed to be safe again, ACC accelerates the car to resume its last speed setting. Pretend you are a designer of ACC. Identify potential failure modes that your ACC must be capable of dealing with. List as many as you can. For example, your car is running on ACC when a loose plastic grocery bag or newspaper page on the freeway is kicked up by the car in front of you and clings to your car’s grille. [15 pts]

5) Imagine in the future, two self-driving cars get into an accident. Who's at fault ? [15 pts]