# PDS 1: Registers and usage protocol

**32 registers (32 bits):**

| Register Number | Assembly Name | Description |
|---|---|---|
| r0 | $zero | ZERO register |
| r1 | $pc | Program Counter |
| r2 - r4 | $v0 - $v2 | Used for Values returned |
| r5 - r8 | $a0 - $a3 | Function Arguments |
| r9 - r18 | $t0 - $t9 | Temporary registers |
| r19 - r26 | $s0 - $s7 | Saved registers |
| r27 | $hi | High register |
| r28 | $lo | Low register |
| r29 | $sp | Stack Pointer |
| r30 | $ir | Instruction register |
| r31 | $ra | Return Address register |

# PDS 2: Instruction and Data Memory Size in VEDA

- Instruction Memory - $2^{20}$ words
- Data Memory - $2^{20}$ words

# PDS 3: Instruction layout and Encoding

**R - Format:** op(6), rs(5), rt(5), rd(5), shamt(5), funct(6)

| Mnemonic | Op | Funct |
|---|---|---|
| add | 0 | 0 |
| sub | 0 | 1 |
| addu | 0 | 2 |
| subu | 0 | 3 |
| and | 0 | 4 |
| or | 0 | 5 |
| sll | 0 | 6 |
| srl | 0 | 7 |
| slt | 0 | 8 |
| jr | 0 | 9 |

**I - Format:** op(6), rs(5), rt(5), imm(16)

| Mnemonic | Op | Imm Field Extension (to 32 bits) |
|---|---|---|
| addi | 3 | Sign extension |
| addiu | 4 | Sign extension |
| andi | 5 | Zero extension |
| ori | 6 | Zero extension |
| lw | 8 | Sign extension |
| sw | 9 | Sign extension |
| beq | 10 | Sign extension |
| bne | 11 | Sign extension |
| bgt | 12 | Sign extension |
| bgte | 13 | Sign extension |
| ble | 14 | Sign extension |
| bleq | 15 | Sign extension |
| slti | 7 | Sign extension |

**J - Format:** op(6), tar_add(26)

| Mnemonic | Op | tar_add field extension (to 32 bits) |
|---|---|---|
| j | 1 | Zero extension |
| jal | 2 | Zero extension |