Analog VLSI Circuits

Lab 4

September 2024

PART1: SIMPLE CURRENT MIRROR DESIGN

Explore current mirror using `nmos` transistor cells from the `gpdk180` library.

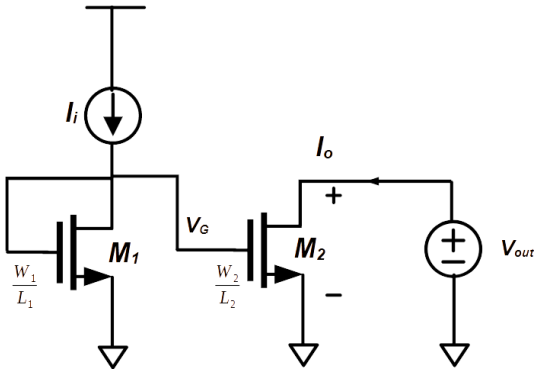

Figure 1: Simple NMOS current mirror

a) Design a current mirror for input reference current of I_i = 10 µA and output current of I_o = 30 µA (initial design 1) Sweep V_{out} and plot % error ($(I_{o,sim} - I_o) \times 100/I_o$ as a function of V_{out}.

b) How can you reduce error in a)? (Hint: increase L, why?). Sweep L and plot change in error with increasing L for a fixed V_{out} (for example V_{out} = VDD).

c) Use initial design, sweep temperature from -40 to 150 C and plot the effect on % error. Can you reduce error by increasing V_{od} (Hint: decrease W/L)? For this question, plot a family of curve with % error vs. temperature for different V_{od}.

d) Based on the results of a), b) and c) finalize a design (final design 1) of the current mirror i.e., W/L values for M1 and M2 and provide your justification.

e) Repeat the exercise for smaller current I_i = 100 nA, and I_o = 3µA, i.e., start with initial design 2 and follow the procedure above to obtain final design 2. Note that you would require large L to satisfy sufficient V_{od}. Compare the estimated area of final design 1 and final design 2.

f) Use the final designs 1 and 2 and provide a step in the respective input current I_i with rise time of 100 ps. Plot the transient settling of I_o with time. Calculate the 10% to 90% rise times. Comment on the results.

g) Draw the layout of the final design 1. Write and justify the layout considerations you made.

PART2: SELF-BIASED HIGH SWING CURRENT MIRROR DESIGN

Design a high-swing current mirror using `pmos` transistor cells from the `gpdk180` library with $I_{ref} = 10\mu A$ and $I_{out} = 50\mu A$. Use V_{od}= 200mV for the mirror device M_1 and M_2. Use V_{od}= 50mV for the cascode devices M_3 and M_4.

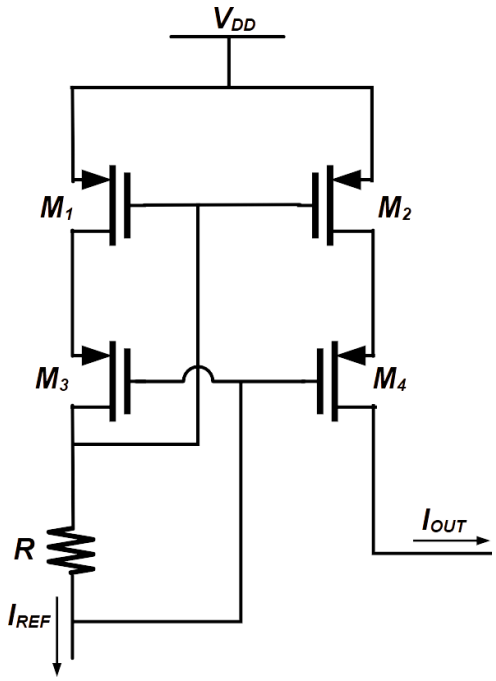

Figure 2: High swing PMOS current mirror

Characterize the following:

a. Perform a DC operating point simulation with $V_{out} = VDD/2$ at room temperature. Annotate the DC operating voltages. Calculate output impedance R_{out} from the DC operating point of the devices. Calculate the minimum required output voltage ($V_{out,min}$).
b. Output current vs. output voltage using a DC sweep of V_{out}. Plot I_{out} vs V_{out}. Calculate R_{out} from the I_{out} vs. V_{out} curve. Plot % error with respect to the ideal output vs. V_{out}. From the error plot estimate the operating output voltage range. Compare the result with a).
c. Characterize output impedance R_{out} for $V_{out} = VDD/2$ using AC simulation. Compare with a) and b).
d. Perform a temperature sweep from -50C to 150C for $V_{out} = VDD/2$ and plot % error vs. temperatur