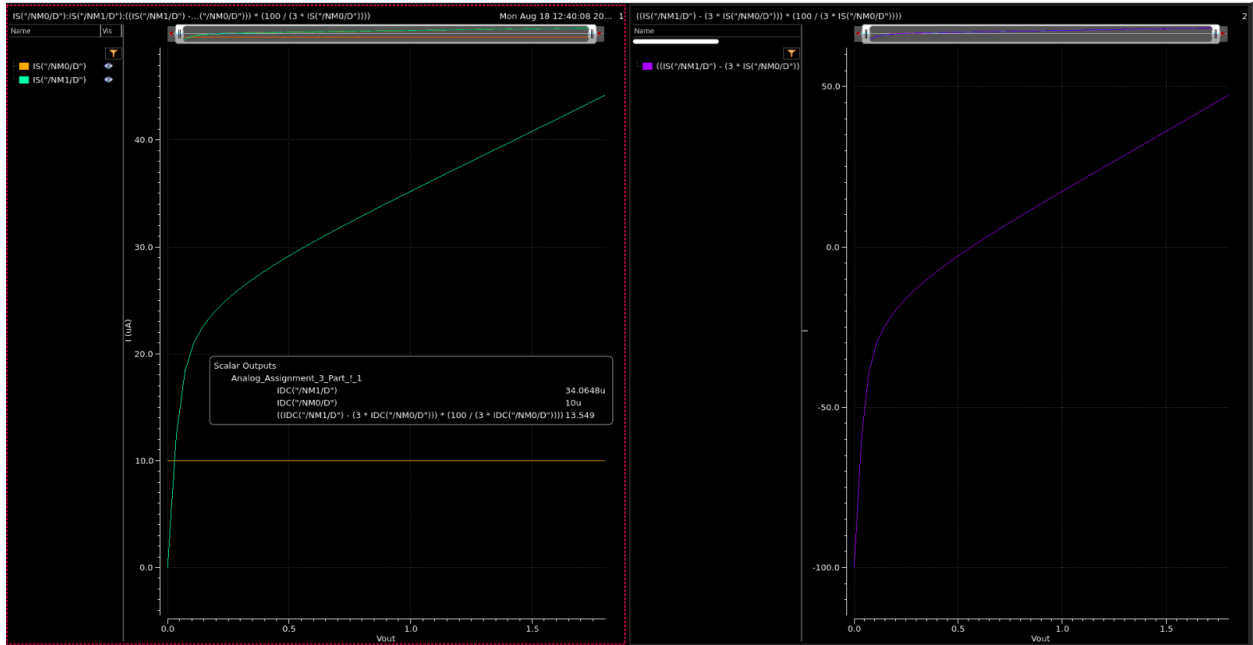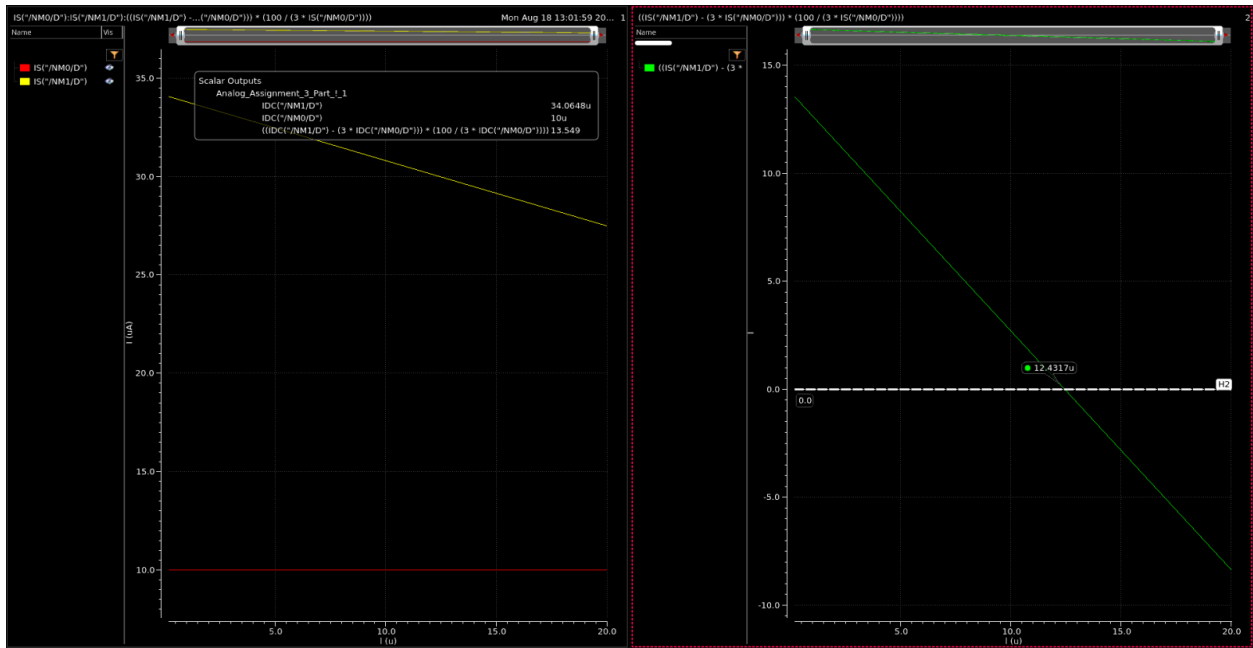# Analog Assignment-4

Part-1
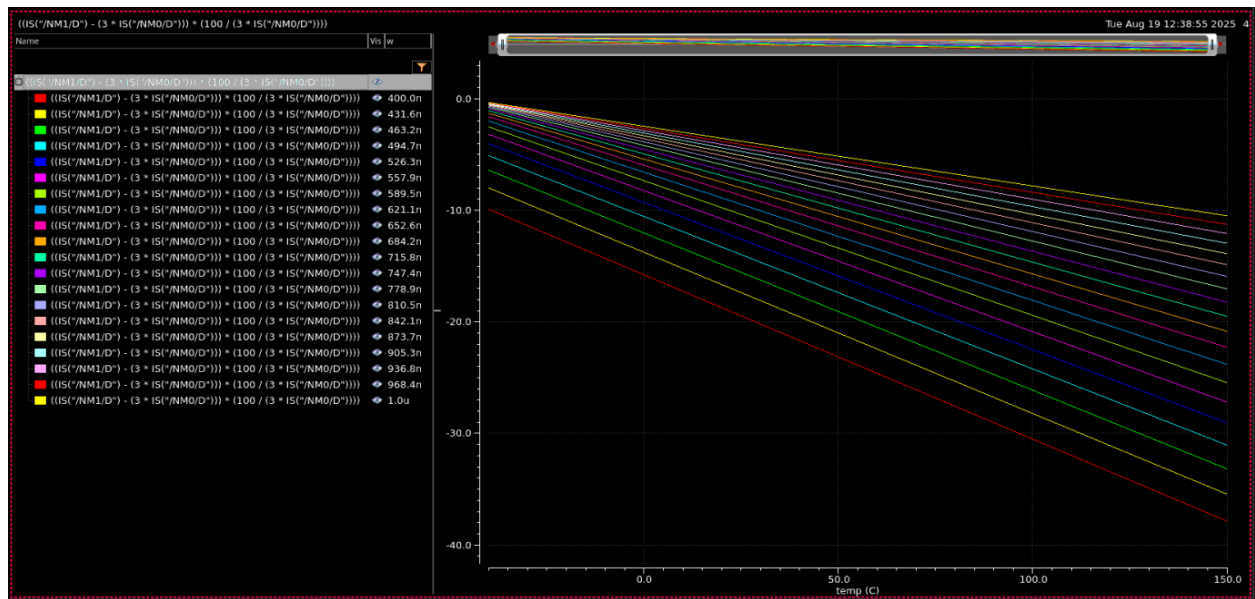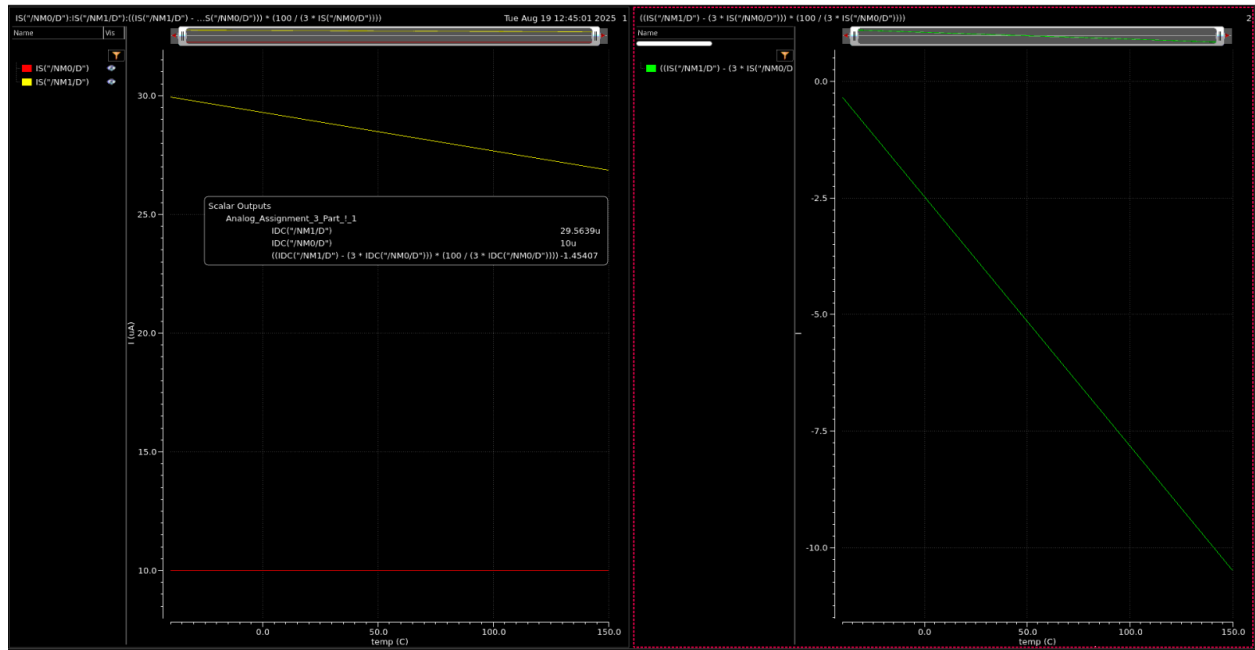a)

b) By increasing 'I', 'r_0' channel resistance increases hence large r_0 makes current less sensitive to V_DS, which can lead to reduced error.
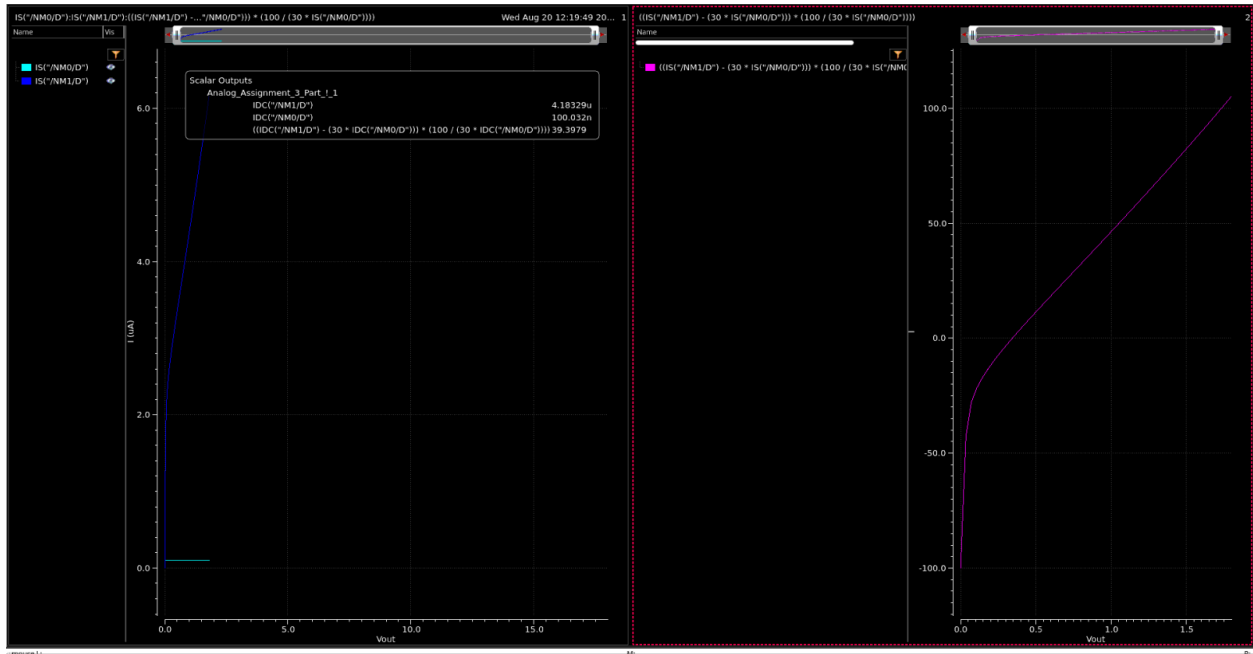
c)
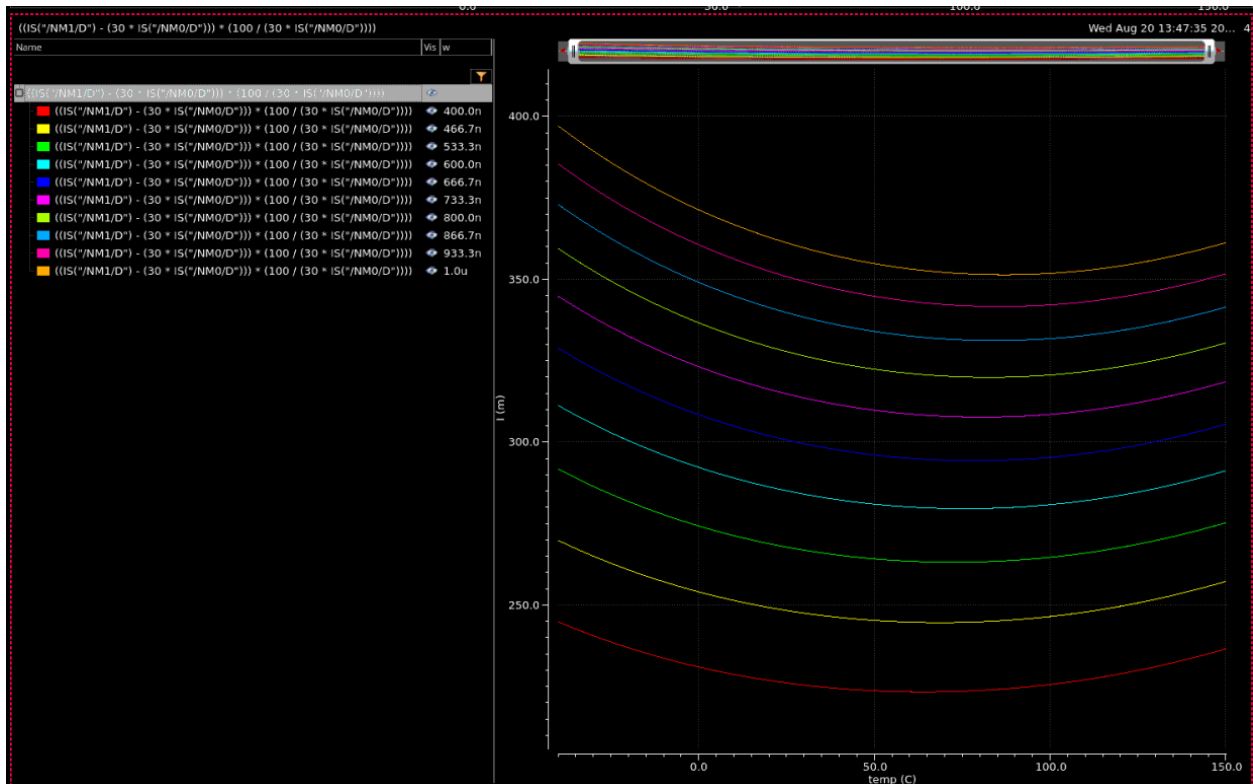

d) The final values of the w/l for M1: width=968.4 nm, length= 12.431 um and for M2: width=2905.2 nm, length=12.431 um (If the device multiplier is **n** (often m = n), then **W_eff = n × W**, while **L stays the same**). Either way, the transconductance and drain current scale roughly with **W_eff**, and the W/L ratio scales by **n** when you set the multiplier to **n**.

e)

IS("/NM0/D"):IS("/NM1/D"):((IS("/NM1/D") - ...*/NM0/D"))) * (100 / (30 * IS("/NM0/D"))))   Wed Aug 20 12:19:49 20...   1

Name   Vis

■ IS("/NM0/D")
■ IS("/NM1/D")

Scalar Outputs
    Analog_Assignment_3_Part_!_1
        IDC("/NM1/D")   4.18329u
        IDC("/NM0/D")   100.032n
        ((IDC("/NM1/D") - (30 * IDC("/NM0/D"))) * (100 / (30 * IDC("/NM0/D")))) 39.3979

((IS("/NM1/D") - (30 * IS("/NM0/D"))) * (100 / (30 * IS("/NM0/D"))))   2

Name

■ ((IS("/NM1/D") - (30 * IS("/NM0/D"))) * (100 / (30 * IS("/NM0

The gpdk180 nmos models, not characterized for such long channels. So max simulating length for proper accuracy is considered to be 20 um. So the minimum error by increasing 'l' is found to be 0.36%.
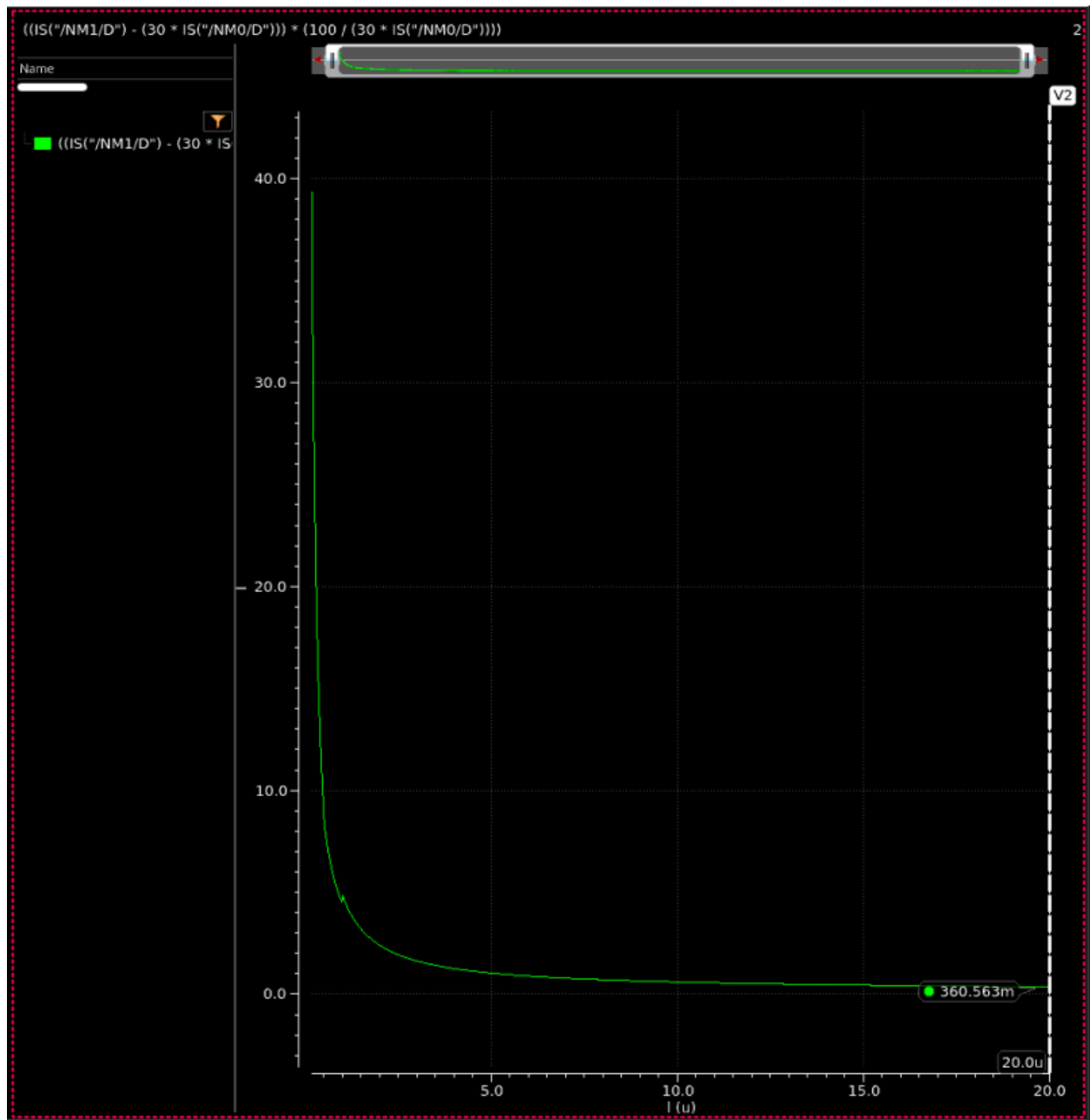
So the final values of the w/l for M1: width=400nm, length= 20 um.(**Design:2**) and for **Design:1**
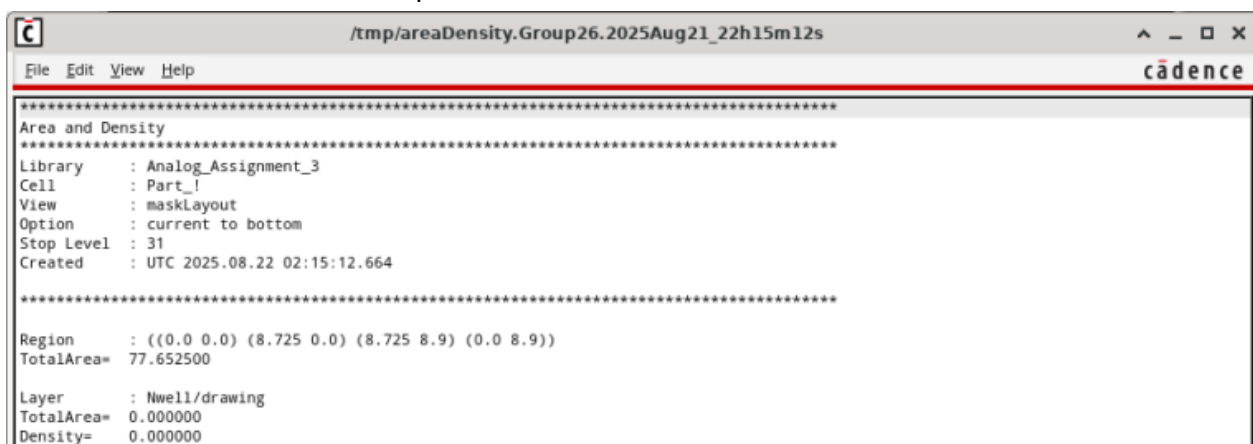the final values of the w/l for M1: width=968.4 nm, length= 12.431 um.

Area Comparison
Design:1
w=968.4 nm and l=12.431 um (computed value).
Area of each nmos = w*l=12.038 p m^2
Area of 4 nmos = 4*w*l=48.152 p m^2

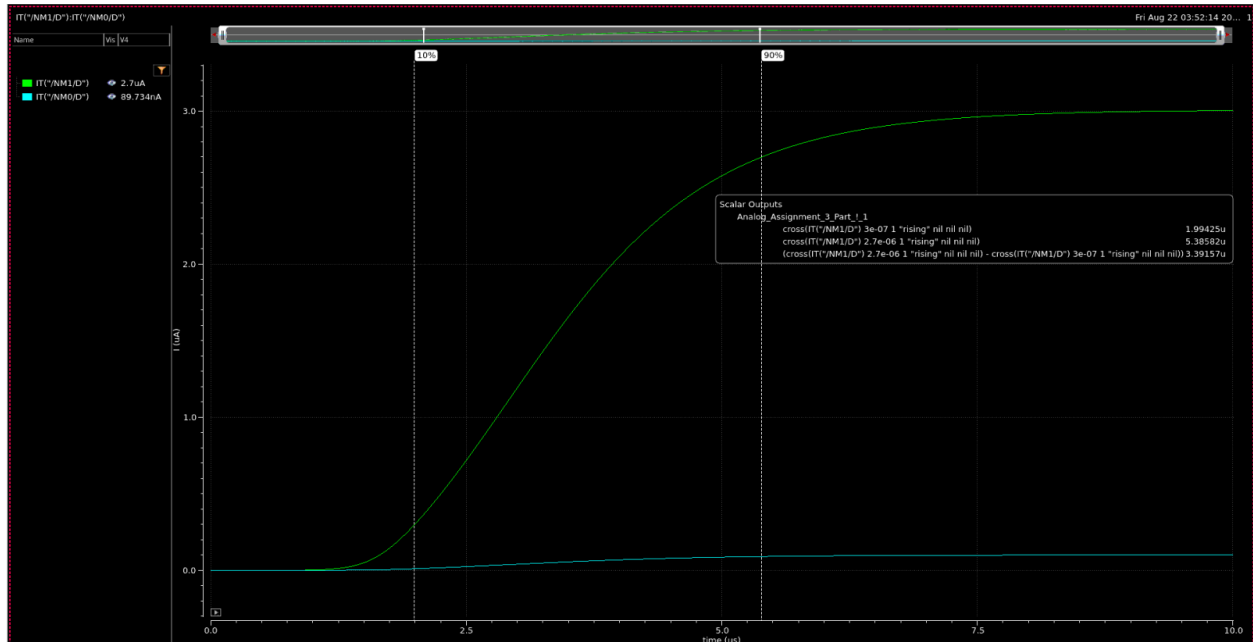Design:2
w=400 nm and l= 20 um (computed value).
Area of each nmos = w*l=8 p m^2
Area of 31 nmos = 31*w*l=248 p m^2
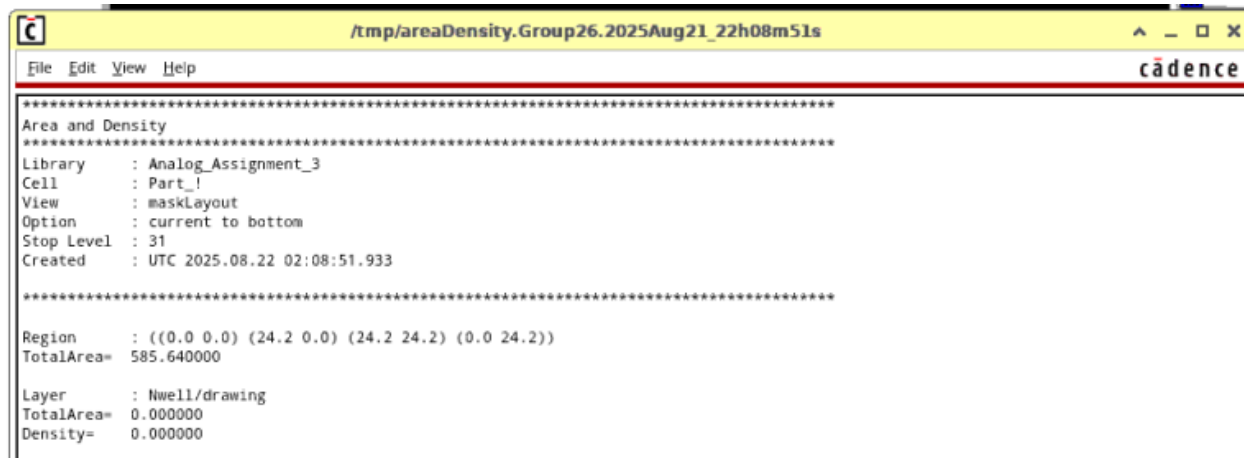
Hence with 30 multipliers the total area is almost similar to that with 3 multipliers, with computation the total area coming out to be almost 601.8 pm^2(As per the simulated value).
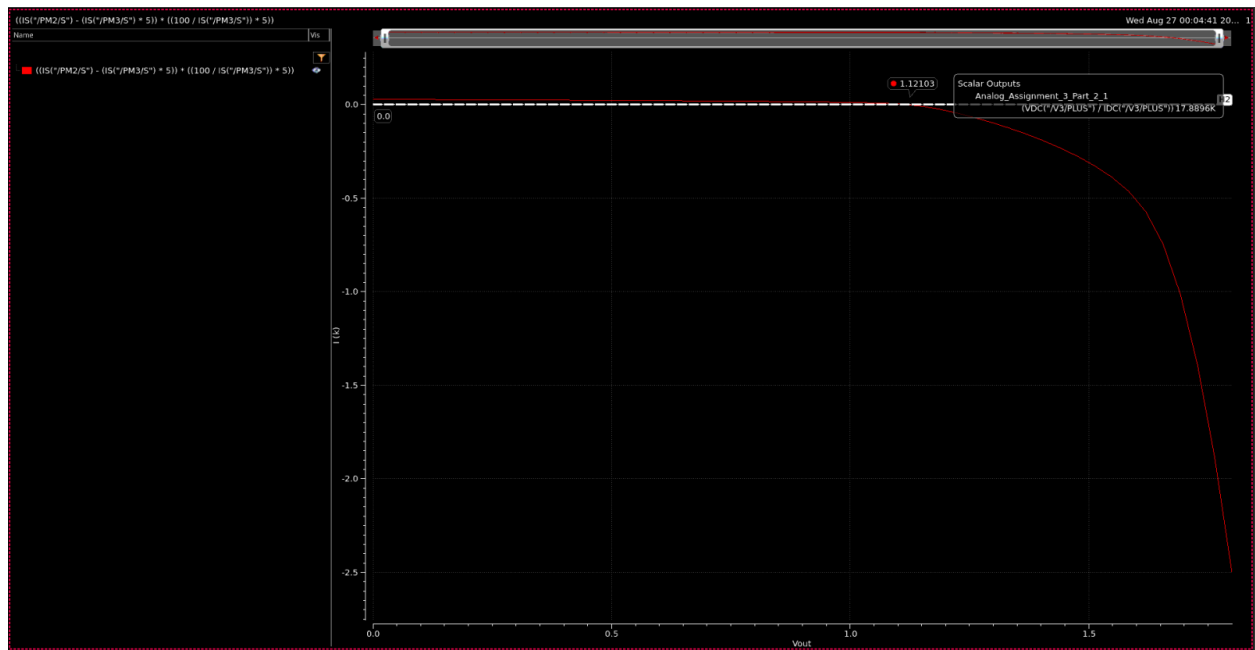
f)
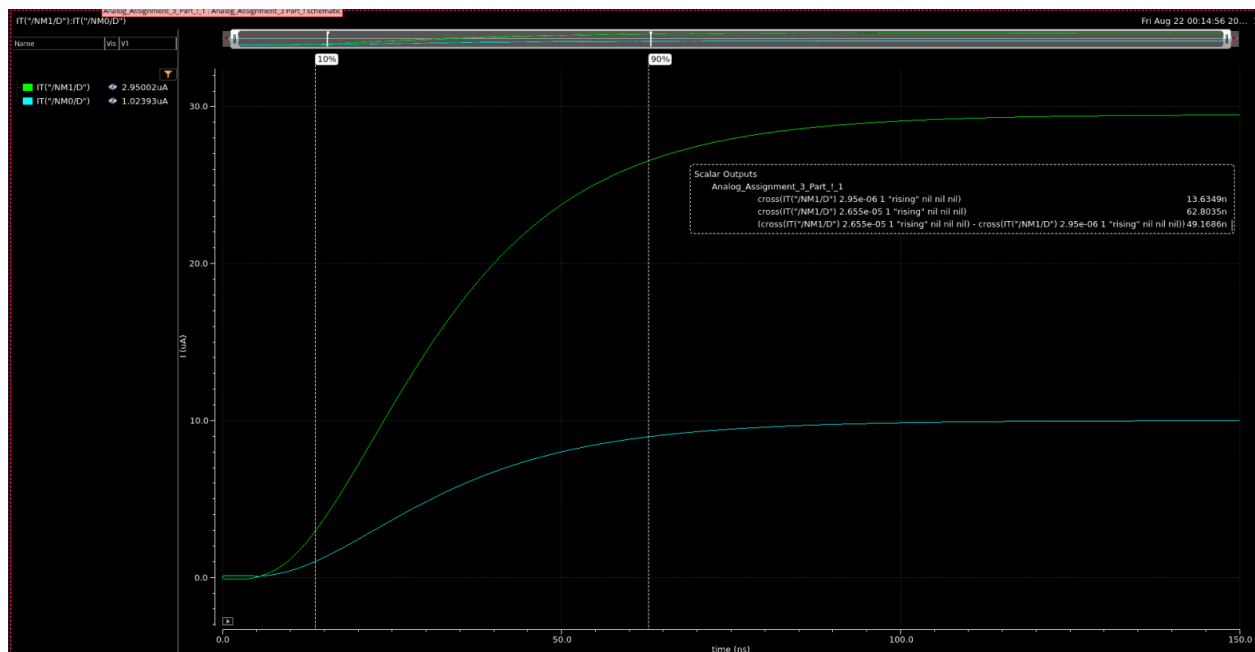
g) While designing a current mirror, the main considerations are **matching, output resistance, compliance voltage, accuracy (mismatch, λ, body effect), frequency response, power trade-offs, and layout techniques**.
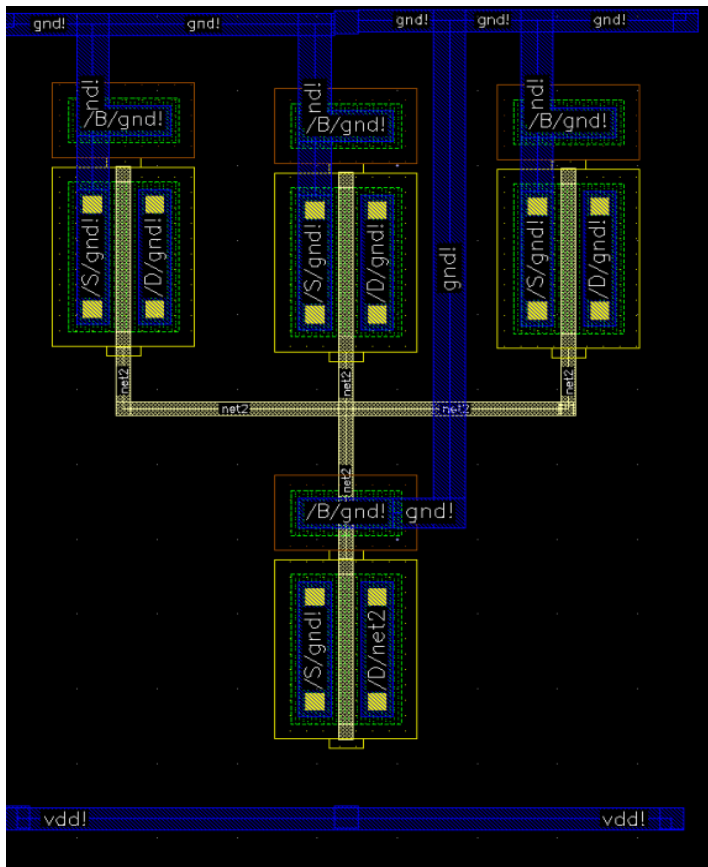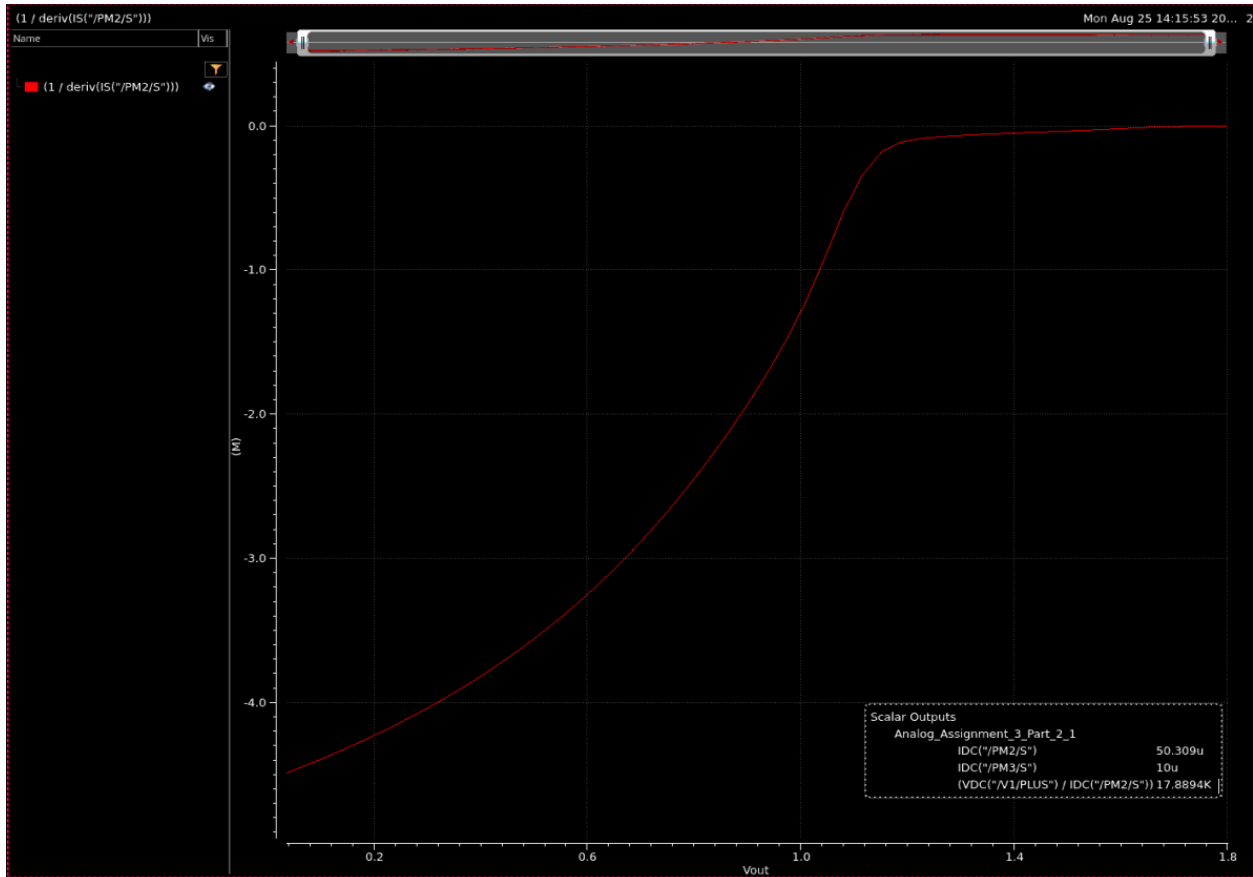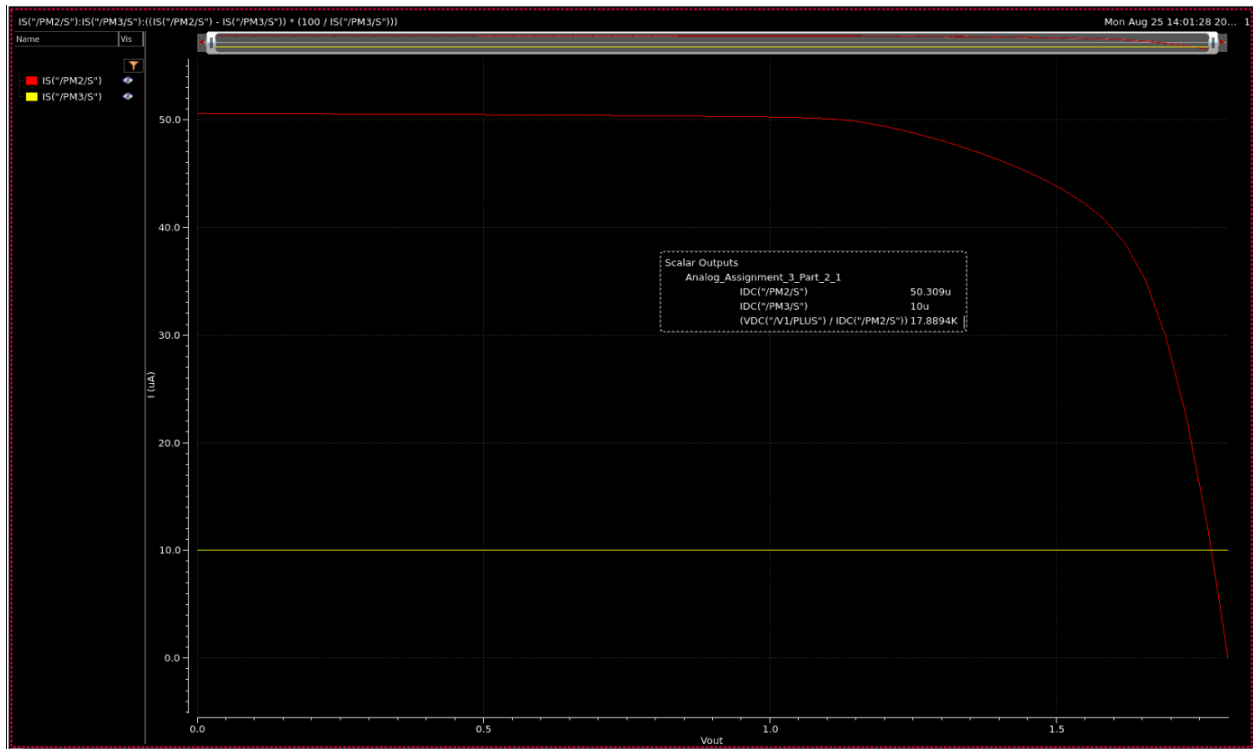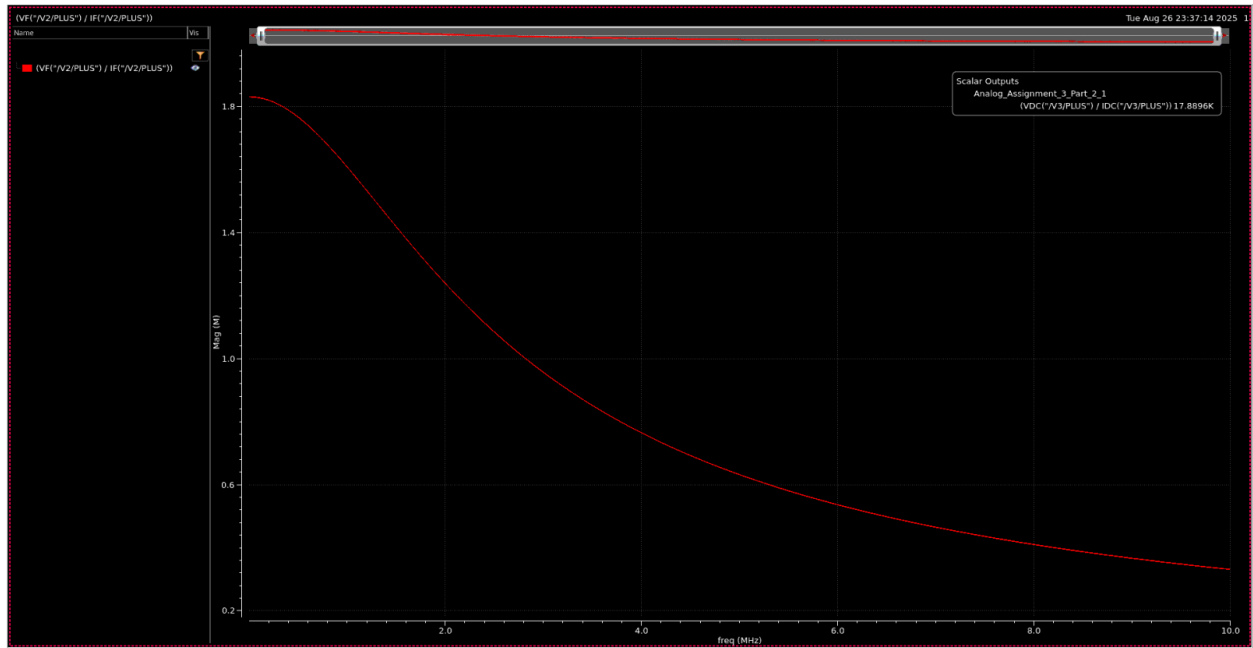
Part_2:

a) The output impedance calculated from the design is 17.889 kohm. The minimum required output voltage for error to be zero is 1.12103 V.

b)

c)The DC output resistance from the circuit is calculated as 17.889 kohm, whereas from DC sweep the magnitude of resistance at Vdd/2 is -2db and for AC analysis it is 1.8 db.

d)