GPCDxT/xTP Series PCB Layout Guideline

1 Description

For PWM audio output mode, refer to the PCB layout suggestion in the following section for design guideline. In addition, reserve certain spaces for ferrite bead and filter capacitor in circuitry that will be used for EMI test and adjustment to finished-product. To determine whether or not the reserved components should exit depends on the EMI test result of PCB.

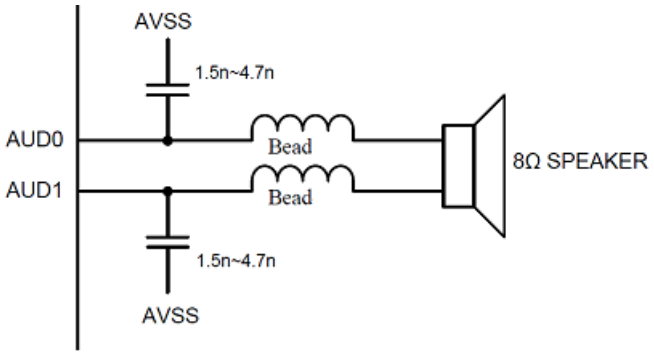
2 Solution

To elevate the EMI protection from layout measure, the placement of components should follow two main principles mentioned below:

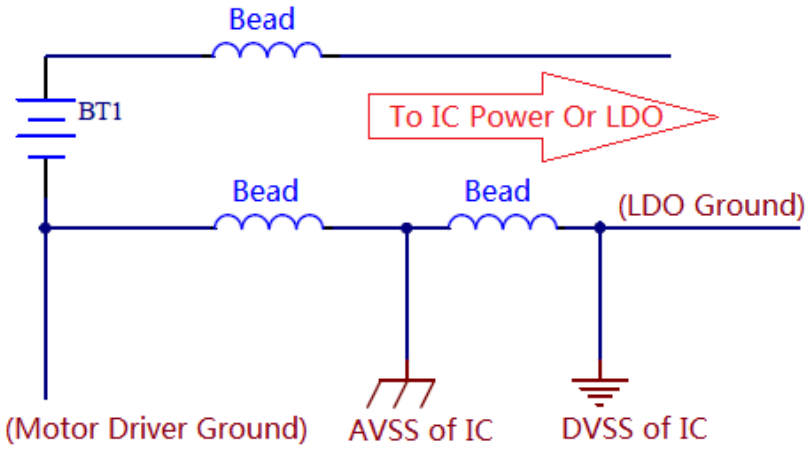
1. For those power-related pinouts should be located as close as possible to power end (battery or LDO).
2. Speaker's pinouts should be located as close as possible to IC's audio pinouts. After all major components are in position, follow the suggestions given below for layout guidance.

2.1 Reserve spaces for ferrite bead and filter capacitor in circuitry

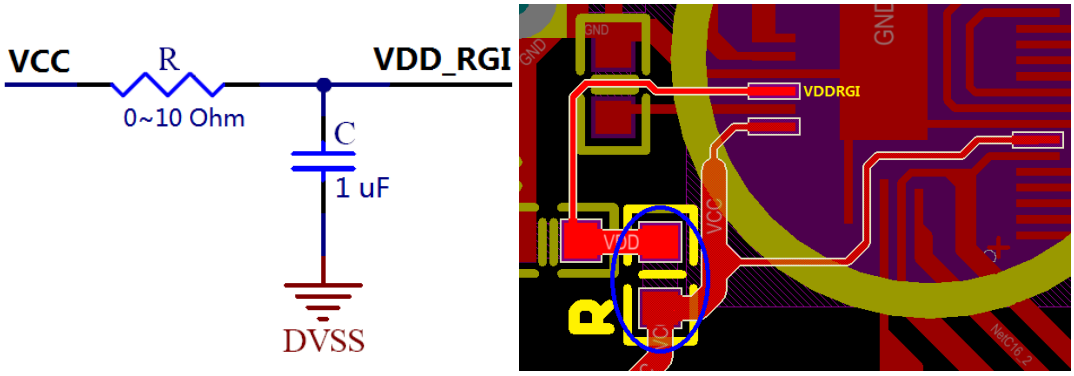
1) Reserve serial ferrite beads and grounding capacitor in AUD0 and AUD1. Furthermore, the path for ferrite bead, capacitor and speaker pinout should be as short as possible.



2) Reserve serial ferrite beads in power interface. While designing layout floor, make the following path as short as possible: Battery ➔ Bead ➔（LDO）➔ IC Power ➔ AVDD. The analog ground and digital ground routes must be separated. If digital ground connects to analog ground, reserve one more space for bead.

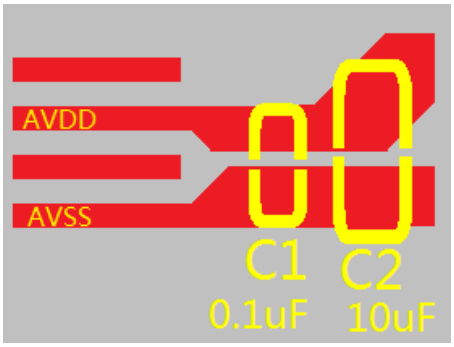


3) Reserve a RC circuit on the route of power entering core power (VDD_RGI) for core power stability when needed.

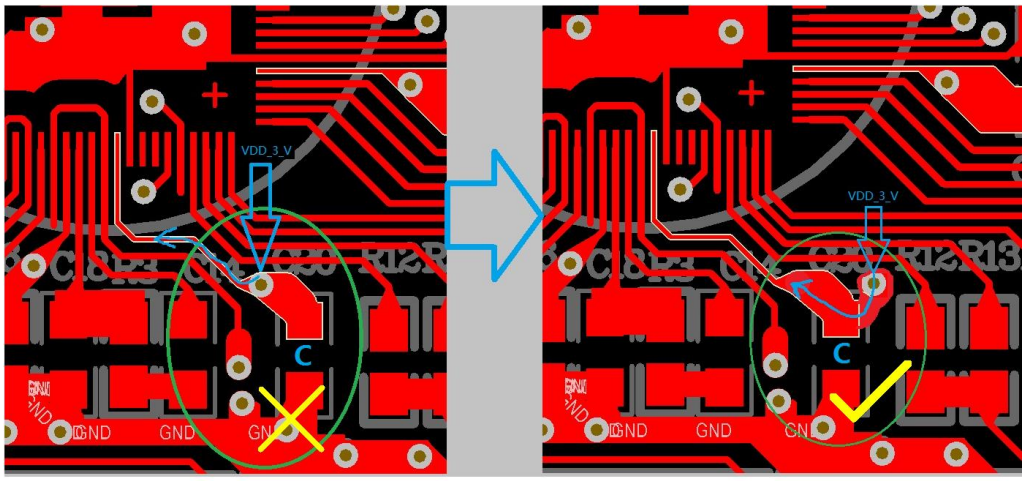


2.2 More Information about PCB Layout

1) The capacitor for audio power should be adjacent to IC's pinouts as close as possible and the width of route should be as wide as possible.



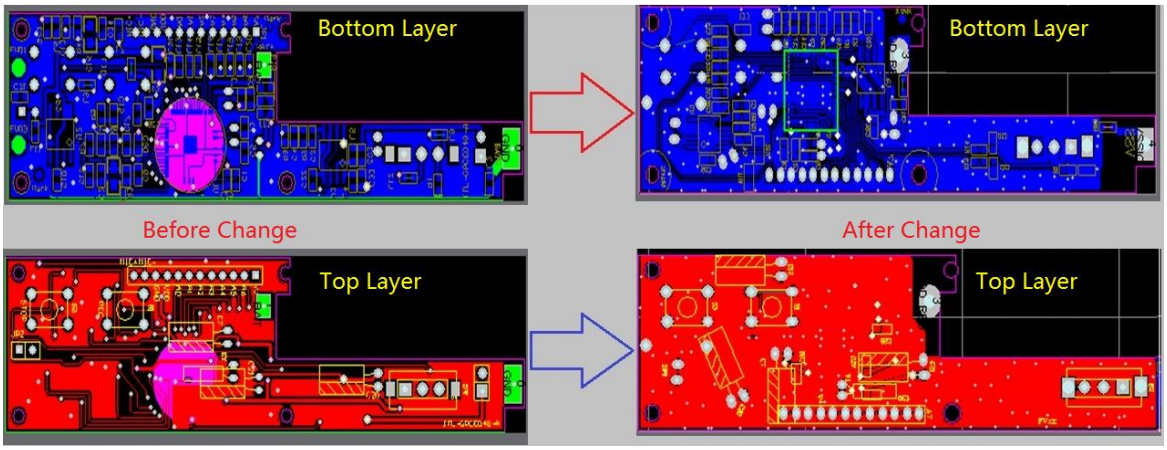
2) IC's power routing must via a filter capacitor before arriving IC's pinout, and the location of the capacitor must as close as possible to IC.



Before Change After Change

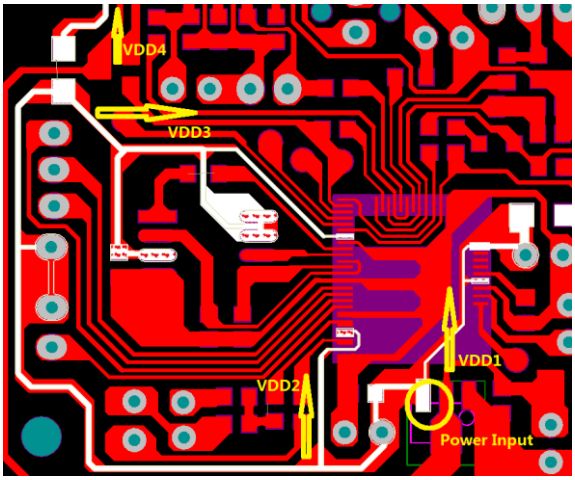
Note: For VDD_3_V routing, make sure it passes through a filter capacitor before reaching IC pinout.

3) For a double-side PCB, we recommend the PCB routing should be located on the component side and reserving a large area of ground on the non-component side with numerous via on blank spaces if possible.

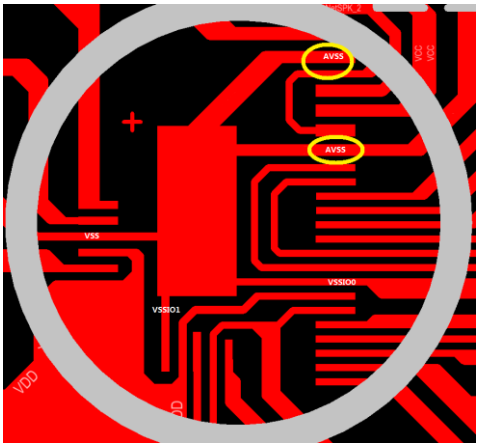


Note: 1. Enlarge IC's grounding area. 2. Properly allocate component 3. Reserve numerous via. 4. PCB routing on component-side if possible (see bottom Layer on the above diagram) 5.non-component side (See top layer on the above diagram) is mainly for grounding.

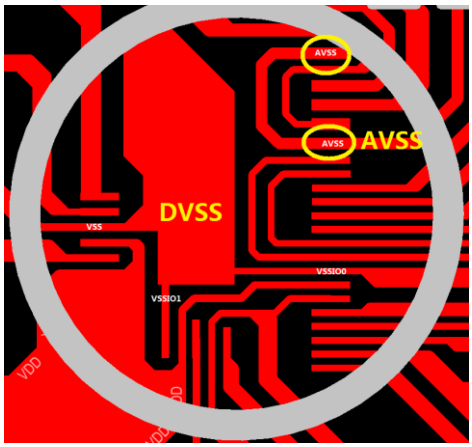
4) For a single side PCB, make the power routing as short as possible. Use a zero-ohm resistance jumper if necessary. To deliver power to each VDD pinout, branching route from a main route is recommended in order to prevent accumulated power noise effect while only using a main route to deliver power.



5) Separate the routes of analog ground (AVSS) and digital ground (VSS/VSSIO0/VSSIO1) as well as their groundings. (Area of substrate must be large enough to connect with digital ground)



Before Change



After Change

6) The AVSS/DVSS on IC's side must be separated from battery ground (refer to 2.1.2 for more details about the circuitry)