DATA SHEET

GPCD9TPXXXA

Multi-Channel Sound Controller

May 24, 2019

Version 1.5

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MULTI-CHANNEL SOUND CONTROLLER

1.GENERAL DESCRIPTION

GPCD9TPXXXA series features a maximum of 2M-byte internal OTP ROM, up to 1024-byte working SRAM, three 12-bit timers, 16~32 general I/Os, two 12-bit current DAC and one 14-bit audio PWM driver. The microprocessor can implement software based on audio processing, function control and others. For audio processing, melody and speech can be mixed into one output. GPCD9TPxxxA is implemented with a high performance SPU voice engine to generate 8-channel high-quality sound voice in ADPCM/PCM format. It operates in a wide voltage range, from 2.2V through 5.5V, along with low voltage reset function. In addition, a sleep mode is designed to save powers for those applications with limited power resources available. A Serial Peripheral Interface (SPI) controller is also included to facilitate communication with other devices and components.

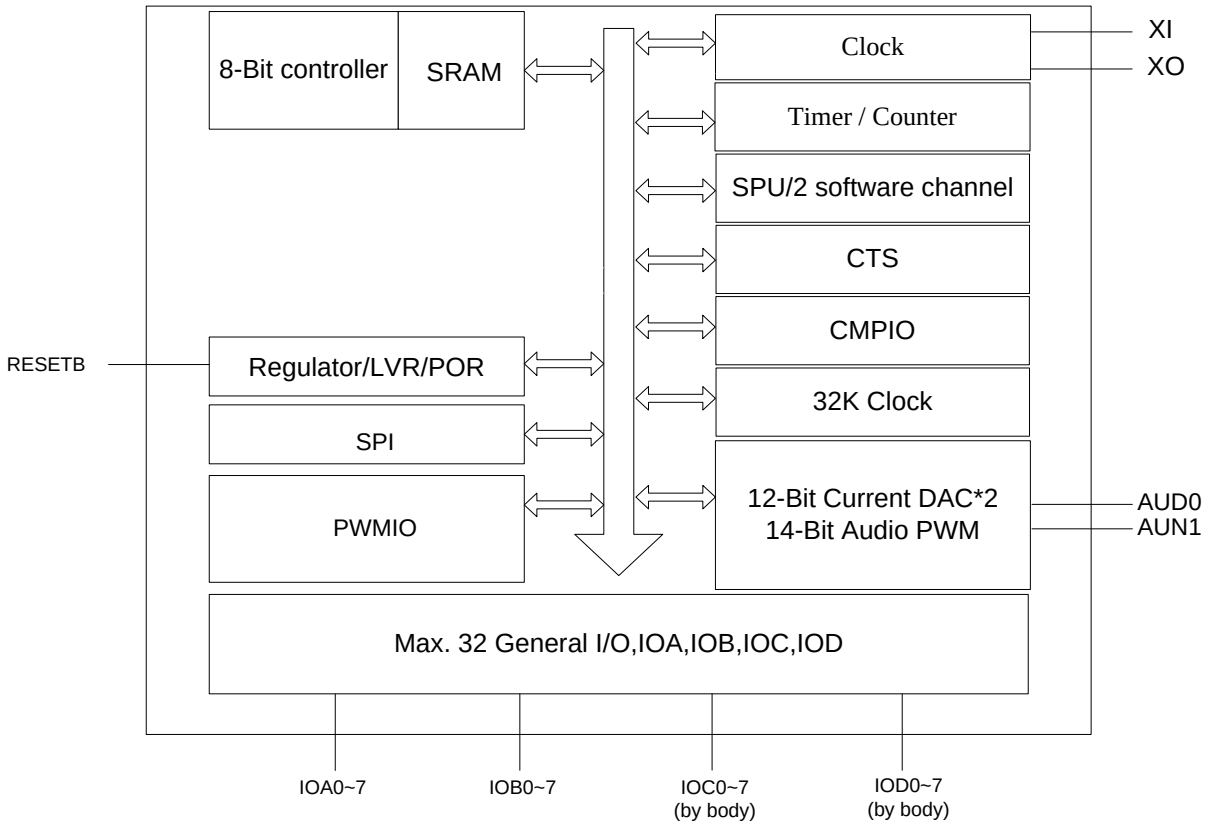
2.FEATURES

- 8-bit micro-processor
- Max. of 1024-byte SRAM
- Operating voltage: 2.2V – 5.5V
- Max. of CPU operating speed : 8.0MHz (Fosc=16MHz)
- Five wakeup sources
- 20 IRQs & 6 NMI Interrupts
- Internal built-in regulator to supply core power
- SPU(Sound Processing Unit) engine
  - Supports 4-bit ADPCM data format and TAG mode
  - Supports special tag, such as silence and event tags
  - 8-voice polyphony
- Two software channels with noise filter for high quality sound playback
- Low Voltage Detection
  8-level (2.2V/ 2.4V/ 2.6V/ 2.8V/ 3.0V/ 3.2V/ 3.4/ 3.6V) voltage detector
- Low Voltage Reset
- Peripherals
  - Max. of 32 I/O pins (IOA[7:0], IOB[7:0], IOC[7:0], IOD[7:0]) (varied by IC)
  - 8~12 I/Os with high sink current (varied by IC)
  - Key wakeup/interrupt function
  - Built-in 32.768KHz oscillator circuit for real time clock function (X'tal or R-osc)
  - Built-in R-oscillator (external resistor is needed), X'tal or internal R-oscillator (only 16MHz available for IOSC) for system operating clock
  - Internal time base generator
  - Three 12-bit timer/counter, TMA with capture and comparison function, TMB/TMC with comparison function (Programmable and auto reload)
  - Watchdog function
  - 14-bit PWM driver for driving speaker directly
  - Two 12-bit current DACs
  - IR output
  - Max. of 12 hardware PWMIOs
  - One SPI serial interface I/Os
  - Hardware Touch function
  - One set built-in comparator with PGA.
- 8-channel SPU engine with ADPCM/PCM wave table
- Sleep mode to reduce power

3.APPLICATION FIELD

- Talking instrument controller
- General music synthesizer
- General purpose controller
- High-end toy controller
- Intelligent education toy
- And more

4.BLOCK DIAGRAM



5. GPCD9TPXXXA FAMILY AND FEATURE LIST

Body	GPCD9TP680A	GPCD9TP340A	GPCD9TP170A	GPCD9TP080A
Voice Duration	680 seconds	340 seconds	170 seconds	80 Sec.
Working Voltage F_{osc} = Max. 16M	2.2~5.5V	2.2~5.5V	2.2~5.5V	2.2~5.5V
RAM Size	1KB	1KB	1KB	1KB
ROM Size	2MB	1MB	512KB	256KB
MAX. ROM address	0x1FFFFF	0x0FFFFF	0x07FFFF	0x03FFFF
IO Pin	32 (IOA/B/C/D)	32 (IOA/B/C/D)	24 (IOA/B/D)	24 (IOA/B/D)
SPU Channel	8	8	8	8
Software Channel	2	2	2	2
SPI	V	V	V	V

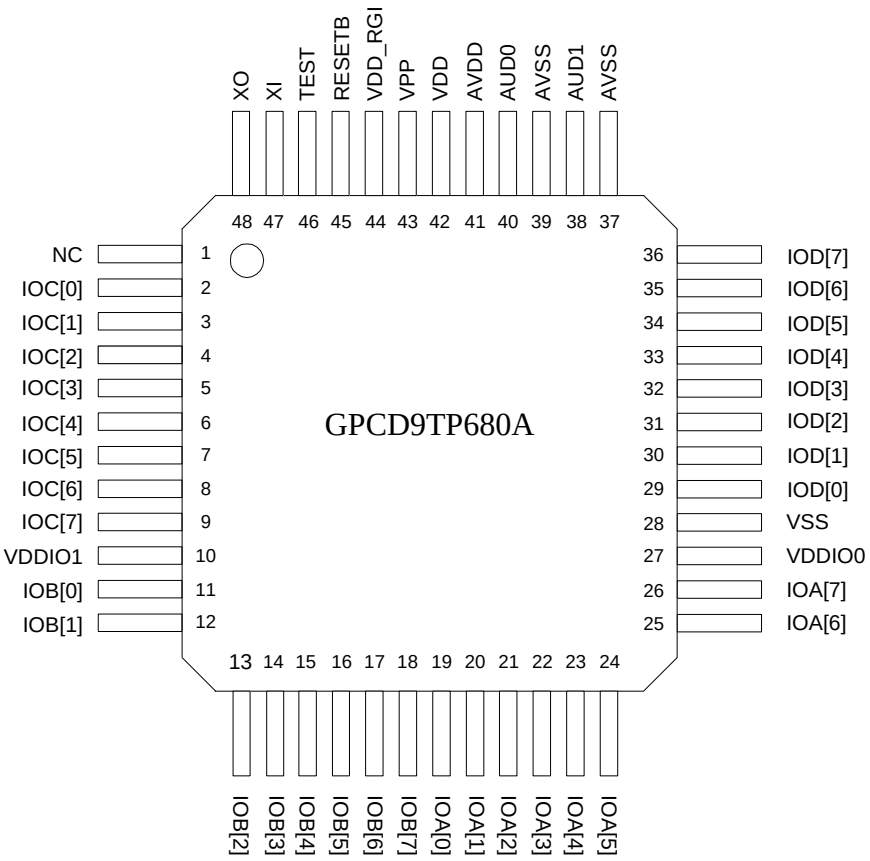
6. SIGNAL DESCRIPTION

6.1. Main Function Pin

Mnemonic	Type	Description
Dedicate IO		
VDDIO0	P	Power for IOA/IOD
VSSIO0	G	GND for all IOA/IOD
VDDIO1	P	Power for IOB/IOC
VSSIO1	G	GND for all IOB/IOC
IOA0~IOA7	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins. IOA1 shares with OTP_SDA; IOA2 share with OTP_SCK
IOB0~IOB7	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOC0~IOC7	I/O	IOC: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOD0~IOD7	I/O	IOD: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power		
VDD_RGI	P	Positive supply for regulator
VSS	G	Ground for Regulator
VDD	P	Power output from regulator out
Clock (max. frequency: 16Mhz)		
XI	O	Crystal input or connected to VDD through a resistor for ROSC
XO	O	Crystal output
Audio		
AVDD	P	Power for audio driver
AVSS	G	GND for audio driver
AUD0	O	Audio output shares with AUDP and IDAC0
AUD1	O	Audio output shares with AUDN and IDAC1
Other Signal		
TEST	I	TEST Mode selection pin, NC for normal application
RESETB	I	System reset pin (active low)
VPP	P	Internal OTP programming voltage, kept floating

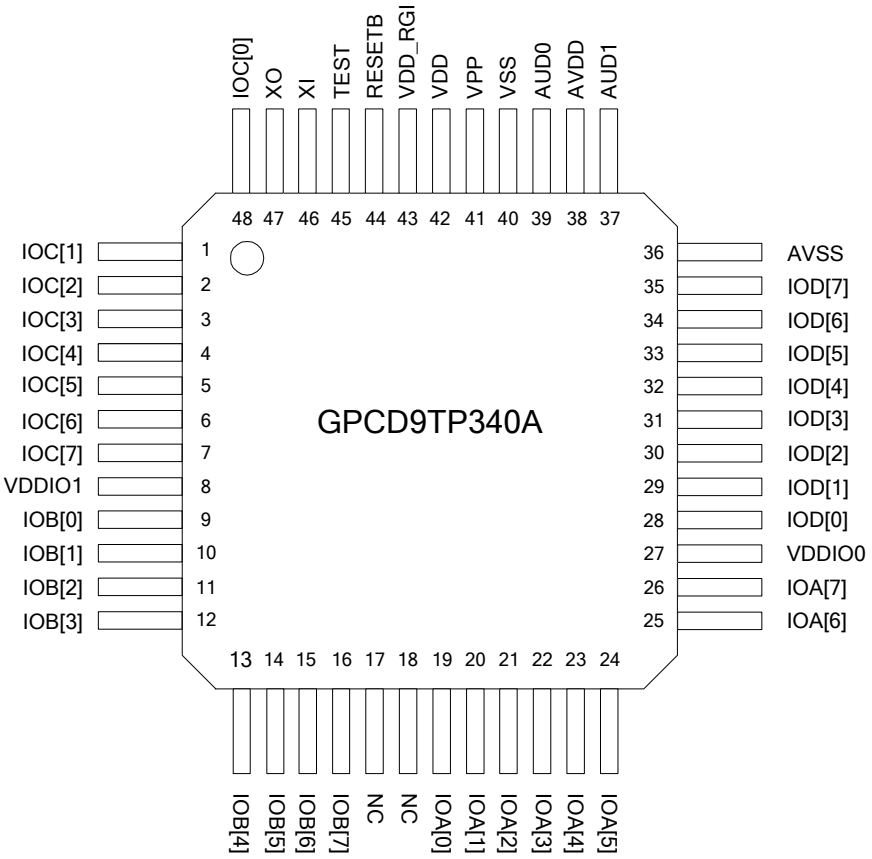
6.2. LQFP48 Package Pin Assignment

6.2.1. GPCD9TP680A



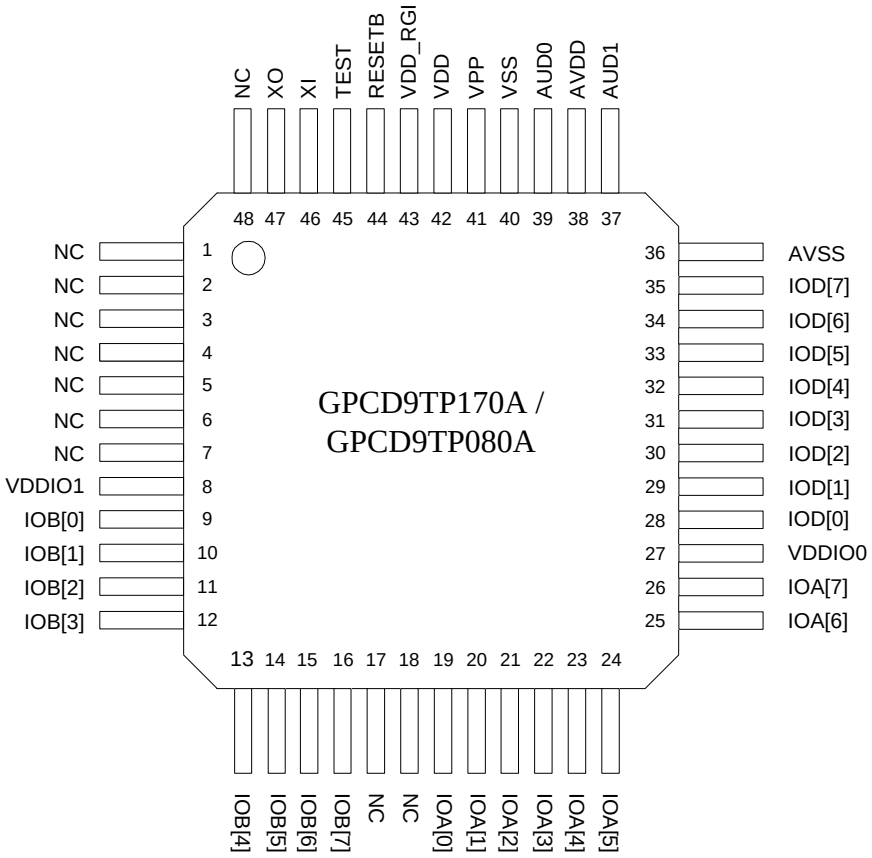
Mnemonic	Pin No. (LQFP48)	Type	Description
Dedicated IO			
VDDIO0	27	P	Power for IOA/IOD
VSSIO0	28	G	GND for all IOA/IOD
VDDIO1	10	P	Power for IOB/IOC
VSSIO1	28	G	GND for all IOB/IOC
IOA0~IOA7	19~26	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins. IOA1 shares with OTP_SDA; IOA2 share with OTP_SCK
IOB0~IOB7	11~18	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOC0~IOC7	2~9	I/O	IOC: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOD0~IOD7	29~36	I/O	IOD: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power			
VDD_RGI	44	P	Positive supply for regulator
VSS	28	G	Ground for regulator
VDD	42	P	Power output from regulator out
Clock(Max. Freq. 16Mhz)			
XI	47	O	Crystal input or connected to VDD through a resistor as ROSC
XO	48	O	Crystal output
Audio			
AVDD	41	P	Power for audio driver
AVSS	37, 39	G	GND for audio driver
AUD0	40	O	Audio output shares with AUDP and IDAC0.
AUD1	38	O	Audio output shares with AUDN and IDAC1.
Other Signal			
TEST	46	I	TEST Mode selection pin, NC for normal application
RESETB	45	I	System reset pin (active low)
VPP	43	P	Internal OTP programming voltage, kept floating

6.2.2. GPCD9TP340A



Mnemonic	Pin No. (LQFP48)	Type	Description
Dedicate IO			
VDDIO0	27	P	Power for IOA/IOD
VSSIO0	40	G	GND for all IOA/IOD
VDDIO1	8	P	Power for IOB/IOC
VSSIO1	40	G	GND for all IOB/IOC
IOA0~IOA7	19~26	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins. IOA1 shares with OTP_SDA; IOA2 share with OTP_SCK
IOB0~IOB7	9~16	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOC0~IOC7	48, 0~7	I/O	IOC: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOD0~IOD7	28~35	I/O	IOD: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power			
VDD_RGI	43	P	Positive supply for regulator
VSS	40	G	Ground for regulator
VDD	42	P	Power output from regulator out
Clock (Max. Freq. 16Mhz)			
XI	46	O	Crystal input or connected to VDD through a resistor as ROSC
XO	47	O	Crystal output
Audio			
AVDD	38	P	Power for audio driver
AVSS	36	G	GND for audio driver
AUD0	39	O	Audio output shares with AUDP and IDAC0.
AUD1	37	O	Audio output shares with AUDN and IDAC1.
Other Signal			
TEST	45	I	TEST Mode selection pin, NC for normal application
RESETB	44	I	System reset pin (active low)
VPP	41	P	Internal OTP programming voltage, kept floating

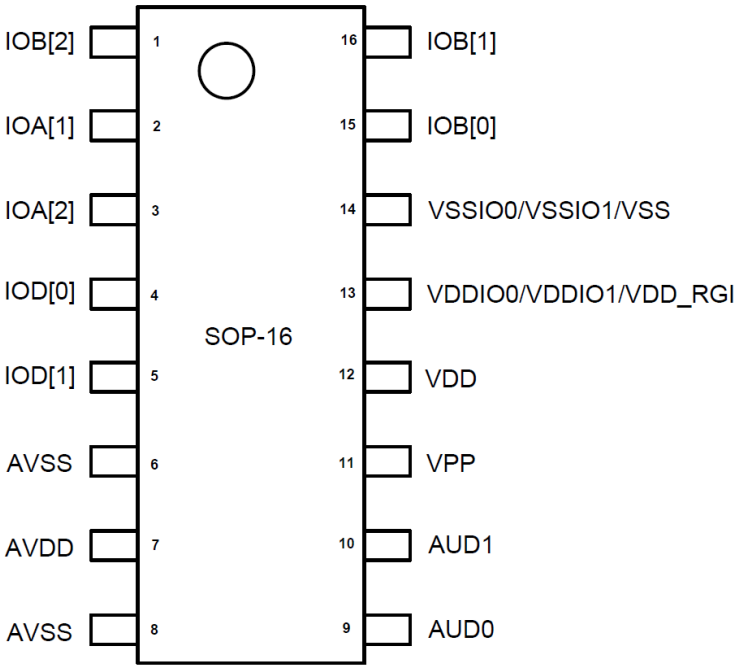
6.2.3. GPCD9TP170A/GPCD9TP080A:



Mnemonic	Pin No. (LQFP48)	Type	Description
Dedicate IO			
VDDIO0	27	P	Power for IOA/IOD
VSSIO0	40	G	GND for all IOA/IOD
VDDIO1	8	P	Power for IOB/IOC
VSSIO1	40	G	GND for all IOB/IOC
IOA0~IOA7	19~26	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins. IOA1 shares with OTP_SDA; IOA2 share with OTP_SCK
IOB0~IOB7	9~16	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOD0~IOD7	28~35	I/O	IOD: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power			
VDD_RGI	43	P	Positive supply for regulator
VSS	40	G	Ground for regulator
VDD	42	P	Power output from regulator out
Clock (Max. Freq. 16Mhz)			
XI	46	O	Crystal input or connected to VDD through a resistor as ROSC
XO	47	O	Crystal output
Audio			
AVDD	38	P	Power for audio driver
AVSS	36	G	GND for audio driver
AUD0	39	O	Audio output shares with AUDP and IDAC0.
AUD1	37	O	Audio output shares with AUDN and IDAC1.
Other Signal			
TEST	45	I	TEST Mode selection pin, NC for normal application
RESETB	44	I	System reset pin (active low)
VPP	41	P	Internal OTP programming voltage, kept floating

6.3. SOP16 Package Pin Assignment

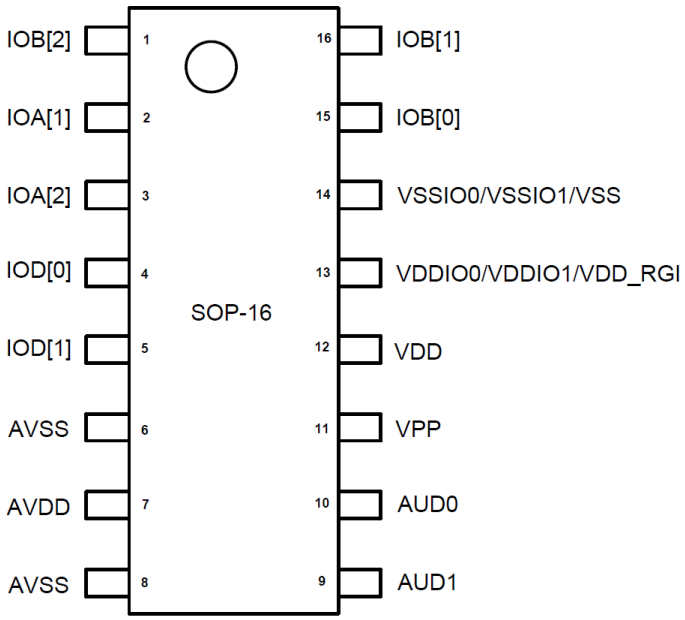
6.3.1. GPCD9TP680A



Mnemonic	Pin No. (SOP16)	Type	Description
Dedicate IO			
VDDIO0/VDDIO1	13	P	Power for IOA/IOB/IOC/IOD
VSSIO0/VSSIO1	14	G	GND for all IOA/IOB/IOC/IOD
IOA1~2	2~3	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins. IOA1 shares with OTP_SDA; IOA2 share with OTP_SCK
IOB0~IOB2	15~16,1	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOD0~IOD	4~5	I/O	IOD: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power			
VDD_RGI	13	P	Positive supply for regulator
VSS	14	G	Ground for regulator
VDD	12	P	Power output from regulator out
Audio			
AVDD	7	P	Power for audio driver
AVSS	6,8	G	GND for audio driver
AUD0	9	O	Audio output shares with AUDP and IDAC0.
AUD1	10	O	Audio output shares with AUDN and IDAC1.
Other Signal			
VPP	11	P	Internal OTP programming voltage, kept floating

Note1: only internal R-oscillator (only 16MHz available for IOSC) for system operating clock
Note2: without SPI application.

6.3.2. GPCD9T340A/GPCD9T170A/GPCD9TP080A



Mnemonic	Pin No. (SOP16)	Type	Description
Dedicate IO			
VDDIO0/VDDIO1	13	P	Power for IOA/IOB/IOC/IOD
VSSIO0/VSSIO1	14	G	GND for all IOA/IOB/IOC/IOD
IOA1~2	2~3	I/O	IOA: bi-directional I/O ports These pins can be programmed as wakeup I/O pins. IOA1 shares with OTP_SDA; IOA2 share with OTP_SCK
IOB0~IOB2	15~16,1	I/O	IOB: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
IOD0~IOD	4~5	I/O	IOD: bi-directional I/O ports These pins can be programmed as wakeup I/O pins.
Regulator - related power			
VDD_RGI	13	P	Positive supply for regulator
VSS	14	G	Ground for regulator
VDD	12	P	Power output from regulator out
Audio			
AVDD	7	P	Power for audio driver
AVSS	6,8	G	GND for audio driver
AUD0	10	O	Audio output shares with AUDP and IDAC0.
AUD1	9	O	Audio output shares with AUDN and IDAC1.
Other Signal			
VPP	11	P	Internal OTP programming voltage, kept floating

Note1: only internal R-oscillator (only 16MHz available for IOSC) for system operating clock
Note2: without SPI application.

7. FUNCTIONAL DESCRIPTIONS

7.1. SRAM

The 1024-byte SRAM (including Stack) area is located in $000000h~$0003FFh.

7.2. ROM

Up to 2M-byte of OTP ROM is available.

7.3. Low Voltage Reset

GPCD9TPXXXA features an important feature, Low Voltage Reset (LVR). With the LVR function, a reset signal is generated to reset system when the operating voltage drops under LVR. Without LVR, CPU becomes unstable and abnormal when working voltage is too low.

7.4. Interrupt

GPCD9TPXXXA has two interrupt (INT) modes: IRQ (interrupt Request) and NMI (Non-Mask Interrupt Request). The interrupt controller controls 20 IRQs and 6 NMIs. A NMI cannot be interrupted by any other IRQ.

Interrupt Source	Interrupt Name	Priority
Timer A	NMI_TIMER_A	NMI
Timer B	NMI_TIMER_B	NMI
Timer C	NMI_TIMER_C	NMI
CPU_CLOCK/1024	NMI_D1024	NMI
CPU_CLOCK/4096	NMI_D4096	NMI
EXT	NMI_EXT	NMI
Timer A	IRQ_TIMER_A	IRQ1
Timer B	IRQ_TIMER_B	IRQ2
Timer C	IRQ_TIMER_C	IRQ3
CPU_CLOCK/1024	IRQ_D1024	IRQ4
CPU_CLOCK/4096	IRQ_D4096	IRQ5
16 Hz	IRQ_16Hz	IRQ6
TBL	IRQ_TBL	IRQ7
KEY	IRQ_KEY	IRQ8
EXT	IRQ_EXT	IRQ9
SPU	IRQ_SPU	IRQ10
SPI	IRQ_SPI	IRQ11
QD1_F	IRQ_QD1_F	IRQ12
QD1_B	IRQ_QD1_B	IRQ13
QD2_F	IRQ_QD2_F	IRQ14
QD2_B	IRQ_QD2_B	IRQ15
CTS_TMA	IRQ_CTS_TMA	IRQ16
CTS_TMB	IRQ_CTS_TMB	IRQ17
SPUFIFO	IRQ_SPUFIFO	IRQ18
CMPIO	IRQ_CMPIO	IRQ19

7.5. Hardware PWMIO

Hardware PWMIO supports 12 LED outputs (IOA[3:0],IOB[3:0], IOD[7:4]) with 256-level brightness control. The clock source of PWMIO can be selected by user's request.

7.6. I/O

The purpose of input and output ports is to communicate with other devices. Four programmable I/O ports are built-in, including Port A, B, C, and D. All Ports are general I/O with programmable wake-up capability and pull low function. In addition to general I/O function, I/O also provides some special functions in certain pins.

7.7. Timer/Counter (Timer A/Timer B/Timer C)

Three 12-bit timers are embedded in GPCD9TPxxxA : Timer A, Timer B and Timer C. These three timers all have 12-bit up counter and a preload register and programmable clock source. Timer A/B can also be the clock source of the software channel 1/2 respectively. The clock source of each timer can be set individually. Two clock sources, including CPU clock and external clock, can be selected individually or their combination to be timer's clock source. Besides, capture and comparison function are supported by TMA. Comparison is supported by TMB and TMC.

7.8. Sleep, Wakeup and Watchdog

7.8.1. Sleep and Wakeup

Sleep mode is to save power by stopping clock while device is not in use. When sleep acts, the device runs from operating mode to standby mode. Wake-up from sleep mode is to turn back to operating mode.

(1) Sleep: After power on reset, IC starts working until a sleep command is given. When a sleep signal is accepted, IC will turn off system clock and enter sleep mode.

(2) Wake-up: While a wakeup signal is generated, GPCD9TPxxxA is waking up from sleep mode. While wake-up completed, program counter will continue to execute the next command.

7.8.2. Watchdog

The purpose of watchdog is to monitor system's operation normally. Within a certain period, watchdog must be cleared. It protects the system from incorrect code execution by generating a system reset when software is failed to clear watchdog flag within around 0.67 seconds.

7.9. Speech and DAC

The GPCD9TPXXXA uses a high performance SPU voice engine to archive 8-channel voice with ADPCM/PCM code. The SPU also supports automatic zero-crossing concatenating function. A hardware multiplier is also embedded in this SPU for software using. Moreover, two 14-bit software channels with noise filter is also supported. There is one 14-bit PWM driver for direct audio output and two 12-bit current DACs for stereo.

In 14-bit PWM application, the long traces will cause EMI issue. Usually the ferrite bead filters and capacitors are used to reduce the high frequency emissions. The suggested layout guide, please reference to section 9.1、9.2 and PCB layout guideline file.

7.10. Comparator

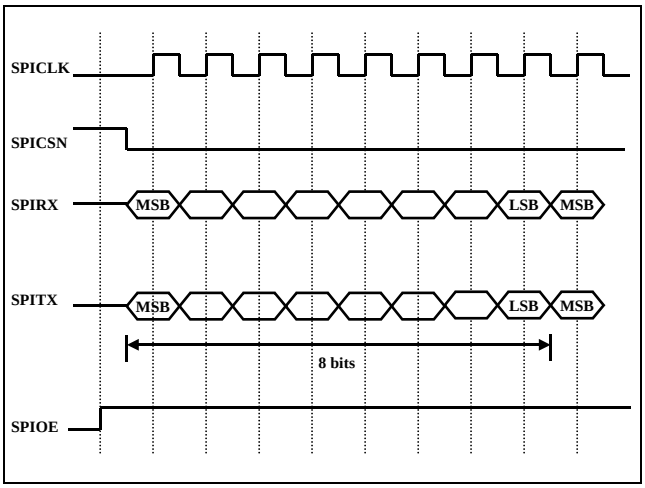
A set of comparator is embedded in GPCD9TPXXXA. Users can using the comparator to sample specific signal.

7.11. Capacitive Touch Sensor (CTS) and CTS Timers

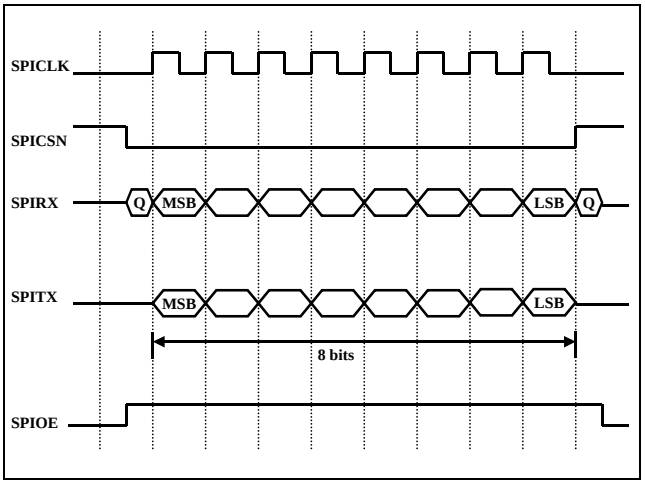
GPCD9TPXXXA provides hardware Capacitive Touch Sensor. It provide that the ability to perform capacitive sensing, decision making, responsive actions and other duties pertinent to the system as well.

7.12. SPI Controller

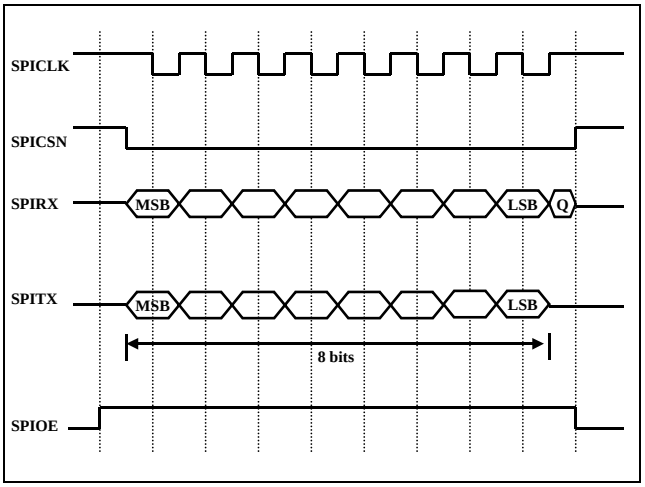
A Serial Peripheral Interface (SPI) controller is built-in GPCD9TPXXXA to facilitate communicating with other devices and components. There are four control signals on SPI including SPITX(SDO), and SPIRX(SDI), SPICLK(SCK) and SPICSN; the four signals are shared with PortA3, PorA2, PortA1 and PortA0 or PortB7, PortB6, PortB5 and PortB4 or PortC3, PortC2, PortC1 and PortC0 or PortD3, PortD2, PortD1 and PortD0. While SPI module is enabled by corresponding control bit. These four pins cannot be GPIOs and any setting on corresponding GPIO control register will have no effect. Four types of timing are supported as follows:



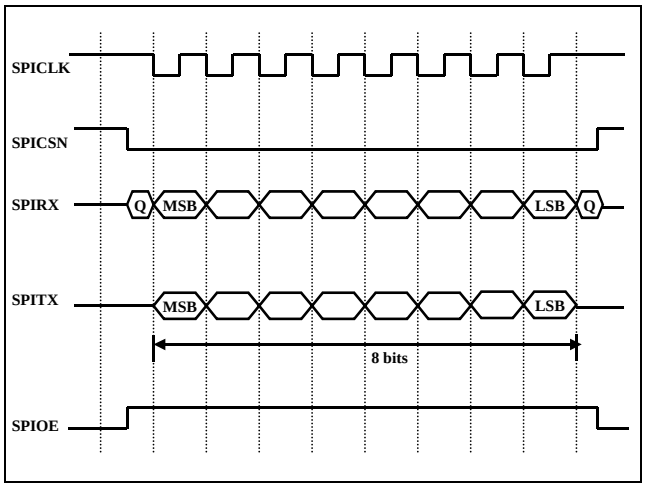
Master Mode, SPO = 0, SPH=0



Master Mode, SPO = 0, SPH=1



Master Mode, SPO = 1, SPH=0



Master Mode, SPO = 1, SPH=1

8. ELECTRICAL SPECIFICATIONS

8.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	0℃ to +70℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions see DC Electrical Characteristics.

8.2. DC Characteristics (VDDIO/VDD_RGI=3.0V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	3.0	3.6	V	For 2-battery
Operating Current-1	I_{OP1}	-	8	11	mA	VDDIO/AVDD /VDD_RGI=3.0V F_{CPU} = 8MHz , PWM on, no load
Operating Current-2	I_{OP2}	-	6	8	mA	VDDIO/AVDD /VDD_RGI=3.0V F_{CPU} = 8MHz , PWM off, no load
Standby Current	I_{STBY}	-	-	7	μA	VDDIO/AVDD/VDD_RGI=3.0V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDDIO/AVDD/VDD_RGI=3.0V
Input High Level-1	V_{IH}	0.7*VDDIO	-	-	V	With Schmitt trigger
Input Low Level-1	V_{IL}	-	-	0.3*VDDIO	V	With Schmitt trigger
Input High Level-2	V_{IH}	0.6*VDDIO	-	-	V	Without Schmitt trigger
Input Low Level-2	V_{IL}	-	-	0.4*VDDIO	V	Without Schmitt trigger
Output High Current (IOA/B/C/D[7:0])*	I_{OH}	3.5	5	6.5	mA	VDDIO/AVDD/VDD_RGI=3.0V, V_{OH} =2.1V
Output Low Sink Current (IOA/B/C[7:4], IOC/D[3:0])	I_{OL1}	7	10	13	mA	VDDIO/AVDD/VDD_RGI=3.0V, V_{OL} =0.9V
Output Low Sink Current (IOA/B[3:0], IOD[7:4])	I_{OL2}	10	20	30	mA	VDDIO/AVDD/VDD_RGI=3.0V, V_{OL} =0.9V
Input Pull-Low Resistor-1 (IOA/B/C/D[7:0])	R_{PL}	550	800	1100	Kohm	VDDIO/AVDD/VDD_RGI=3.0V, Vin=3.0V
Input Pull-Low Resistor-2 (IOA/B/C/D[7:0])	R_{PL}	55	80	110	Kohm	VDDIO/AVDD/VDD_RGI=3.0V, Vin=3.0V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PH}	55	80	110	Kohm	VDDIO/AVDD/VDD_RGI=3.0V, Vin=VSS
IROSC16M Frequency deviation for chip (lot deviation) **	F_{I16M}	-1	-	+1	%	VDDIO/AVDD/VDD_RGI=3.0V
IROSC16M Frequency deviation for LQFP48	$F_{I16M-LQFP48}$	-3	-	+3	%	VDDIO/AVDD/VDD_RGI=3.0V
EROSC16M Frequency deviation(lot deviation)	F_{E16M}	-7	-	+7	%	VDDIO/AVDD/VDD_RGI=3.0V

***Note:** IOC[7:0] are available on GPCD9T680A/GPCD9TP340A.

****Note:** IROSC16M Frequency deviation is without epoxy on chip.

8.3. DC Characteristics (VDDIO/VDD_RGI=4.5V, TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.2	4.5	5.5	V	For 3-battery
Operating Current-1	I_{OP1}	-	11	15	mA	VDDIO/AVDD/VDD_RGI=4.5V F_{CPU} = 8MHz , PWM on, no load
Operating Current-2	I_{OP2}	-	7	10	mA	VDDIO/AVDD/VDD_RGI=4.5V F_{CPU} = 8MHz , PWM off, no load
Standby Current	I_{STBY}	-	-	7	μA	VDDIO/AVDD/VDD_RGI=4.5V
OSC Frequency	F_{OSC}	-	-	16	MHz	VDDIO/AVDD/VDD_RGI=4.5V
Input High Level-1	V_{IH}	0.7*VDD	-	-	V	With Schmitt trigger
Input Low Level-1	V_{IL}	-	-	0.3*VDD	V	With Schmitt trigger
Input High Level-2	V_{IH}	0.6*VDD	-	-	V	Without Schmitt trigger
Input Low Level-2	V_{IL}	-	-	0.4*VDD	V	Without Schmitt trigger
Output High Current (IOA/B/C/D[7:0])	I_{OH}	7	10	13	mA	VDDIO/AVDD/VDD_RGI=4.5V, V_{OH} =3.15V
Output Low Sink Current (IOA/B/C[7:4], IOC/D[3:0])	I_{OL1}	14	20	26	mA	VDDIO/AVDD/VDD_RGI=4.5V, V_{OL} =1.35V
Output Low Sink Current (IOA/B[3:0], IOD[7:4])	I_{OL2}	20	40	60	mA	VDDIO/AVDD/VDD_RGI=4.5V, V_{OL} =1.35V
Input Pull-Low Resistor-1 (IOA/B/C/D[7:0]) *	R_{PL}	550	800	1100	Kohm	VDDIO/AVDD/VDD_RGI=4.5V, Vin=4.5V
Input Pull-Low Resistor-2 (IOA/B/C/D[7:0]) *	R_{PL}	55	80	110	Kohm	VDDIO/AVDD/VDD_RGI=4.5V, Vin=4.5V
Input Pull-High Resistor (IOA/B/C/D[7:0])	R_{PH}	55	80	110	Kohm	VDDIO/AVDD/VDD_RGI=4.5V, Vin=VSS
IROSC16M Frequency deviation for chip (lot deviation)**	F_{I16M}	-1	-	+1	%	VDDIO/AVDD/VDD_RGI=4.5V
IROSC16M Frequency deviation for LQFP48	$F_{I16M-LQFP48}$	-3	-	+3	%	VDDIO/AVDD/VDD_RGI=4.5V
EROSC16M Frequency deviation(lot deviation)	F_{E16M}	-7	-	+7	%	VDDIO/AVDD/VDD_RGI=4.5V

***Note:** IOC[7:0] are available on GPCD9T680A/GPCD9TP340A.

****Note:** IROSC16M Frequency deviation is without epoxy on chip.

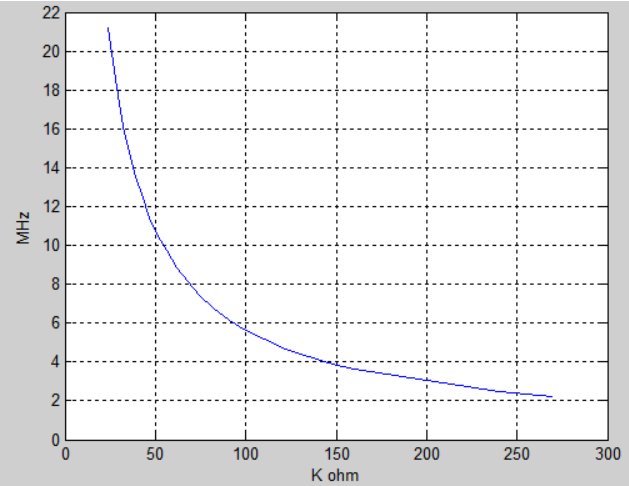
8.4. Audio PWM Characteristics (VDDIO/VDD_RGI/AVDD =4.5V, R_L=8Ω, f=1KHz, TA=25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
DAC Resolution	RESO	-	-	14	bit
THD+n(5V@0.7W)	--	-	1	-	%
Noise at No Signal	-	-	-100	-	dBr A
Dynamic Range (-60dB)	-	-	-80	-	dBr A

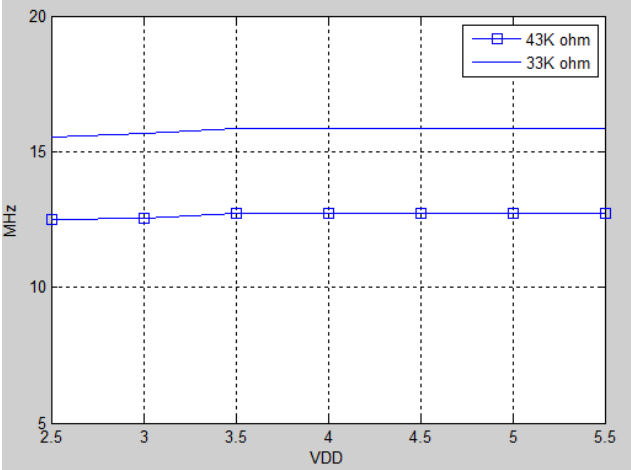
8.5. Regulator Characteristics (TA=25℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Input Voltage	VREGI	2.1	-	5.5	V	
Maximum Current Output	IREGO	-	-	40	mA	VDD_RGI (Regulator in)= 4.5V,△VDD (Regulator out) <100mV
Output Voltage	V3_REGO	3.14	3.3	3.47	V	VDD_RGI > 3.5V and V3_REGO is 3.3V
Standby Current	IREGS	-	2.5	-	uA	

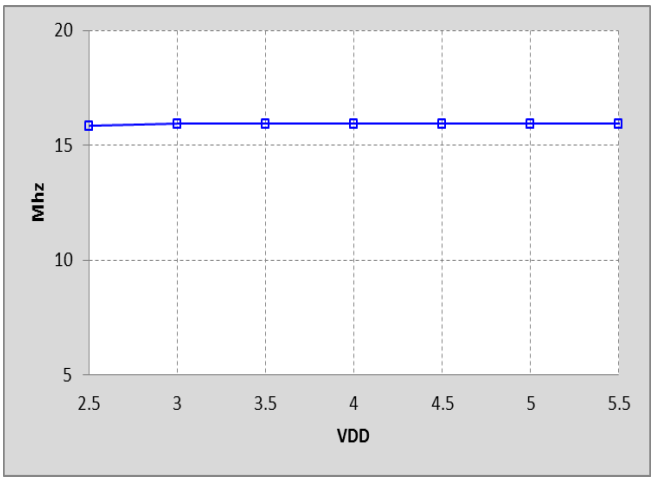
8.6. The EROSC Relationship between R_{osc} and F_{osc} (TA=25℃)



8.7. The EROSC Relationship between VDD and F_{osc} (TA=25℃)

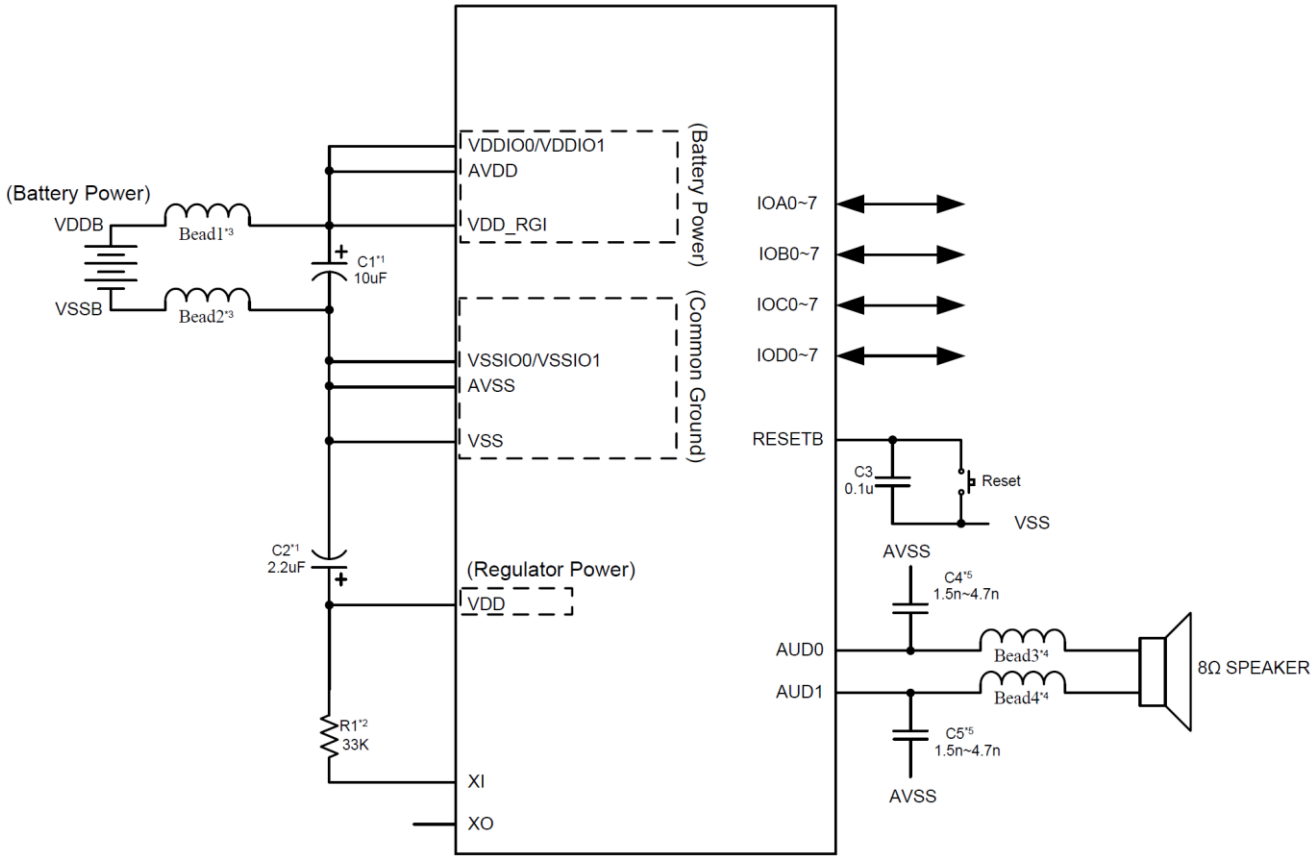


8.8. The IROSC Relationship between VDD and F_{osc} (TA=25℃)



9. APPLICATION CIRCUITS

9.1. GPCD9TPXXXA Application Circuit with External ROSC Mode (R_{OSC}-mode)



Note*1: These capacitor values are for design guidance only. Adding 10uF and 0.1uF capacitors in parallel to each power group are recommended for noise sensitive application. The recommended features are ESR=0.05~1Ω

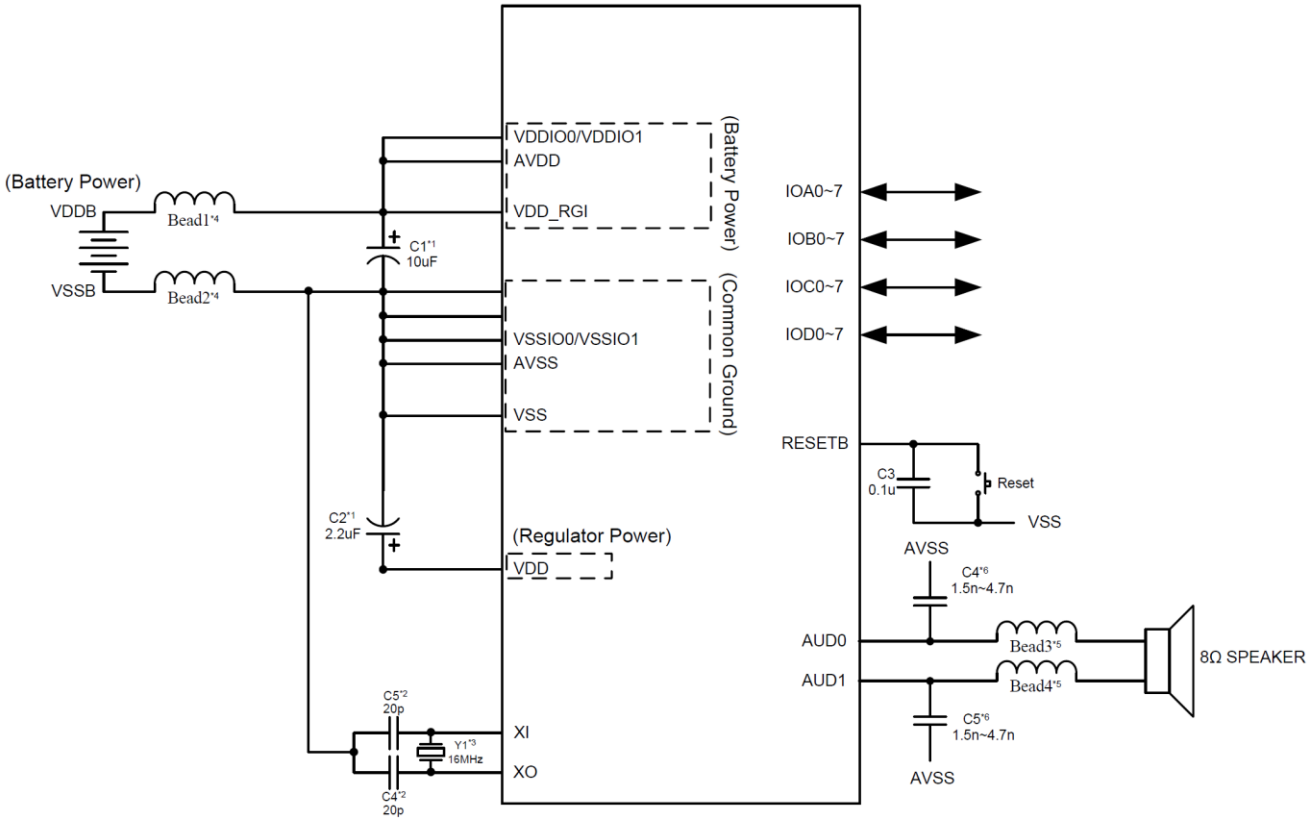
Note*2: R1=33K ohm for 16MHz clock and R1=43K ohm for 12MHz clock.

Note*3: Bead1/2 are optional for EMI sensitive application. The beads are used to reduce the high frequency emissions. For better EMI performance select bead which offers highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. **Bead1/2 should be as close as possible to VDDB/VSSB/AVSS.**

Note*4: Bead3/4 are optional for EMI sensitive application. If bead1/2 don't reduce the EMI effectively, please add bead3/4 to enhance EMI performance. **Bead3/4 should be as close as possible to AUD0/AUD1/AVSS.**

Note*5: The typical value of C4/5 is 1.5nF, and could be modified in different loading. C4/5 should be as close as possible to AUD0/AUD1/AVSS.

9.2. GPCD9TPXXXA Application Circuit with 16MHz X'tal (XTAL-mode)



Note*1: These capacitor values are for design guidance only. Adding 10uF and 0.1uF capacitors in parallel to each power group are recommended for noise sensitive application. The recommended features are ESR=0.05~1Ω

Note*2: These capacitor values are for design guidance only. The recommended features are ESR=11.2~60K and C4=C5=18~28pF (including PCB parasitic loading, for example, user should apply additional 12~22pF on XI and XO if PCB parasitic loading is 6pF)

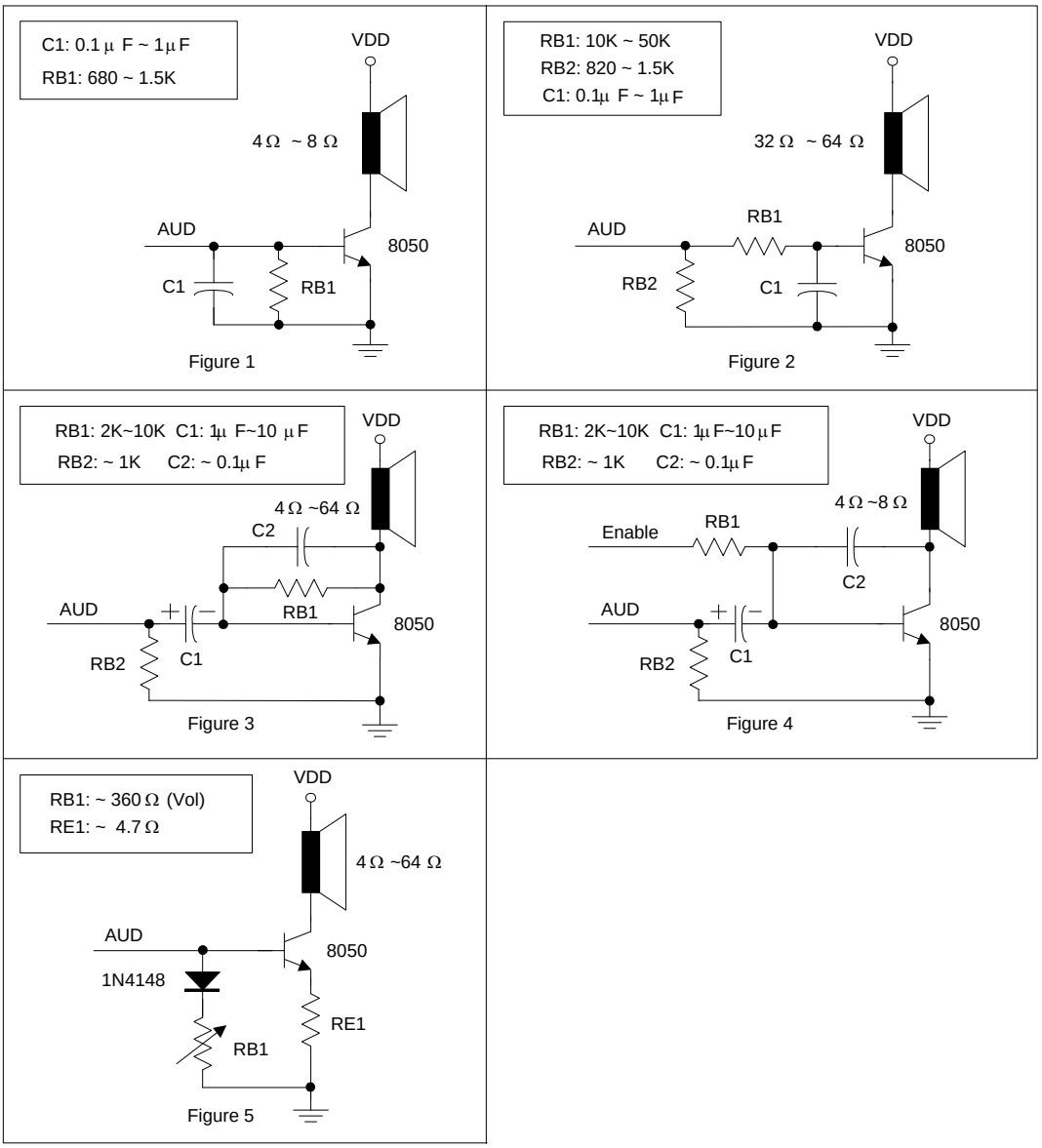
Note*3: 16MHz X'tal or 12Mhz X'tal can be used for different speed applications.

Note*4: Bead1/2 are optional for EMI sensitive application. The beads are used to reduce the high frequency emissions. For better EMI performance select bead which offers highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. **Bead1/2 should be as close as possible to VDDB/VSSB/AVSS.**

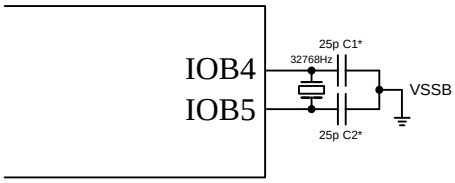
Note*5: Bead3/4 are optional for EMI sensitive application. If bead1/2 don't reduce the EMI effectively, please add bead3/4 to enhance EMI performance. **Bead3/4 should be as close as possible to AUD0/AUD1/AVSS.**

Note*6: The typical value of C4/5 is 1.5nF, and could be modified in different loading. **C4/5 should be as close as possible to AUD0/AUD1/AVSS.**

9.3. GPCD9TPXXXA Current DAC Application Circuit



9.4. GPCD9TPXXXA 32K X'tal Application Circuit



Note*: These capacitor values are for design guidance only. The recommended 32K XTAL features are ESR=11.2~60K and C1=C2 =26~36pF (including PCB parasitic loading, for example, user should apply additional 20~30pF on X32I and X32O if PCB parasitic loading is 6pF)

10. PACKAGE/PAD LOCATIONS

10.1. Ordering Information

Product Number	Package Type
GPCD9TPXXXA-NnnV-C	Chip form
GPCD9TPXXXA-NnnV-QL23x	Green Package – LQFP48
GPCD9TPXXXA-NnnV-HS03x	Green Package – SOP16

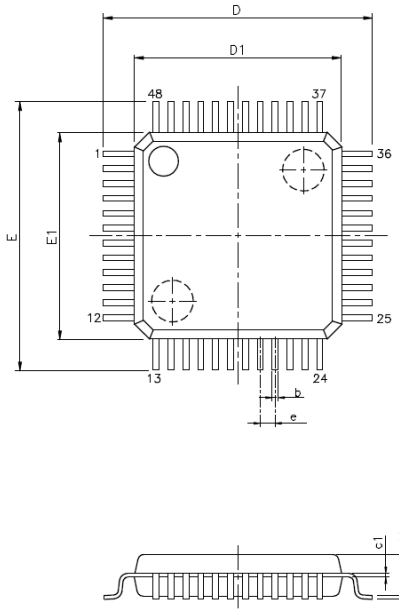
Note1: Code number is assigned for customer.

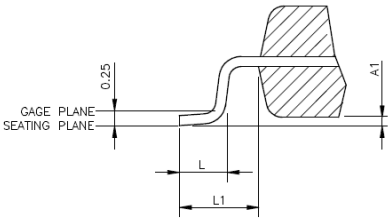
Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

Note3: Package form number (x = 1 - 9, serial number).

10.2. Package Information

10.2.1. LQFP 48





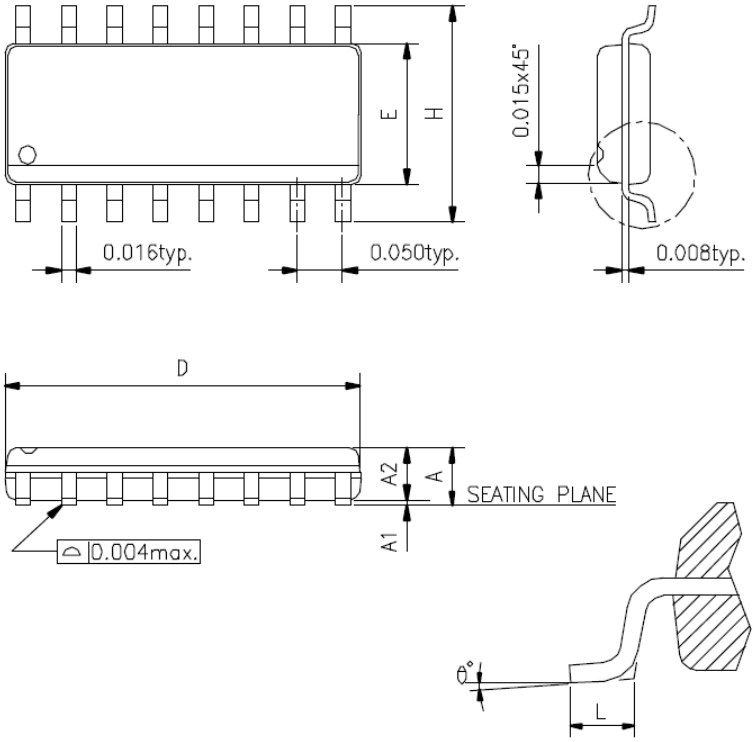
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:

1. JEDEC OUTLINE:MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

10.2.2. SOP 16



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1. JEDEC OUTLINE : MS-012 AC
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

11. DISCLAIMER

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12. REVISION HISTORY

Date	Revision #	Description	Page
May 24, 2019	1.5	1. Remove NMI → SPUFIFO 2. Modify 8.1 Operating Temperature range	4,16 19
Mar. 14, 2018	1.4	Add GPCD9TP080A information.	6,12,15
Dec. 28, 2017	1.3	1.Modify Feature for Peripherals information. 2.Modify SIGNAL DESCRIPTIONS 3.Add Package SOP-16 information. 4.Modify DC Characteristics for IROSC16M/EROSC16M Frequency deviation and notes. 5.Modify FUNCTIONAL DESCRIPTIONS for Speech and DAC information. 6.Modify Audio PWM Characteristics. 7.Add The IROSC16M Relationship between VDD and FOSC. 8. Modify APPLICATION CIRCUITS for EMI effects.	4, 7,8,10,12 14,15,27, 28, 19,20, 17, 20, 22, 23,24
Sep. 28, 2017	1.2	Add GPCD9TP680A information.	6, 8
Aug. 15, 2017	1.1	1.Correct Block Diagram. 2.Add IROSC16M and EROSC specification. 3.Modify application circuits notices.	5, 19, 23,24
Jun. 20, 2017	1.0	Original	24