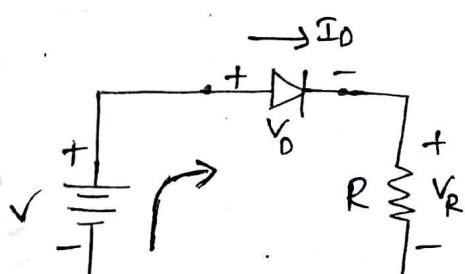
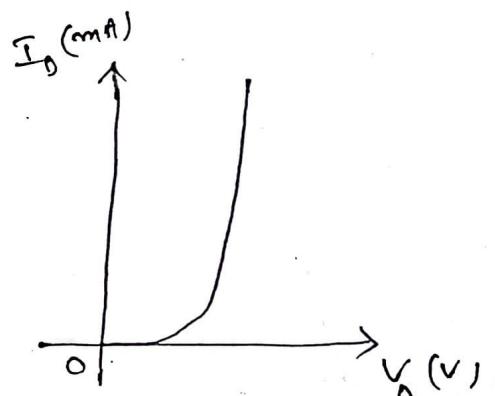


TRANSISTOR BIASING AND STABILIZATIONLoad Line Analysis:

- The applied load will normally have an important impact on the point or region of operation of the device. If the analysis is performed in a graphical manner, a line can be drawn on the characteristics of the device that represents the applied load.
- The intersection of the load line with the characteristics will determine the point of operation of the system. Such an analysis is called "load line analysis".
- Consider a network shown in figure 'a' employing a diode having characteristics shown in figure 'b'. Now consider the region of interest which is forward biased region.



(a)



(b)

- Apply KVL to the series circuit will result in

$$V = V_D + I_D R \quad \rightarrow ①$$

- The intersections of the load line on the characteristics can easily be determined if one simply employs that anywhere on the horizontal axis $I_D = 0$ A and anywhere on the vertical axis $V_D = 0$ V

→ if we set $V_D = 0V$ in Eq ① and solve for I_D .

$$V = RI_D + V_D$$

$$V = I_D R + (0V)$$

$$\boxed{I_D = \frac{V}{R} \quad | \quad V_D = 0V}$$

→ if we set $I_D = 0A$, in Eq ① and solve for V_D .

$$V = V_D + I_D R$$

$$V = V_D + (0A) R$$

$$\boxed{V_D = V \quad | \quad I_D = 0A}$$

→ now indicate these two points on characteristics curve. A straight line drawn between the two points will define the load line as shown below.

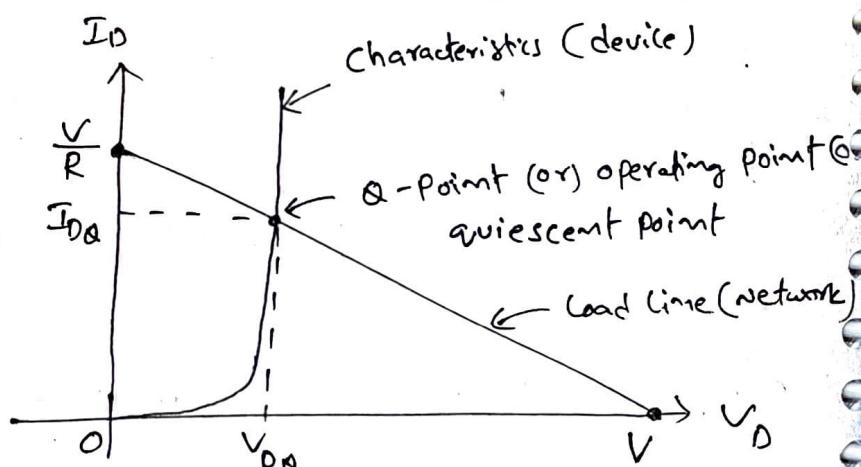
→ Change the level of ' R ', and intersection on vertical axis will change. The Result will be a change in the slope of the load line

→ Load Line Generally defined by network.

→ The point of intersection b/w load line and characteristic curve is the point of operation for the circuit shown in figure 'a'.

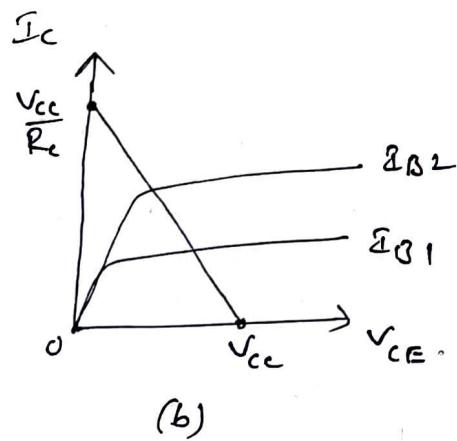
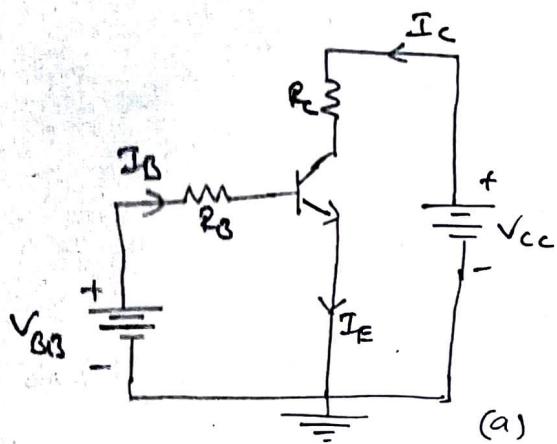
→ By simply drawing a line down to the Horizontal axis the diode voltage V_{DQ} can be determined, whereas a horizontal line from the point of intersection to the vertical axis will provide the level of I_{DQ} .

→ The point of operation is usually called the Quiescent point (or) operating point (or) Q point to reflect its "still unmoving qualities defined by network."



OC Load Line Analysis for Transistor:-

→ With the help of DC load line, we can easily analyse the performance of an amplifier circuit.



→ Consider the CE n-p-n Transistor circuit shown above Figure (a). Applying KVL to the collector portion of the circuit, we have

$$V_{CC} = I_C R_C + V_{CE}$$

$$\begin{aligned} I_C R_C &= V_{CC} - V_{CE} \\ \frac{V_{CC} - V_{CE}}{R_C} &= m \alpha + c \\ I_C &= \left(-\frac{1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C} \rightarrow \textcircled{1} \end{aligned}$$

Eq \textcircled{1} is in the form of straight line equation $y = mx + c \rightarrow \textcircled{2}$

Comparing Eq \textcircled{1} & Eq \textcircled{2}, slope of the straight line is $m = -\frac{1}{R_C}$

→ Therefore, if Eq \textcircled{1} is plotted on the output characteristic curves, we will get a straight line having slope equal to $-\frac{1}{R_C}$ and intercepts on Vertical axis equal to $\frac{V_{CC}}{R_C}$ and on Horizontal axis at equal to V_{CC} .

"The line plotted by joining these two points on the output characteristics is called DC load line."

This is shown in Figure (b).

→ Let us see how to plot a DC load line for a Transistor circuit.

→ From figure(a), the value of Collector-Emitter voltage V_{CE} is given as

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C \rightarrow ③$$

(i) when $I_C = 0$, then V_{CE} is maximum and is equal to V_{CC} i.e

$$\text{max. } V_{CE} = V_{CC} - 0 \cdot R_C$$

$$\boxed{\text{max. } V_{CE} = V_{CC}} \rightarrow ④$$

This condition gives the point on V_{CE} axis as shown in Figure b.

(ii) when $V_{CE} = 0$, the collector current is maximum and is given as $\frac{V_{CC}}{R_C}$.

i.e

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_{CC} = I_C R_C$$

$$\boxed{\text{max. } I_C = \frac{V_{CC}}{R_C}} \rightarrow ⑤$$

This condition gives the point on I_C axis.

By joining these two points, DC load line is constructed.

"This line is called DC load line because its slope depends upon the value of resistor R_C which is the DC load of the circuit"

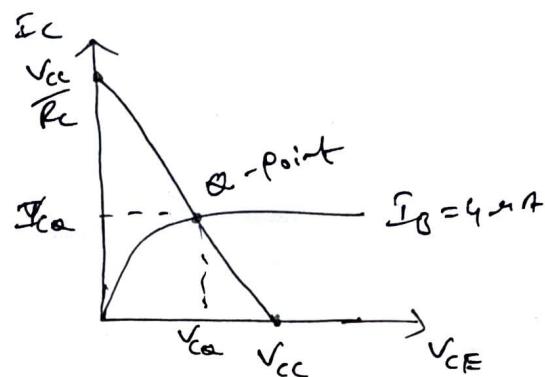
operating point:

→ The zero signal values (no AC signal is applied) of I_C and V_{CE} are known as the operating point.

→ It is called operating point because the variations of I_C & V_{CE} take place about this point when AC signal is applied.

→ It is also called Quiescent (Silent) point or Q-point because it is the point on I_C - V_{CE} characteristics when transistor is silent (i.e no AC signal is applied).

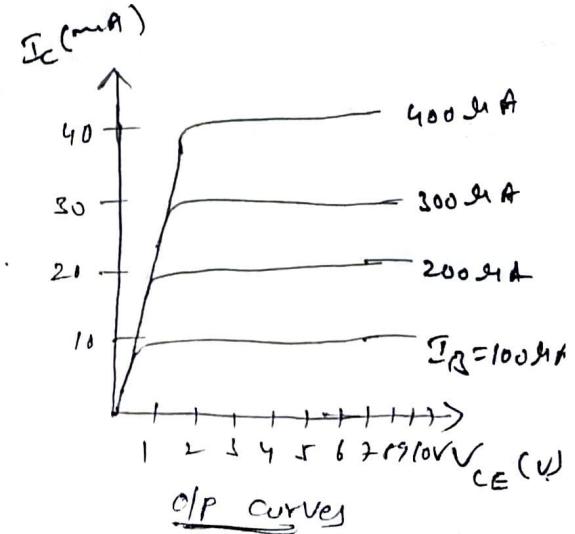
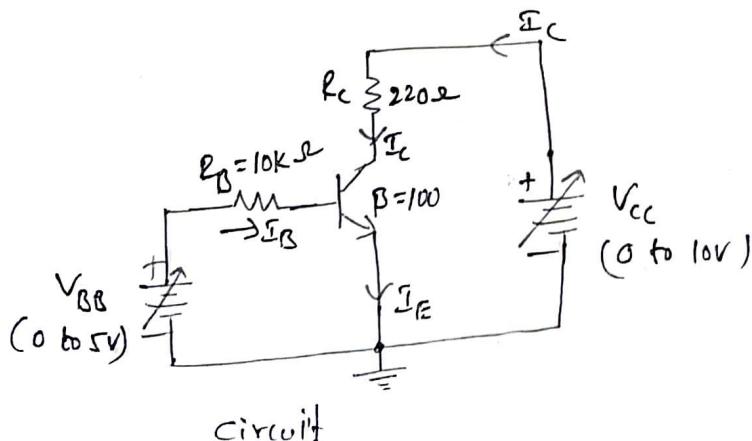
→ Suppose in the absence of AC signal, assume $I_B = 4mA$. Then I_C and V_{CE} conditions in the circuit must be represented by some point on I_B characteristic curve. But I_C and V_{CE} conditions in the circuit should also be represented by some point on DC load line. The point α where the load line and characteristic curve intersect is the only point which satisfies both these conditions.



Selection of operating point:

- For faithful amplification of input signal, a proper selection of operating point is very important.
- To get faithful amplification, proper biasing is given at I/p & O/p circuit which establishes the DC operating point for proper operation of the amplifier.
- If an amplifier not biased with correct DC voltages, we don't get proper operating point, so that transistor can go into saturation or cut off region when an input AC signal is applied.

→ Let see the circuit given below,



→ let us examine ~~the~~ what happens to I_c and V_{CE} , at different values of I_B .

(i) Take $I_B = 200 \mu A$, $\beta = \frac{I_c}{I_B} \Rightarrow I_c = 200 \times 10^{-6} \times 100 = 20 \text{ mA}$

then

$$V_{CC} = I_c R_C + V_{CE}$$

$$\begin{aligned} V_{CE} &= V_{CC} - I_c R_C \\ &= 10 - (20 \times 10^{-3}) (220 \Omega) \\ &= 5.6 \text{ V} \end{aligned}$$

$$Q_1 = (5.6 \text{ V}, 20 \text{ mA})$$

(ii) $I_B = 300 \mu A$, $I_c = 300 \times 10^{-6} \times 100 = 30 \text{ mA}$

$$V_{CE} = 10 - 30 \times 10^{-3} \times 220 = 3.4 \text{ V}$$

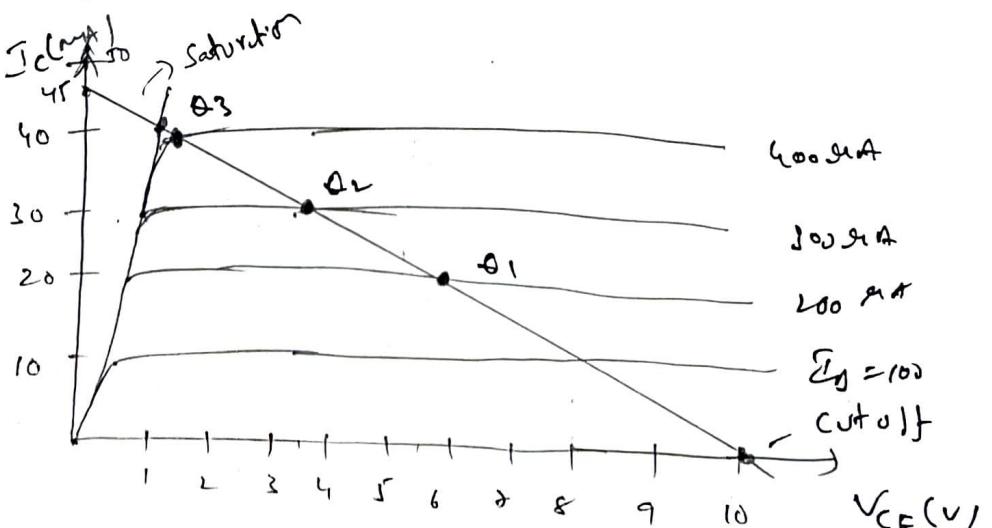
$$Q_2 = (3.4 \text{ V}, 30 \text{ mA})$$

(iii) $I_B = 400 \mu A$, $I_c = 400 \times 10^{-6} \times 100 = 40 \text{ mA}$

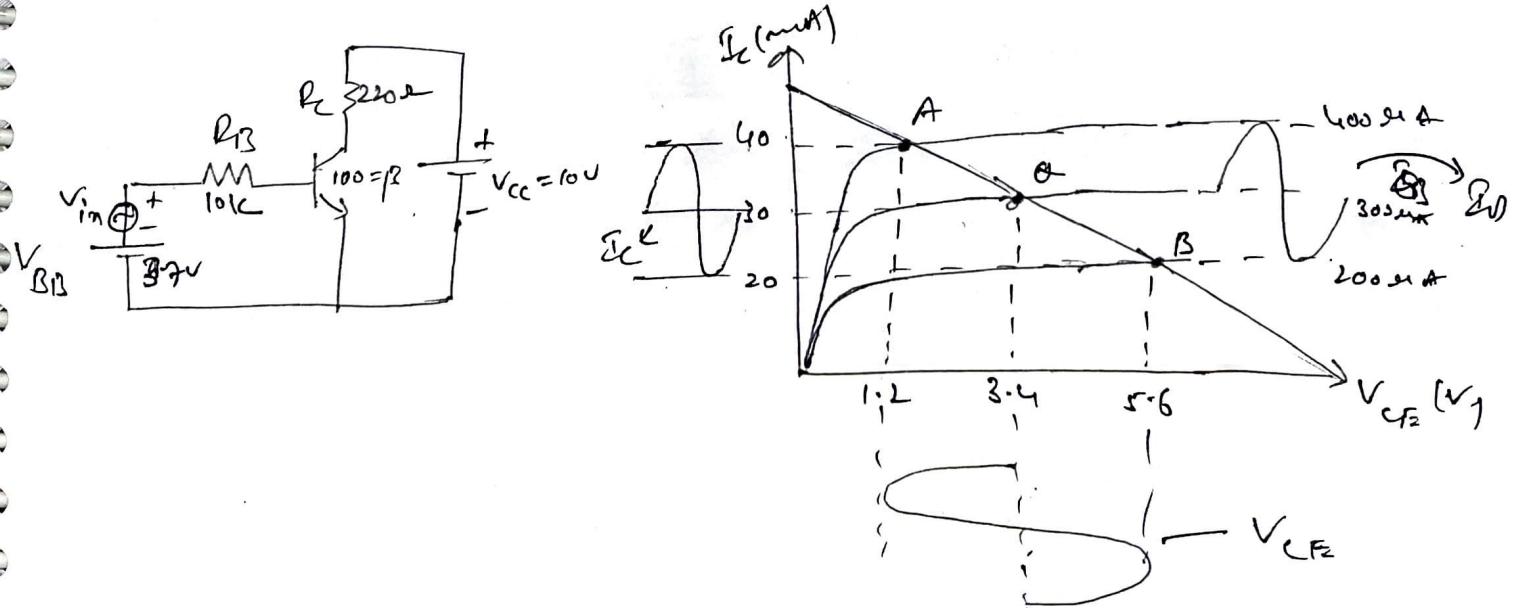
$$V_{CE} = 10 - 40 \times 10^{-3} \times 220 = 1.2 \text{ V}$$

$$Q_3 = (1.2 \text{ V}, 40 \text{ mA})$$

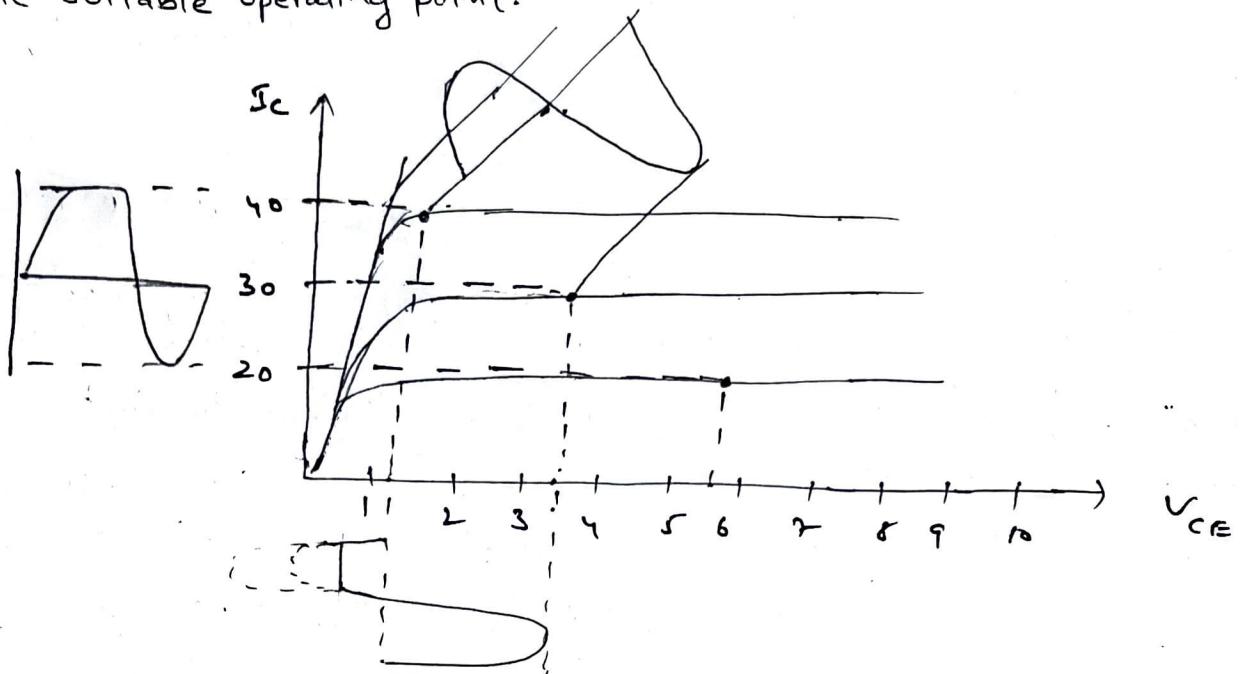
now plot these three points on characteristic curve



- now draw a line which joins these three points & it intersects I_C axis at $\frac{V_{CC}}{R_C}$ & at V_{CC} on V_{CE} axis.
- The AC load line intersects the V_{CE} axis at 10V, the point where V_{CE} = V_{CC}. This is the transistor cut-off point because I_B and I_C are zero Ideally.
- DC load line intersects the I_C at 45.45 mA (≈ 45.5 mA). This is the Transistor Saturation point because I_C is maximum when V_{CE} = 0 & $I_C = \frac{V_{CC}}{R_C}$
- The Region along the load line including all points between Saturation and cutoff is generally known as linear region of Transistor operation.
- The Below figure shows the example of the linear operation of the Transistor. Assume a sinusoidal voltage V_{in} is superimposed on V_{BB}, causing the Base Current to vary sinusoidally 100.01A above & below its Q-point value 300mA. This in turn causes the I_C to vary 10mA above & below its Q-point value of 30mA. As a result of variation in I_C, V_{CE} varies 2.2V above & below its Q-point value of 3.4V. Point 'A' on load line corresponds to +ve peak of the sinusoidal i/p, point 'B' corresponds to -ve peak and 'Q' corresponds to the zero value of i/p.

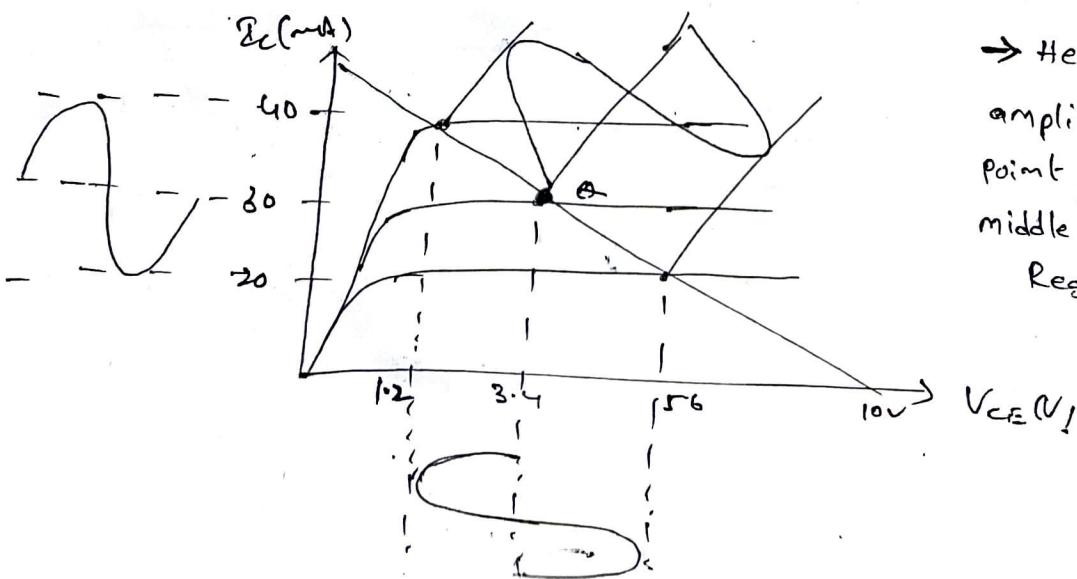


Case(i): If A is the operating point, then A will lie near the saturation region. Therefore the positive cycle of the input signal will be clipped off. Hence distortion will occur. Thus the point A is not the suitable operating point.



Case(ii): If B is considered as the operating point, then this point will lie near the cut-off region. Therefore, the negative cycle of input will be clipped off. Hence distortion will occur. So the point B is also not the suitable operating point.

Case(iii): If 'C' is chosen as the operating point, then this will lie in the active region. Also this point is in the middle of the active region. Therefore signal will not be clipped off. Hence there will be no distortion at all. Therefore, point C is the suitable operating point.



→ Hence, for faithful amplification, operating point must lie in the middle of the Active Region

Bias Stability :-

- Collector current in a transistor changes when
 - Temperature changes
 - Transistor is Replaced by another of same type. This is due to Variations in transistor parameters
- When above two situations occurred the operating point also changes. But for faithful amplification operating point must be remain fixed. So it is necessary to make operating point remain fixed. So that a point can be independent of these variations. This is known as Stabilization

"The process of making operating point independent of temperature changes or variation in transistor parameters is known as Stabilization".

- Once stabilization is done, zero signal values of I_C & V_{CE} become independent of parameter variation & temperature variation. So that operating point is fixed
- A Good Biasing circuit always needs stabilization of Q-point.

Need for Stabilization :-

① Instability due to β change & V_{BE} :

The value of β and V_{BE} are not ~~exactly~~ exactly same for any two transistors even of same type. ~~β vary widely between~~ Change in β will shift the operating point in any undesired region even though if we maintain I_C as constant. V_{BE} decreases when temperature increases. So that operating point will change and it needs to stabilize.

② Thermal Instability (Dependence of I_C on Temperature) :-

Another reason for instability in operating point is change in temperature. We know that in a transistor collector current I_C is given as

$$I_C = \beta I_B + (1 + \beta) I_{C0}$$

The reverse saturation current I_{C0} is temperature dependent. I_{C0} becomes double for every 10°C rise in temperature. The increase in the value of I_{C0} increases I_C . The increase in I_C will lead to change the operating point because more power loss in collector junction due to increasing the temperature at I_C . This i.e., increased temperature again increases I_{C0} . So fast Transistor damage.

So to stabilize operating point, it is required to hold I_C constant despite of temperature variations.

Stability factor :-

→ In biasing a transistor in active region, it is necessary to keep the operating point stable by keeping I_C & V_{CE} constant.

There are two techniques used for maintaining the Q-point as constant

(1) Stabilization Technique :- This technique refers to the use of resistive biasing circuits which allow I_B to vary so as to keep I_C relatively constant with variations in I_{C0} , β and V_{BE} .

(2) Compensation Technique :- This technique refers to the use of temperature sensitive devices such as diodes, transistors, thermistors, etc. Such devices provide compensating voltages and currents to maintain the operating point constant.

→ There are number of ~~techniques~~ stabilization & compensation circuits. In order to compare these biasing circuits a common factor called stability factor is used.

→ Since there are three variables I_{C0} , β & V_{BE} which are temperature dependent, we define three stability factors.

(1) Stability Factor S :- It is defined as the rate of change of collector current with respect to the reverse saturation current, keeping β and V_{BE} constant. i.e

$$S = \frac{dI_c}{dI_{C0}} \approx \left. \frac{\Delta I_c}{\Delta I_{C0}} \right| \beta, V_{BE} = \text{constant}$$

The larger the value of S , the circuit exhibit thermal instability.
The smaller is the value of S , higher the stability.

(2). Stability Factor S' (or) S_V :- This is defined as the rate of change of I_c with V_{BE} , keeping I_{C0} and β constant.

$$S' = \frac{dI_c}{dV_{BE}} \approx \left. \frac{\Delta I_c}{\Delta V_{BE}} \right| \beta, I_{C0} = \text{constant}$$

(3) Stability Factor S'' (or) S_β :- This is defined as rate of change of I_c with β , keeping I_{C0} and V_{BE} constant.

$$S'' = \frac{dI_c}{d\beta} \approx \left. \frac{\Delta I_c}{\Delta \beta} \right| I_{C0}, V_{BE} = \text{constant}$$

Expression for 'S' :-

$$I_c = \beta I_B + (1+\beta) I_{C0}$$

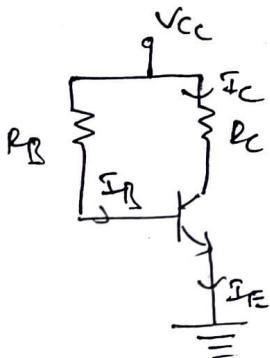
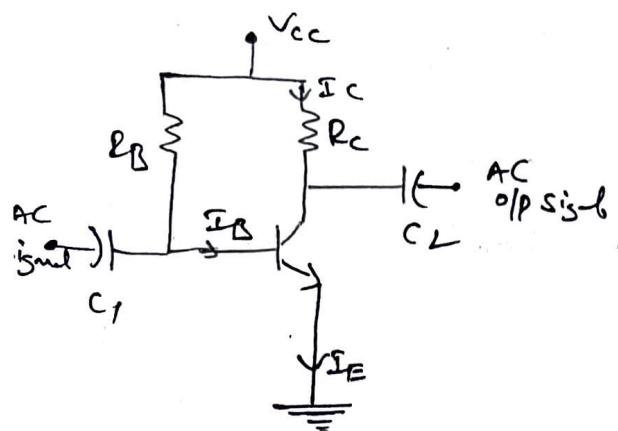
Differentiate the above equation wrt I_c we get, (β is constant)

$$\frac{dI_c}{dI_c} = \beta \frac{dI_B}{dI_c} + (1+\beta) \frac{dI_{C0}}{dI_c}$$

$$1 = \beta \frac{dI_B}{dI_c} + \frac{1+\beta}{1+\beta}$$

$$S = \frac{1}{1 - \beta \left(\frac{dI_B}{dI_c} \right)}$$

Fixed Bias: it is also called Base Bias method. The Fixed Bias circuit is shown below with capacitors. For DC analysis capacitors are replaced by OC because $X_C = \infty$. The DC Equivalent for Fixed Bias circuit is shown below.



Base circuit

Apply KVL for 'B' to E loop. Then

$$V_{CC} = I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$R_B = \frac{V_{CC}}{I_B} \quad (\because V_{BE} \ll V_{CC})$$

Collector circuit Apply KVL for collector circuit then

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$

and we know that $I_C = R_B I_B$

$$I_C = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right)$$

It is important to note that since the Base current is controlled by the value of R_B & I_C is related to I_B by a constant β . The magnitude of I_C is not a function of R_C . So this method is called Base Bias or fixed bias. Change in R_C to any level will not affect the I_B or I_C in active region.

7

stability factor S : Here V_{BE} & β are constants

$$S = \frac{1+\beta}{1-\beta \left(\frac{dI_B}{dI_C} \right)}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$\frac{dI_B}{dI_C} = 0$, because V_{CC} , V_{BE} & R_B are constants.

then $S = \frac{1+\beta}{1-\beta(0)}$

$$\boxed{S = 1+\beta} \checkmark$$

Stability factor S' Here I_{CO} & β are constants

$$S' = \frac{dI_C}{dV_{BE}} \quad \left| I_{CO} \text{ & } \beta \text{ are constants} \right.$$

Take $I_C = \beta I_B + (1+\beta) I_{CO}$

$$I_C = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right) + I_{CO}(1+\beta)$$

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + I_{CO}(1+\beta)$$

$$\frac{dI_C}{dV_{BE}} = 0 - \frac{\beta}{R_B} + 0$$

$(\beta, I_{CO}, V_{BE} \text{ are constants})$

$$\boxed{S' = -\frac{\beta}{R_B}} \checkmark$$

Stability Factor s''

$$s'' = \frac{d I_c}{d \beta} \quad | \quad I_{C_0} \text{ & } V_{BE} \text{ are constants}$$

$$I_c = \beta I_B + (1+\beta) I_{C_0}$$

$$I_c = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right) + (1+\beta) I_{C_0}$$

$$I_c = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{C_0} \Rightarrow I_c = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right) + I_{C_0}$$

$$\frac{d I_c}{d \beta} = \left(\frac{V_{CC}}{R_B} - \frac{V_{BE}}{R_B} \right) + I_{C_0}$$

$$s'' = I_B + I_{C_0}$$

$$\boxed{s'' = \frac{I_c}{\beta}} \quad (\because I_c = \beta I_B), \& (I_B \gg I_{C_0}).$$

or

By Applying KVL to input side

$$V_{CC} = V_{BE} + I_B R_B$$

$$V_{CC} = V_{BE} + R_B \left[\frac{I_c - (1+\beta) I_{C_0}}{\beta} \right]$$

Differentiate above eqn wrt I_c , where V_{BE} & I_{C_0} are constants

$$0 = 0 + R_B \left[\frac{\beta - I_c \left(\frac{d\beta}{d I_c} \right)}{\beta^2} \right]$$

$$\begin{cases} \beta \gg 1 \\ I_c \gg I_{C_0} \\ \therefore \beta I_{C_0} \text{ is negligible} \end{cases}$$

$$(\frac{u}{v} = \frac{u_1 - u_2}{v_1 - v_2})$$

$$0 = \frac{R_B}{\beta^2} \left[\beta - I_c \left(\frac{d\beta}{d I_c} \right) \right]$$

$$\beta = I_c \frac{d\beta}{d I_c} \Rightarrow \beta = I_c \cdot \frac{1}{s''} \Rightarrow \boxed{s'' = \frac{I_c}{\beta}} \checkmark$$

Collector-to-Base Bias (or) Voltage Feed Back Bias :-

→ The Biasing Resistor R_B is connected between Collector and Base of the Transistor.

→ Let the I_B flows through R_B and $I_C + I_B$ flows through the R_C .

→ If there is a change in β , or if there is any increase of ambient temperature, the collector current I_C tends to increase.

As a result, voltage drop $I_C R_C$ increases. Since supply voltage V_{CC} is constant, therefore V_{CE} decreases. This reduced collector-to-emitter voltage results in reduced I_B . Since now I_B is reduced, collector current I_C is reduced. Thus Q-point is stable.

→ Thus we find that the Collector-to-Base biasing helps to partly compensate the changes which occurred originally due to change in temperature or change in β .

→ The below given Analysis shows how Q-point is maintained constant.

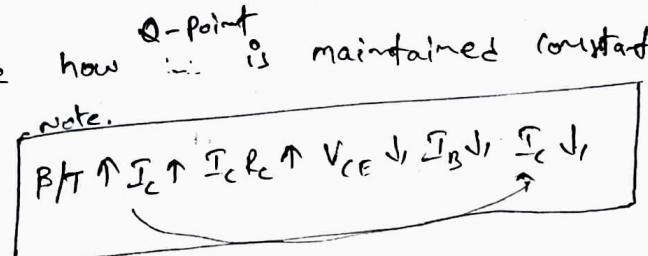
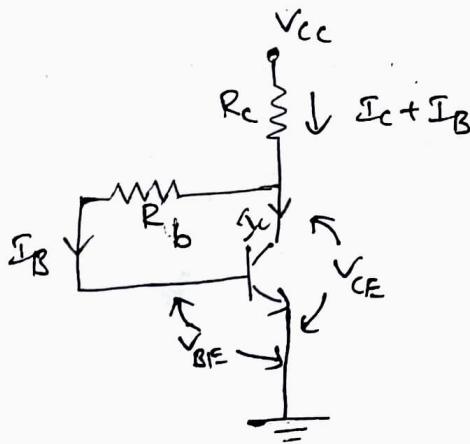
Apply KVL to Base circuit we get

$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C} \rightarrow (1)$$

$$\therefore \frac{I_C}{\beta} = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$$

$$I_C = \frac{\beta (V_{CC} - V_{BE} - I_C R_C)}{R_B + R_C} \rightarrow (2)$$



→ Equation (2) indicates that if β will change I_C will change.

Apply KVL to collector circuit we get

$$V_{CC} = (I_C + I_B) R_C + V_{CE}$$

$$V_{CC} - I_C R_C = I_B R_C + V_{CE} \rightarrow (3)$$

From Equation ① $V_{CC} - I_C R_C = I_B (R_C + R_B) + V_{BE} \rightarrow (4)$

now make (3)=(4)

$$V_{CE} + I_B R_C = I_B (R_C + R_B) + V_{BE}$$

$$V_{CE} + I_B R_C = I_B R_C + I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CE} - V_{BE}}{R_B} \rightarrow (5)$$

OR OR

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CE} - V_{BE} = V_{CB}$$

$$V_{CE} - V_{BE} = I_B R_B$$

$I_B = \frac{V_{CE} - V_{BE}}{R_B}$

This Eqn indicates that if V_{CE} is Reduced, so that I_B also Reduced. so that I_C is Reduced then Q-point is fixed.

Stability Factor S

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{dI_B}{dI_C} \right)}$$

From Equation ① $I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_b + R_C}$

$$\frac{dI_B}{dI_C} = - \frac{R_C}{R_b + R_C}$$

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_C}{R_b + R_C} \right)}$$

$\rightarrow (7)$

This value of S is smaller than $(1 + \beta)$ which was the stability factor S for Fixed-Bias Circuit. Thus for Collector-to-Base bias has smaller S, so that this circuit has ~~poor~~ good stability over Fixed Bias circuit.

Stabilization against change in β

The stability Factor S of this circuit is highly dependent on β ,

$$\text{i.e. } S = \frac{1+\beta}{1+\beta\left(\frac{R_c}{R_b+R_c}\right)}$$

→ if we design the circuit with condition $\beta R_c \gg R_b$, then we make S independent of β . This can be proved as follows.

we know that $I_c = (1+\beta) I_{C0} + \beta I_B$

$$I_B = \frac{I_c - (1+\beta) I_{C0}}{\beta}$$

By applying KVL for bias circuit we get

$$V_{CC} = R_c (I_B + I_c) + I_B R_b + V_{BE}$$

$$V_{CC} = I_B R_c + I_c R_c + I_B R_b + V_{BE}$$

$$V_{CC} = I_B (R_c + R_b) + I_c R_c + V_{BE}$$

$$V_{CC} = \left(\frac{I_c - (1+\beta) I_{C0}}{\beta} \right) (R_c + R_b) + I_c R_c + V_{BE}$$

Multiply on both sides by β

$$\beta V_{CC} = (I_c - (1+\beta) I_{C0}) (R_c + R_b) + \beta I_c R_c + \beta V_{BE}$$

$$\beta V_{CC} - \beta V_{BE} = I_c (R_c + R_b) - \beta I_{C0} (R_c + R_b) + \beta I_c R_c$$

$$\beta V_{CC} - \beta V_{BE} + \beta I_{C0} (R_c + R_b) = I_c R_c + I_c R_b + \beta I_c R_c$$

assume $\beta R_c \gg R_c$ so that $\beta R_c + R_c \approx \beta R_c$

$$I_c = \frac{\beta [V_{CC} - V_{BE} + I_{C0} (R_c + R_b)]}{\beta R_c + R_b}$$

make $\beta R_c \gg R_b$ then

$\because \beta \gg 1$
 $\therefore 1+\beta \approx \beta$

$$I_C = \frac{V_{CC} - V_{BE} + I_{CO}(R_C + R_B)}{R_C}$$

$\therefore I_C$ has become independent of β & hence stabilized against changes in β .

Stability Factors:-

$$S' = \left| \frac{dI_C}{dV_{BE}} \right| \quad | I_{CO} \text{ & } \beta \text{ are constants}$$

From Base Circuit,

$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_B(R_B + R_C) + I_C R_C + V_{BE}$$

$$V_{CC} = \left[\frac{I_C - (1+\beta)I_{CO}}{\beta} \right] (R_B + R_C) + I_C R_C + V_{BE}$$

$$\therefore I_C = \beta I_B + (1+\beta)I_{CO}$$

$$\therefore I_B = \frac{I_C - (1+\beta)I_{CO}}{\beta}$$

assume $\beta \gg 1$ & $I_C \gg I_{CO}$, neglecting $(1+\beta)I_{CO}$

$$V_{CC} = \frac{I_C}{\beta} (R_B + R_C) + I_C R_C + V_{BE}$$

Differentiate above Eqn wrt to I_C

$$\frac{1}{S'} = -R_C \frac{(\beta+1)}{\beta} - \frac{R_B}{\beta}$$

$$\frac{1}{S'} = -\frac{1}{\beta} [R_C(1+\beta) + R_B]$$

$$S' = \frac{-\beta}{[R_C(1+\beta) + R_B]}$$

$$S_0 = R_C + \frac{R_C}{\beta} + \frac{R_B}{\beta} + \frac{1}{S'}$$

$$S' = \frac{-\beta}{R_C(1+\beta) + R_B}$$

$$S_0 = R_C \left[1 + \frac{1}{\beta} \right] + \frac{R_B}{\beta} + \frac{1}{S'}$$

S''

Applying KVL to Base circuit we get ✓

$$V_{CC} = R_C (I_C + I_E) + I_B R_B + V_{BE}$$

$$V_{CC} = R_C I_C + I_B (R_C + R_B) + V_{BE}$$

$$V_{CC} = R_C I_C + V_{BE} + (R_C + R_B) \left(\frac{I_C - (1+\beta) I_{C0}}{\beta} \right)$$

Assume $1+\beta \approx \beta$, neglect I_{C0} .

$$V_{CC} = R_C I_C + V_{BE} + (R_C + R_B) \left(\frac{I_C}{\beta} \right)$$

Differentiate wrt I_C taking I_{C0} & V_{BE} constants.

$$0 = R_C + 0 + (R_C + R_B) \left[\frac{\beta(1) - I_C \left(\frac{\partial \beta}{\partial I_C} \right)}{\beta^2} \right]$$

$$0 = R_C + \left(\frac{R_C + R_B}{\beta^2} \right) \left[\beta - I_C \left(\frac{1}{S''} \right) \right]$$

$$0 = R_C + \left[\frac{R_C + R_B}{\beta} - \frac{I_C (R_C + R_B)}{S'' \beta^2} \right]$$

$$\frac{I_C (R_C + R_B)}{S'' \beta^2} = R_C + \frac{R_C + R_B}{\beta}$$

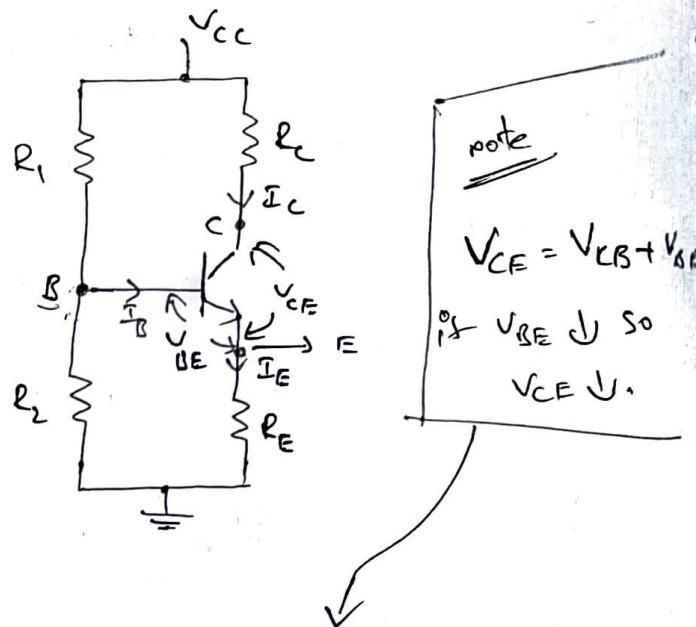
$$\frac{I_C (R_C + R_B)}{S'' \beta^2} = \frac{\beta R_C + R_C + R_B}{\beta}$$

$$S'' = \frac{I_C (R_C + R_B)}{\beta [R_C (1+\beta) + R_B]}$$

$$\frac{e_1}{v} = \frac{V_{U1} - V_U}{V^2}$$

4) Voltage Divider Bias (or) Self-Bias (or) Emitter Bias:

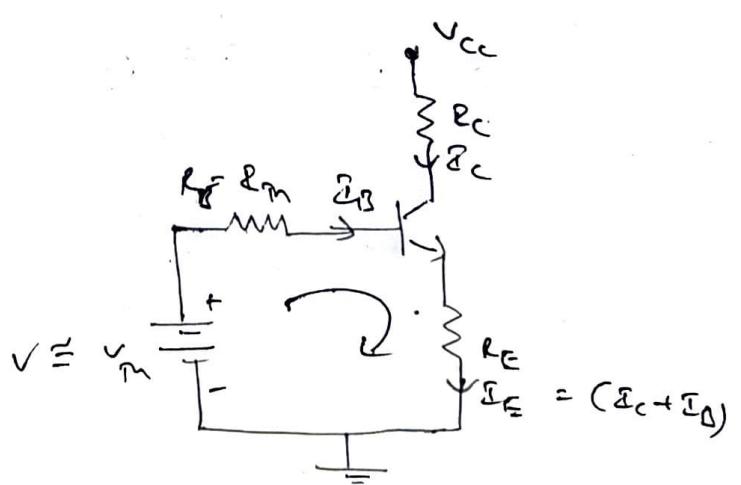
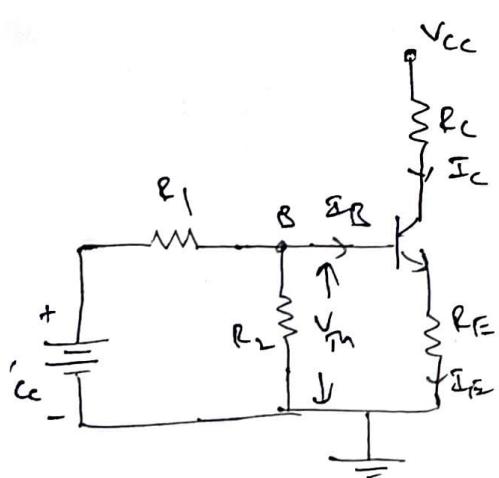
- The Biasing is provided by three Resistors R_1 , R_2 & R_E .
- The Resistors R_1 and R_2 acts as a potential divider giving a fixed voltage to point B (i.e. at Base).
- If I_C tends to increase, then I_E also increases and voltage drop across R_E increases.
- As a result voltage difference (i.e. $V_B - V_E$) between Base & Emitter will reduce and hence I_B will reduce. In turn I_C will reduce, trying to partly compensate for the original change.



$$I_C \uparrow I_E \uparrow I_E R_E \uparrow V_{BE} \downarrow I_B \downarrow, I_C \downarrow$$

Stability Factor S

- For determining this above circuit should be modified as follows. The above circuit is redrawn as shown below and then replace the voltage divider network R_1 & R_2 by its Thevenin equivalent circuit.



$$V = V_m = \frac{R_2 V_{CC}}{R_1 + R_2}, R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

Applying KVL around the Base circuit loop

$$V = I_B R_B + V_{BE} + I_E R_E$$

$$V = I_B R_B + V_{BE} + (I_B + I_C) R_E$$

Differentiating wrt I_C and consider V_{BE} to be independent of I_C , we get

$$0 = \frac{\partial I_B}{\partial I_C} R_B + 0 + \frac{\partial I_B}{\partial I_C} R_E + R_E$$

$$0 = \frac{\partial I_B}{\partial I_C} (R_B + R_E) + R_E$$

$$\boxed{\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_B + R_E}}$$

$$S = \frac{1 + \beta}{1 - \beta \left(\frac{\partial I_B}{\partial I_C} \right)} \Rightarrow S = \frac{1 + \beta}{1 + \beta \left(\frac{R_E}{R_B + R_E} \right)}$$

$$\boxed{S = \frac{(1 + \beta)(R_B + R_E)}{R_B + R_E + \beta R_E}}$$

$$S = \frac{(1 + \beta) R_E \left(1 + \frac{R_B}{R_E} \right)}{R_E \left(1 + \frac{R_B}{R_E} + \beta \right)}$$

Dividing R_B & R_E we get

$$\boxed{S = \frac{(1 + \beta) \left(1 + \frac{R_B}{R_E} \right)}{1 + \beta + \frac{R_B}{R_E}}}$$

From above Equation we conclude that

① If $\frac{R_B}{R_E} \ll 1$, then $S = \frac{1+\beta}{1+\alpha} = 1$.

Practically $\frac{R_B}{R_E} \neq 0$. But to have better S, the Ratio $\frac{R_B}{R_E}$ as small as possible.

② To keep $\frac{R_B}{R_E}$ small, it is necessary to keep R_B small. This means $R_1 || R_2$ must be small. But if R_B is reduced, input impedance of Ckt also Reduced. This is not desirable condition. so that R_B can't be made very small.

③ By increasing R_E , we can reduce $\frac{R_B}{R_E}$. But it will cause drop I_{E/R_E} will also increase & since V_{CC} is fixed, this shifts the Q-point which is not desirable & hence there is a limit for increasing R_E .

Thus while designing Self-Bias Circuit we have to find compromising values

" $S \rightarrow$ small," $R_B \rightarrow$ Reasonably small, $R_E \rightarrow$ not very large.

④ If Ratio $\frac{R_B}{R_E}$ is fixed, S increases with β . Therefore stability decreases with increasing β .

⑤ S is essentially independent of β for small values of S.

S for self-Bias circuit is less compared to other Biasing circuit so this circuit is most commonly used circuit.

Stability Factor S' : $S' = \frac{dI_C}{dV_{BE}}$ | I_{C0}, β are constants.

applying KVL around Base loop

$$V = I_B R_B + V_{BE} + (I_C + I_B) R_E$$

$$(I_E = I_B + I_C)$$

$$V_{BE} = V - I_B (R_B + R_E) - I_C R_E$$

$$V_{BE} = V - \left[\frac{I_C - (1+\beta) I_{C0}}{\beta} \right] (R_B + R_E) - I_C R_E$$

$$V_{BE} = V - \left[\frac{(R_E + R_B) I_C - (R_E + R_B)(1+\beta) I_{C0}}{\beta} \right] - I_C R_E$$

$$V_{BE} = V - \left[\frac{(R_E + R_B) I_C + I_C R_E \beta}{\beta} \right] + \frac{(R_E + R_B)(1+\beta) I_{C0}}{\beta}$$

or

Differentiating wrt V_{BE} with I_{C0} & β as constants

$$0 = 0 - \frac{(R_B + (1+\beta) R_E)}{\beta} \frac{\partial I_C}{\partial V_{BE}} + 0$$

$$s' = -\frac{\beta}{R_B + (1+\beta) R_E}$$

$$\begin{aligned} v &= I_B (R_C + R_E) + V_{BE} + I_C R_E \\ \text{diff wrt } I_C \\ v &= \frac{I_C}{\beta} (R_C + R_E) + V_{BE} + I_C R_E \end{aligned}$$

$$\begin{aligned} 0 &= \frac{R_C + R_E}{\beta} + \frac{dV_{BE}}{dI_C} + R_E \\ -\frac{(R_C + R_E)}{\beta} - R_E &= \frac{1}{s'} \\ \frac{1}{s'} &= -\left[\frac{R_C + R_E + R_E}{\beta} \right] \Rightarrow s' = -\frac{\beta}{R_C + (1+\beta) R_E} \end{aligned}$$

Stability Factor s'' : $s'' = \frac{\partial I_C}{\partial \beta} \quad | \quad I_{C0}, V_{BE} \text{ constants}$

We know that from above analysis,

$$V_{BE} = V - \frac{(R_B + (1+\beta) R_E) I_C}{\beta} + \frac{(R_E + R_B)(1+\beta) I_{C0}}{\beta}$$

$$V_{BE} = V - \frac{(R_B + (1+\beta) R_E) I_C}{\beta} + V'$$

$$V' = \frac{(R_E + R_B)(1+\beta)}{\beta} I_{C0} \quad (\because)$$

$$V' = (R_E + R_B) I_{C0} \quad (\because \beta \gg 1)$$

$$I_c = \frac{\beta(V + v' - V_{BE})}{R_B + R_E(1+\beta)}$$

Differentiating wrt β & taking v' independent of β

$$\frac{dI_c}{d\beta} = \frac{[R_B + R_E(1+\beta)][V + v' - V_{BE}] - \beta(V + v' - V_{BE}) \cdot R_E}{[R_B + R_E(1+\beta)]^2}$$

$$\frac{u}{v} = \frac{V + v' - V_{BE}}{V}$$

multiplying Nr & Dr by $(1+\beta)$, we get

$$s'' = \frac{[(R_B + R_E(1+\beta)) - \beta R_E](V + v' - V_{BE})(1+\beta)}{(1+\beta)[R_B + R_E(1+\beta)]^2}$$

$$s'' = \frac{(R_B + R_E + \cancel{\beta R_E} - \cancel{\beta R_E})(V + v' - V_{BE})(1+\beta)}{(1+\beta)[R_B + R_E(1+\beta)][R_B + R_E(1+\beta)]}$$

$$s'' = \frac{(1+\beta)(R_B + R_E)(V + v' - V_{BE})}{(1+\beta)[R_B + R_E(1+\beta)][R_B + R_E(1+\beta)]}$$

$$s'' = \frac{s(V + v' - V_{BE})}{(1+\beta)[R_B + R_E(1+\beta)]}$$

$$\therefore s = \frac{(1+\beta)(R_E + R_B)}{R_B + R_E(1+\beta)}$$

multiplying Nr & Dr by β we get

$$s'' = \frac{s\beta(V + v' - V_{BE})}{\beta(1+\beta)[R_B + R_E(1+\beta)]}$$

$$s'' = \frac{I_c s}{\beta(1+\beta)} \rightarrow ①$$

$$\therefore I_c = \frac{R(V + v' - V_{BE})}{R_B + R_E(1+\beta)}$$

A difficulty arises in the use of s'' which is not present with s and s' .

The change in collector current due to a change in β is

$$s'' = \frac{\Delta I_C}{\Delta \beta}$$

$$\Delta I_C = s'' \Delta \beta$$

$$\Delta I_C = \frac{I_C s}{R(1+\beta)} \Delta \beta$$

where $\Delta \beta = \beta_2 - \beta_1$ may represent a large change in β . Hence it is not clear whether to use β_1 , β_2 or average value of β for s'' & s .

This difficulty is avoided if s'' is obtained by taking finite differences rather than by evaluating a derivative. Thus

$$s'' = \frac{I_{C2} - I_{C1}}{\beta_2 - \beta_1} = \frac{\Delta I_C}{\Delta \beta}$$

$$I_C = \frac{\beta(V + V' - V_{BE})}{R_B + R_E(1+\beta)}$$

$$\frac{I_{C2}}{I_{C1}} = \frac{\beta_2}{\beta_1} \frac{R_B + R_E(1+\beta_1)}{R_B + R_E(1+\beta_2)}$$

Subtracting unity from both sides yields

$$\frac{I_{C2}}{I_{C1}} - 1 = \left(\left(\frac{\beta_2}{\beta_1} \right) \frac{R_B + R_E(1+\beta_1)}{R_B + R_E(1+\beta_2)} \right) - 1$$

$$\frac{\Delta I_{C_2} - I_{C_1}}{I_{C_1}} = \frac{\beta_2 [R_B + R_E(1+\beta_1)] - \beta_1 [R_B + R_E(1+\beta_2)]}{\beta_1 [R_B + R_E(1+\beta_2)]}$$

$$\frac{\Delta I_C}{I_{C_1}} = \frac{\beta_2 R_B + \beta_2 R_E + \beta_1 \cancel{\beta_2} R_E - \beta_1 R_B - \beta_1 R_E - \cancel{\beta_1 \beta_2} R_E}{\beta_1 [R_B + R_E(1+\beta_2)]}$$

$$\frac{\delta I_C}{I_{C_1}} = \frac{\beta_2 (R_B + R_E) - \beta_1 (R_B + R_E)}{\beta_1 [R_B + R_E(1+\beta_2)]}$$

$$\frac{\delta I_C}{I_{C_1}} = \left[\frac{\beta_2 - \beta_1}{\beta_1} \right] \frac{R_B + R_E}{R_B + R_E(1+\beta_2)}$$

$$\frac{\delta I_C}{I_{C_1}} = \frac{\delta \beta}{\beta_1} \frac{R_B + R_E}{R_B + R_E(1+\beta_2)}$$

when $\beta = \beta_2$
since $s_2 = s = \frac{(1+\beta)(R_B + R_E)}{R_B + R_E(1+\beta_2)}$

$$\frac{\delta I_C}{\delta \beta} = \frac{I_{C_1}}{\beta_1} \frac{R_B + R_E}{R_B + R_E(1+\beta_2)}$$

Multiplying Nr & Dr with $(1+\beta)$ we get

$$\frac{\delta I_C}{\delta \beta} = \frac{I_{C_1}}{\beta_1} \cdot \frac{(1+\beta)(R_B + R_E)}{(1+\beta)(R_B + R_E(1+\beta_2))}$$

$$\frac{\delta I_C}{\delta \beta} = \frac{I_{C_1}}{\beta_1} \cdot \frac{s_2}{(1+\beta_2)}$$

$$s'' = \frac{I_{C_1} s_2}{\beta_1 (1+\beta_2)} \rightarrow ②$$

As $\delta \beta = \beta_2 - \beta_1 \rightarrow 0$, equation ②

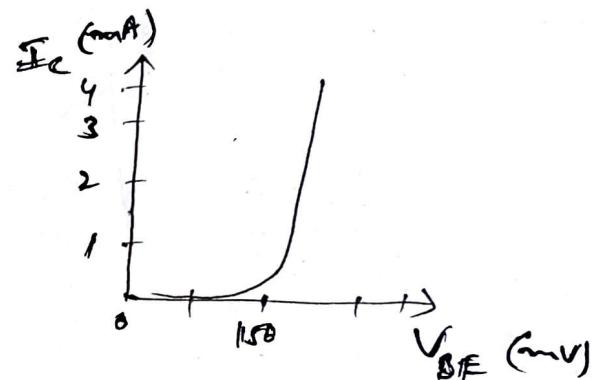
becomes Eq ①.

Stabilization Against Variations in V_{BE} & β for Self Bias Circuit :-

- we shall neglect the effect of the change of V_{CE} with temperature because this variation is small and because we assume that the Transistor operates in the active Region, where I_C approximately independent of V_{CE} .
- The Variation of V_{BE} with temperature has a very important effect on bias stability.
- For a Silicon Transistor, $V_{BE} = 0.6V$ & for Ge, $V_{BE} = 0.2V$ at roomtemperature. As the Temperature increases, $|V_{BE}|$ decreased at the rate of $2.5 \text{ mV}/^\circ\text{C}$ for both Ge & Si transistors.

The Transfer characteristics :-

- The output Current I_C is plotted as a function of V_{BE} for typical Ge Transistor.
- Each curve shifts to the left at the rate of $2.5 \text{ mV}/^\circ\text{C}$ for increasing temperature.



- we now examine the effect of shift in transfer characteristics and variation of β and I_{Co} with temperature.

we already obtained Expression for V_{BE} by applying KVL around Base loop for self Bias circuit i.e given as

$$V_{BE} = V + \frac{(R_B + R_E)(1+\beta)}{\beta} I_{Co} - \frac{[R_B + R_E(1+\beta)]}{\beta} I_C$$

$$V_{BE} = V - \frac{[R_B + R_E(1+\beta)]I_C}{R} + V^1$$

$$\text{where } V^1 = \frac{(R_B + R_E)(1+\beta)I_{Co}}{R} \approx (R_B + R_E)I_{Co} (\because \beta \gg 1)$$

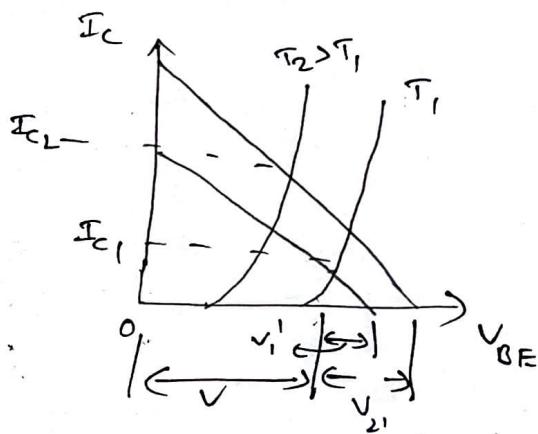
\rightarrow If $T = T_1 (\tau_2)$, $I_c = I_{c01} (I_{c02})$ and $\beta = \beta_1 (\beta_2)$, then

$V_1' = (R_B + R_E) I_{c01}$ & $V_2' = (R_B + R_E) I_{c02}$. Hence the intercept of the load line on the V_{BE} axis is a function of temperature because I_{c0} increases with T . The slope of the load line is

$$\sigma = -\frac{\beta}{R_B + R_E(1+\beta)} \quad \text{and hence it increased with } T$$

because β increases with T .

\rightarrow The transfer characteristics for $T = T_2 > T_1$, shifts to the left of the corresponding curve for $T = T_1$ because V_{BE} varies with T .



$$\rightarrow \text{The stability factor } s^1 = \frac{-\beta}{R_B + R_E(1+\beta)} = -\frac{s}{R_B + R_E} \cdot \frac{\beta}{\beta+1}$$

as we reduce s towards unity, we minimize the change of I_c with respect to both V_{BE} & I_{c0} .

$$\rightarrow s'' = \frac{I_c s}{\beta(1+\beta)}$$

as s is reduced, s'' is also ~~reduced~~ reduced so stabilization is done.

Bias Compensation:

Biasing circuits discussed so far provide stability of operating point in case of variations in Transistor parameters such as I_{CO} , V_{BE} and β . In applications where extremely stable biasing conditions are required then it is necessary to use compensation techniques. Compensation techniques use Temperature sensitive devices such as diodes, transistors, thermistors and semistors to maintain operating point constant.

Diode Compensation for V_{BE} :

→ A circuit utilizing the self bias stabilization technique and diode compensation is shown here

→ V_{DD} is used to keep diode in forward Bias Condition

→ If the diode is of the same material and type as the transistor, the Voltage V_D across the diode will have the same temperature coefficient ($-2.5 \text{ mV}/\text{C}$) as the V_{BE} .

We know that

$$V_{BE} = V - \frac{R_B + (1+\beta) R_E}{\beta} I_C + \frac{(R_E + R_B)(1+\beta)}{\beta} I_{CO}$$

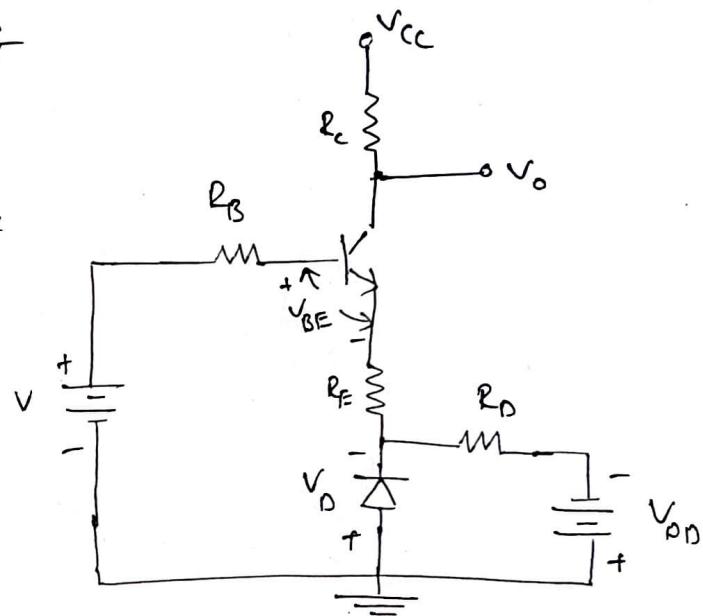
$$\therefore I_C = \frac{\beta(V - V_{BE}) + (R_E + R_B)(1+\beta) I_{CO}}{R_B + R_E(1+\beta)}$$

or $I_C = \frac{\beta(V - V_{BE} + V')}{R_B + R_E(1+\beta)}$

→ By writing KVL to the I/p circuit we get I_C as

$$I_C = \frac{\beta(V - (V_{BE} - V_0)) + (R_E + R_B)(1+\beta) I_{CO}}{R_B + (1+\beta) R_E}$$

Since V_{BE} tracks V_D wrt Temperature, it is clear from above Eq., I_C will be insensitive to variations in V_{BE} .



Diode Compensation for I_{C0} :

→ For Germanium Transistors, changes in I_{C0} with Temperature play an important role in collector current stability.

→ The Diode compensation circuit shown here offers stabilization against variations in I_{C0} , and therefore useful for stabilizing Ge Transistors.

→ If the diode and Transistor are of the same type and material, the reverse saturation current I_0 of the diode will increase with Temperature at the same rate as Transistor I_{C0} . From above figure we have

$$V_{CC} = IR_1 + V_{BE}$$

$$I = \frac{V_{CC} - V_{BE}}{R_1} \approx \frac{V_{CC}}{R_1} = \text{constant.}$$

since the diode is Reverse biased by an amount $V_{BE} \approx 0.2 \text{ V}$, for Ge devices, it follows that the current through Di is I_0 .

→ The Base current $I_B = I - I_0$.

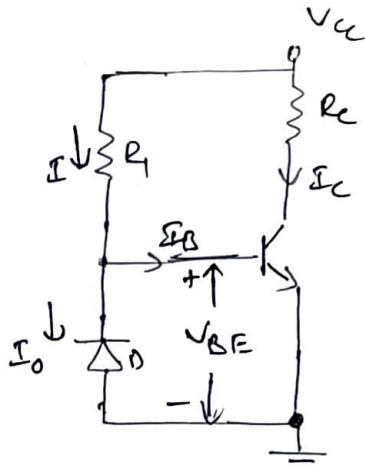
$$\text{we know that } I_c = \beta I_B + (1+\beta) I_{C0}$$

$$I_c = \beta(I - I_0) + (1+\beta) I_{C0}$$

$$I_c = \beta I - \beta I_0 + (1+\beta) I_{C0}$$

$$I_c = \beta I - \beta I_0 + \beta I_{C0} \quad (\because I \ll \beta)$$

From above Equation, but if $\beta \gg 1$, and if I_0 of D & I_{C0} of T track each other over desired temperature range, then I_c remains essentially constant.

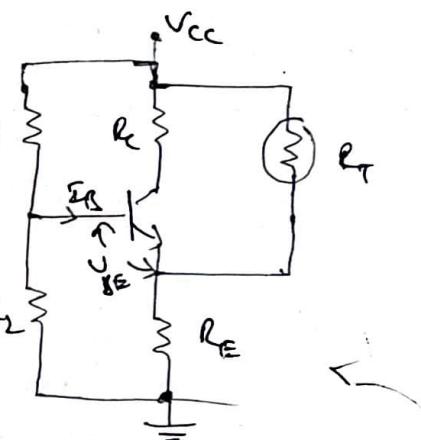


Thermistor Compensation:

- There is a method of Transistor compensation which involves the use of the Temperature-sensitive Resistive elements rather than diodes or Transistors.
- The Thermistor has a -ve Temperature Coefficient, its Resistance decreasing exponentially with increasing T .
- Consider the circuit which uses Thermistor R_T b/w V_{CC} & Emitter to minimize the increase in collector current due to changes in I_{CO} , V_{BE} or β with T . As T rises, R_T decreases, ~~and~~ and current fed through R_T into R_E increases. This increases the voltage drop across R_E (i.e. V_E).
- This increase in V_E Reduces the V_{BE} (i.e. $V_{SE} = V_B - V_E$), which reduces the I_B .

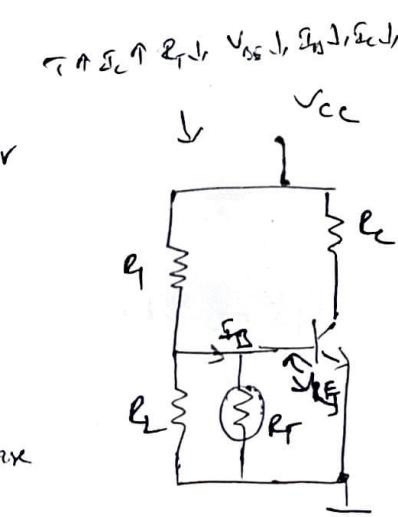
I_C is given by

$$I_C = \beta I_B + (1+\beta) I_{CO}. \text{ As } I_{CO} \text{ increases with } T, I_B \text{ decreases and hence } I_C \text{ remain constant.}$$



- An alternative configuration using Thermistor Compensation is to move R_T from its position in above figure and place it across R_2 .

- As T increases, drop across R_T decreases so V_{BE} Reduces. Hence I_B Reduced. This Behavior will tend to offset the increase in I_C with Temperature.

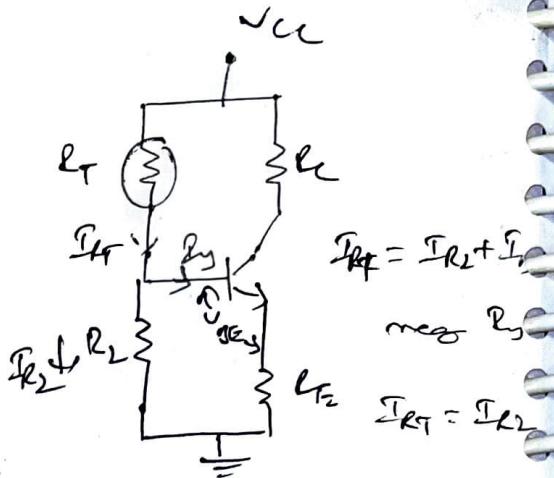


$$T \uparrow I_C \uparrow R_T \downarrow I_{RT} \uparrow \frac{I_{ER}}{V_E} \uparrow V_{BE} \downarrow I_B \downarrow I_C \downarrow$$

Sensistor Compensation:

- Instead of a Thermistor, it is possible to use a Temperature Sensitive Resistor with the Temperature Co-efficient such as a metal or the sensistor.
- The sensistor has a Temperature Co-efficient of Resistance which is +0.7 percent/ $^{\circ}\text{C}$.
- As the T rises, R_T increases which decreases the Current flowing through it. Hence current through R_2 decreases which Reduces the voltage drop across it. So V_{BE} is Reduced which Reduces I_B , hence when I_C increases I_B Reduces so that I_C is ~~fixed~~.

$$\boxed{I \propto I_C \uparrow R_T \uparrow I_C \downarrow R_2 \downarrow V_{BE} \downarrow I_B \downarrow I_C \downarrow}$$



Thermal Runaway:

- The maximum average power $P_D(\text{max})$ which a Transistor can dissipate depends upon the transistor construction and may lie in the range from a few milliwatts to 200W.
- This maximum power is limited by the temperature that the Collector-to-Base Junction can withstand.
- For Si Transistors this temperature is in the range 150 to 225 $^{\circ}\text{C}$ and for Ge it is between 60 and 100 $^{\circ}\text{C}$.
- The collector junction temperature may rise due to
 - (1) Rise in ambient temperature
 - (2) Self heating
- Self heating: The increase in the collector current increases the power dissipation at the collector junction, this in turn further increases

The Temperature at the Junction and hence increases the I_{CQ} , so that I_C increases. This process is cumulative and is referred to as "self heating". This excess heat produced at the Collector Base Junction may even burn and destroy the transistor. This situation is called "Thermal Runaway" of the Transistor.

Thermal Resistance :-

→ The steady-state temperature rise at T_C is proportional to the power dissipated at the Junction is given as

$$(T_J - T_A) \propto P_D$$

$$\textcircled{1} \leftarrow T_J - T_A = \theta P_D \Rightarrow \theta = \frac{T_J - T_A}{P_D} {}^{\circ}\text{C/W}$$

θ , → The constant of proportionality is called the "Thermal Resistance". Its value depends on the size of the Transistor, radiation to the surrounding and on the heat sink.

→ Typical Values for ~~various~~ Transistor

(1) High power Transistor is $0.2 {}^{\circ}\text{C/W}$

(2) Low power Transistor is $1000 {}^{\circ}\text{C/W}$

T_J - Junction Temperature in ${}^{\circ}\text{C}$

T_A - Ambient Temperature in ${}^{\circ}\text{C}$

P_D - Power dissipated in watts at T_C .

Condition for Thermal Stability :-

To avoid Thermal Runaway the required condition is that the rate at which heat is released at the collector Junction must not exceed the rate at which the heat can be dissipated.

mathematically it is given as

$$\frac{dP_c}{dT_j} < \frac{dP_D}{dT_j} \rightarrow (2)$$

→ if we differentiate Eq (1) with respect to T_j , we get

$$T_j - T_A = \theta P_D$$

$$1 = \theta \frac{dP_D}{dT_j}$$

$$\frac{dP_D}{dT_j} = \frac{1}{\theta} \rightarrow (3)$$

Substituting in Eq (2) we get

$$\frac{dP_c}{dT_j} < \frac{1}{\theta} \rightarrow (4)$$

This condition must be satisfied to prevent thermal Runaway, in a Transistor

→ By suitable circuit design it is possible to ensure that the Transistor can't runaway below a specified ambient Temperature.

Thermal stability of an amplifier

Let us consider voltage divider Bias Circuit in the active region.

The Power Generated at the T_c is given by no sign is

~~$P_c = DC power in the circuit$~~

$$P_c = I_c V_{CB} \approx I_c V_{CE}$$

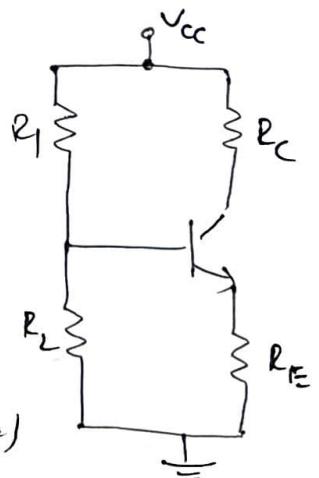
Apply KVL at O/P/Ckt then $V_{CE} = I_c R_C + V_{CE} + I_E R_E$

$$V_{CE} = I_c (R_C + R_E) + V_{CE} \quad : (I_c \approx I_E)$$

$$\therefore P_c = V_{CC} I_c - I_c^2 (R_C + R_E) \rightarrow (1)$$

$$V_{CE} = V_{CC} - I_c (R_C + R_E)$$

$$P_c = V_{CC} I_c - I_c^2 (R_C + R_E) \rightarrow (2)$$



→ let us consider $\frac{dP_c}{dT_j} < \frac{1}{\theta}$. This can be rewritten as follows:

$$\frac{dP_c}{dI_c} \cdot \frac{dI_c}{dT_j} < \frac{1}{\theta} \rightarrow ③$$

→ The First partial derivative of Eq ③ can be obtained from Eq ②:

$$\frac{dP_c}{dI_c} = V_{CC} - 2I_c(R_E + R_C) \rightarrow ④$$

→ The second partial derivative in Eq ③ gives ~~not~~ the rate at which collector current increases with temperature. We know that the Junction temperature affects I_c by affecting I_{C0} , V_{BE} & β .

Hence we write $\frac{dI_c}{dT_j}$ as

$$\frac{dI_c}{dT_j} = S \frac{dI_{C0}}{dT_j} + S' \frac{dV_{BE}}{dT_j} + S'' \frac{d\beta}{dT_j} \rightarrow ⑤$$

→ In some practical problems the effect of I_{C0} dominates, and above Eq ⑤ modified as

$$\frac{dI_c}{dT_j} = S \frac{dI_{C0}}{dT_j} \rightarrow ⑥$$

→ From Eq ③ & Eq ⑥

~~$\frac{dP_c}{dI_c}$~~ $\left(S \frac{dI_{C0}}{dT_j} \right) < \frac{1}{\theta} \rightarrow ⑦$

→ Generally the Reverse saturation current for either Si or Ge increases about 7%/ $^{\circ}\text{C}$

$$\frac{dI_{C0}}{dT_j} = 0.07 I_{C0} \rightarrow ⑧$$

⇒ now substitute Eq(4) & Eq(8) in Eq(7), we get

$$\left[V_{CC} - 2 I_C (R_C + R_E) \right] S (0.07 I_{CO}) < \frac{1}{\theta} \rightarrow (9)$$

Eq(9) is valid for pnp Transistor also.

As the θ , S , and I_{CO} are positive, the above inequality is always satisfied provided that the quantity in the Square Brackets is -ve or provided that

$$V_{CC} < 2 I_C (R_C + R_E)$$



$$\frac{V_{CC}}{2} < I_C (R_E + R_C) \rightarrow (10)$$

⇒ By applying KVL to op loop

$$V_{CC} = I_C R_C + I_E R_E + V_{CE}$$

$$I_C \approx I_E$$

$$V_{CC} = I_C (R_C + R_E) + V_{CE}$$

$$V_{CE} = V_{CC} - I_C (R_E + R_C)$$

$$V_{CC} - V_{CE} = I_C (R_E + R_C) \rightarrow (11)$$

$$Eq(10) = Eq(11)$$

$$\frac{V_{CC}}{2} < V_{CC} - V_{CE}$$

$$V_{CE} < V_{CC} - \frac{V_{CC}}{2}$$

$$V_{CE} < \frac{V_{CC}}{2} \rightarrow \text{This means stability is ensured.}$$