Main: PC, Instruction Memory, Clk, states, Muxes —> Roberts

Decoder: in: instruction (32b)
out(1b): isLoad
isStore
isIType
ALUOp
WrtEnable
isJType
isBranch
—> Anusha

RF: in: 3 registers, WrtEnable
out: 2 values(data), isEq —> kevin

ALU: in: Data1(32 b), Data2(32 b), ALUOp (3bits)
out: 1 value (data of 32 bits) —> Dmitriy

DM: in: address(32b), WriteData (32b), isLoad, isStore
out: ReadData(32b) —> Siddhartha

Assembly to machine code —> Karl

Write VHDL entities for these blocks and test them! Check the slides “Lecture 4” for help. Roberts will take care of the MUXs, don’t include them in the entities. For example, the MUX before the ALU should not be coded by Dmitriy