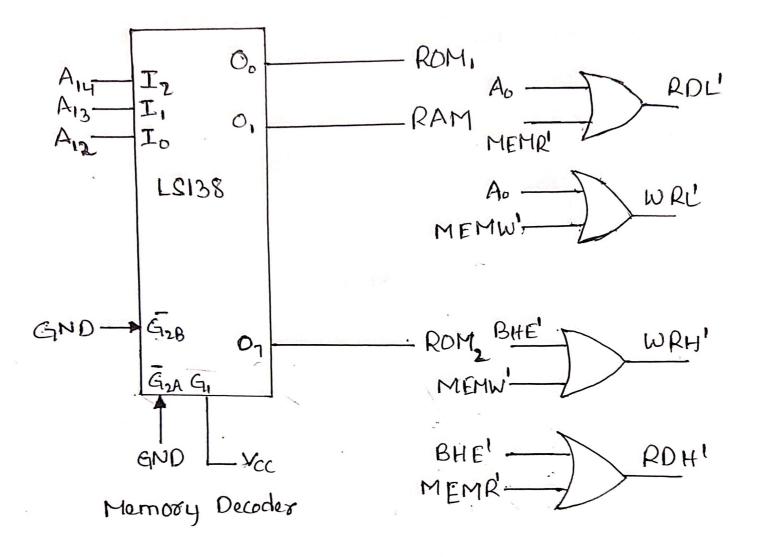
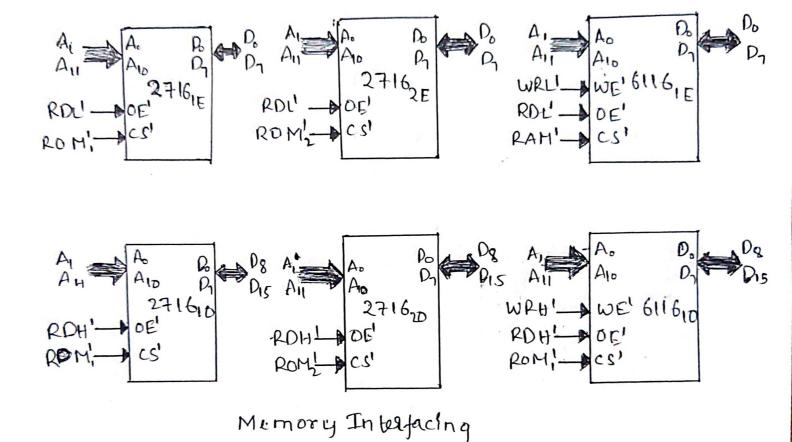
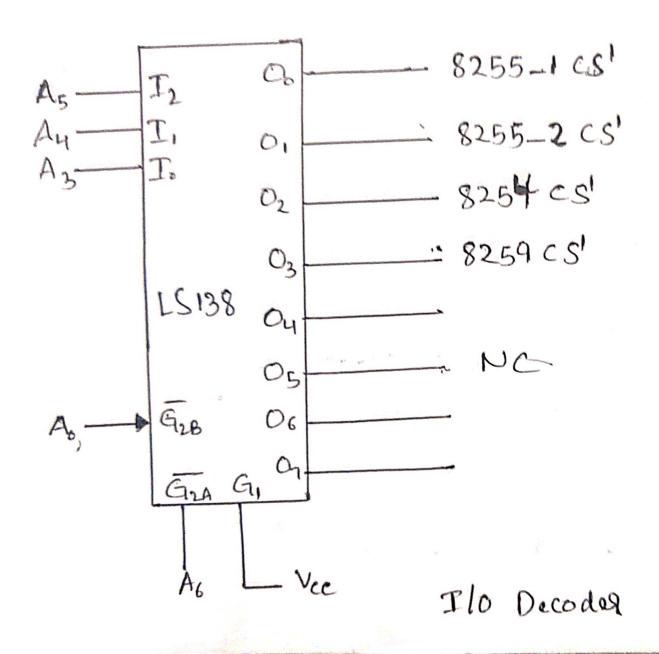


M/IO'-	D' -	MEMR'
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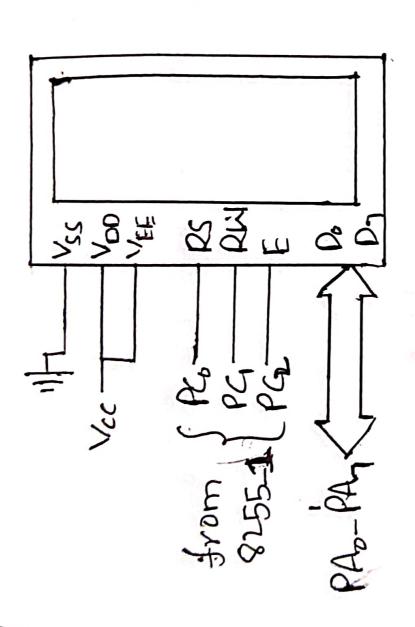
M/IO"	RDI	MR'	Bus cycle
1	0	1	MEMR'
	1	0	MEMW'
0	0	l,	IOR'
0	1	0	Iow'





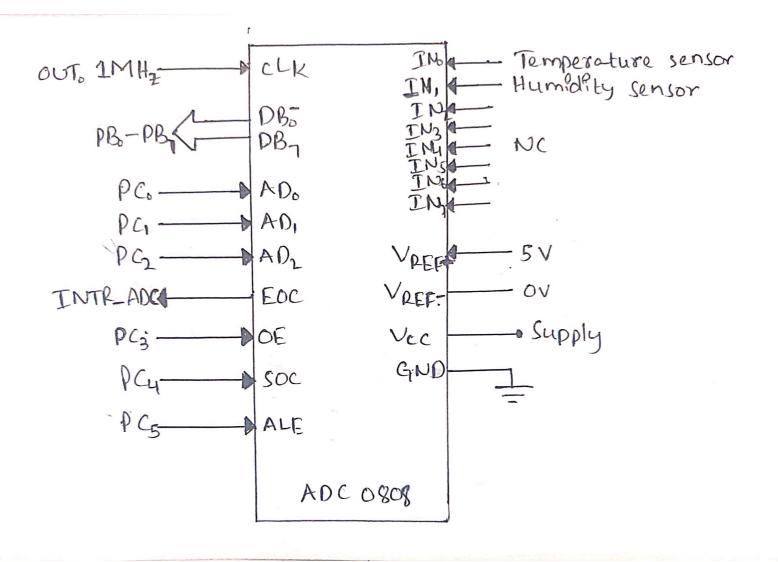


82551Interface	to
proces sor	,
A,	Ao
A2	A
8255-1 csl	cs
	8255_1
TOR -	RD
TOW	WR
Do-Di	$D_0 - D_{\gamma}$
ZESET from 8284	REJET.
	l



(16x) ALPHANOMERIC LCD DISPLAY) LCD Interfacting LMOIGL

8255-2 Interface to processor 8-255_2cs'-8255-2 RO TOR TOW from 8284 RESET



8254 Interface to the Processor 8254CS'-8254 TOR TOW

	CLK 5MHz	CLKo	OUTO	Count=5d
	5 V &	GATE	mode ₃	
	100 HZ	OUT,	CLK,	5MH2
	5v	GATE	made ₂	Counts 50000d
		CLK2	OUT ₂	2minutes
	5V	GATE ₂	mode 2	Count-12000d TimesINT

