Mini Project
ECE213 Digital Electronics

LOVELY PROFESSIONAL UNIVERSITY
Transforming Education Transforming India

Topic Name - Ten Bit Even Parity Generator

Date of allotment:02/03/2017
Date of submission:
Submitted to- Garima Rana

Name : Siddhant Saurabh
Roll No: 11602270 B-46
Section: K1630

Acknowledgement

I ,Siddhant Saurabh, thanks my Digital Electronic Madam Garima Rana for giving the chance to write a report on Ten Bit Even Parity Generator. Electronics is the heart of a computer so it has always fascinated me. I extend my gratitude to my brother and my friends for helping me with various materials for my report.

Contents

Introduction

In digital systems, when binary data is transmitted and processed , data may be subjected to noise such that such noise can alter 0s (of data bits) to 1s and 1s to 0s, the cause may be whatsoever.

And this noise increases with increase in length of transmission range so repeaters is also require for checking at regular intervals.

Parity Generators are the bits attached to the message bits to check the null and voiding of these message bits occured due to noise.

Parity Generators

The parity generating technique is one of the most widely used error detection techniques for the data transmission.

A parity generator is a combinational logic circuit that generates the parity bit in the transmitter.

On the other hand, a circuit that checks the parity in the receiver is called parity checker.

A combined circuit or devices of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data word.

Working Principle of Infrared Sensors

The basic principle involved in the implementation of parity circuits is that sum of odd number of 1s is always 1 and

sum of even number of 1s is always zero. Such error detecting and correction can be implemented by using Ex-OR gates.

Disadvantages of this method is that only one bit errors can be detected. It also increases the data size that is to be transmitted.

Different types of Parity Generators

The sum of the data bits and parity bits can be even or odd .

In even parity, the added parity bit will make the total number of 1s an even amount whereas

in odd parity the added parity bit will make the total number of 1s odd amount.

Methods of using Parity

1st Method

Parity bit is added at the last of the word containing data.

Thus that bit is used to detect errors, during the transmission of binary data.

The message containing the data bits along with parity bit is transmitted from transmitter node to receiver node.

At the receiving end, the number of 1s in the message is counted and if it doesn’t match with the transmitted one, then it means there is an error in the data.

Disadvantages

In this if the parity does not match then the data is discarded so wastage of the resources.

2nd Method

Parity bits are widely used in Generation of Humming Code (Single bit error Detection Code). Here it is also used for detecting the error correcting the message up to 1 bit in the received Humming Code so data is not wasted assuming that only one bit error can only could at max happen.

Disadvantage

In this the data size increases more than the 1st Method.

My evaluation of 10 Bit Parity Generator

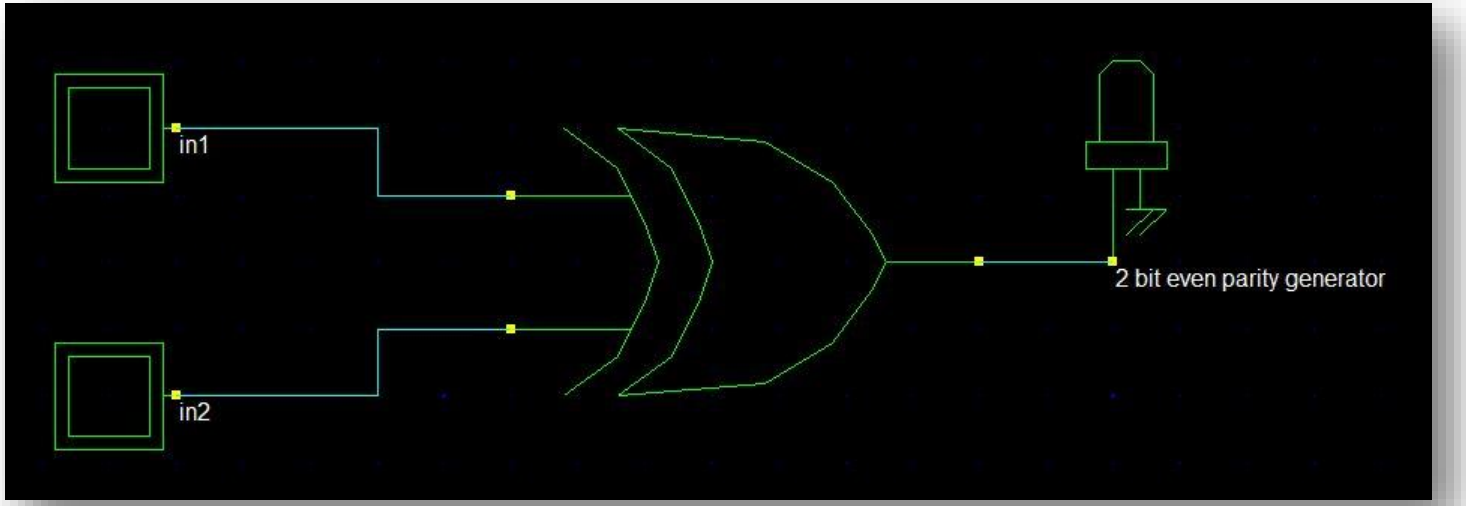
My task was to realize 10 bit even parity Generator. But it Includes 1024 case which I found using permutation of 10 input.

More over I needed to generate the K-Map along with the 1024 gray codes for the 10 inputs for simplifying which is huge error prone task.

I went to shock almost but then I remember it is Lpu.

Nothing is difficult here.

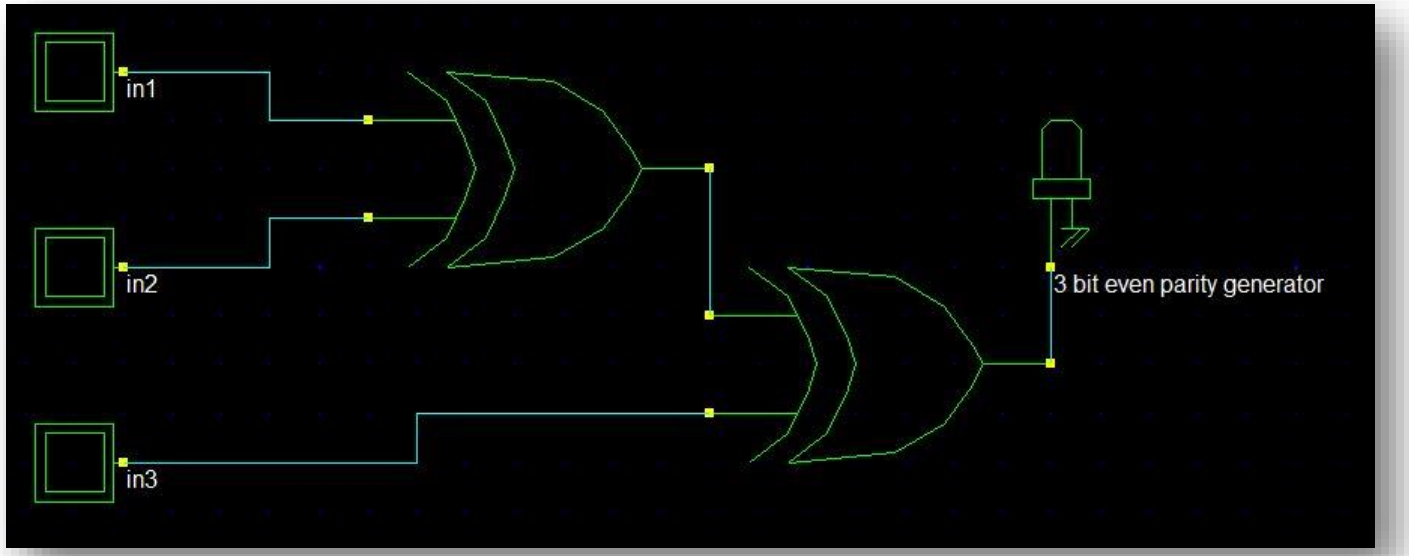
- So I first realized 2 bit Even parity Generator.



Inputs		Outputs
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

$$= (A \oplus B)$$

Then I realize 3 bit Even parity Generator.



3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

A \ BC	00	01	11	10
00	0 (0)	1 (1)	0 (3)	1 (2)
01	1 (4)	0 (5)	1 (7)	0 (6)

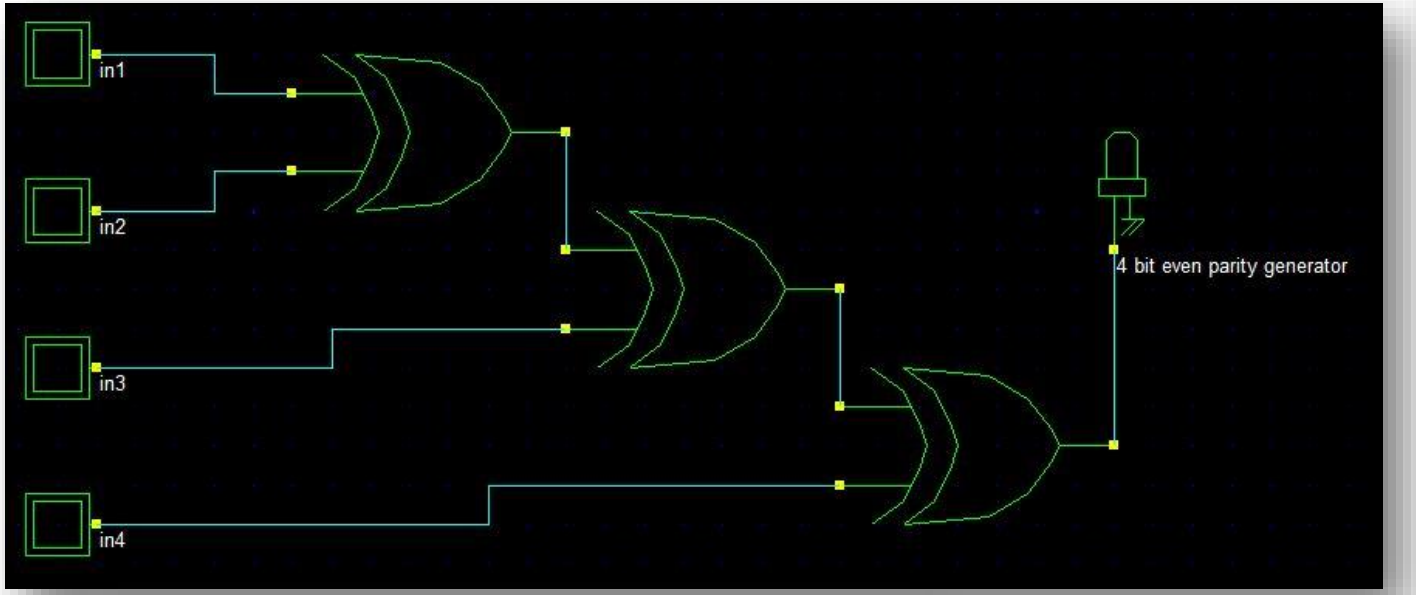
$$P = \bar{A}\,\bar{B}\,C + \bar{A}\,B\,\bar{C} + A\,\bar{B}\,\bar{C} + A\,B\,C$$

$$= \bar{A}\,(\bar{B}\,C + B\,\bar{C}) + A\,(\bar{B}\,\bar{C} + B\,C)$$

$$= \bar{A}\,(B \oplus C) + A\,(\overline{B \oplus C})$$

$$P = A \oplus B \oplus C$$

Then I realized 4 bit Even Parity Generator.



4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

CP / AB	00	01	11	10
00	0 (0)	1 (1)	0 (3)	1 (2)
01	1 (4)	0 (5)	1 (7)	0 (6)
11	0 (12)	1 (13)	0 (15)	1 (14)
10	1 (8)	0 (9)	1 (11)	0 (10)

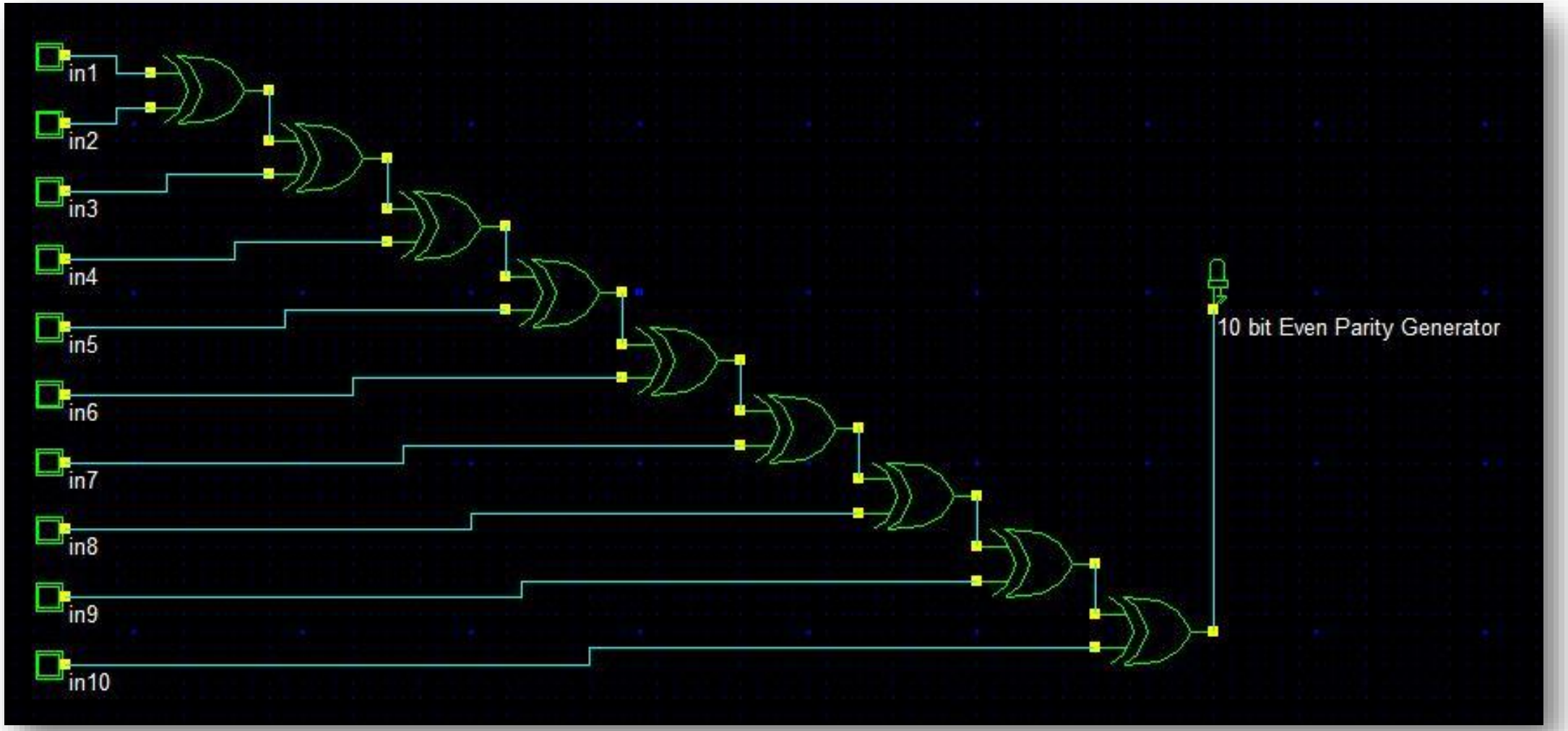
$$PEC = \bar{A}\,\bar{B}\,(\bar{C}\,D + C\,\bar{D}) + \bar{A}\,B\,(\bar{C}\,\bar{D} + C\,D) + A\,B\,(\bar{C}\,D + C\,\bar{D}) + A\,\bar{B}\,(\bar{C}\,\bar{D} + C\,D)$$

$$= \bar{A}\,\bar{B}\,(C \oplus D) + \bar{A}\,B\,(\overline{C \oplus D}) + A\,B\,(C \oplus D) + A\,\bar{B}\,(\overline{C \oplus D})$$

$$= (\bar{A}\,\bar{B} + A\,B)\,(C \oplus D) + (\bar{A}\,B + A\,\bar{B})\,(\overline{C \oplus D})$$

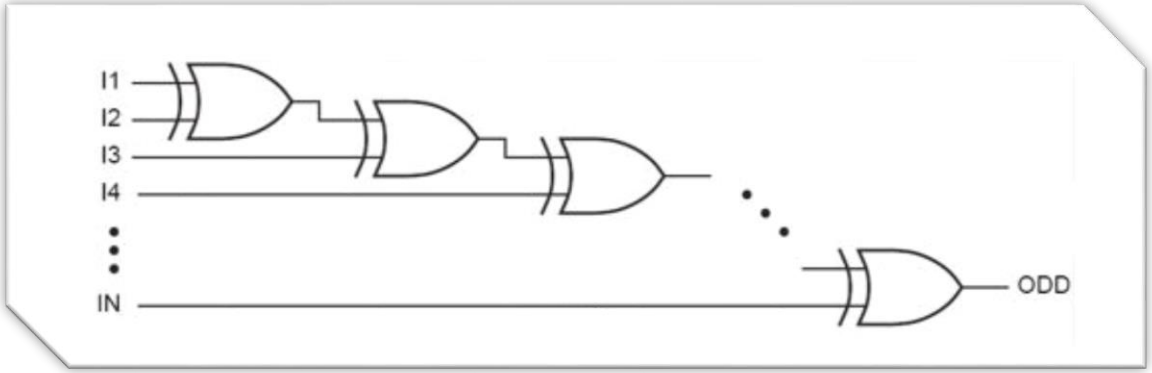
$$= (A \oplus B) \oplus (C \oplus D)$$

I realized that there is a pattern common in all the above even parity generator, so the 10 bit Even Parity Generator should also follow this pattern. Therefore I don't need to generate the truth table for so many 1024 case. I don't need to generate the complicated K-Map for it and I don't need to simplify it.



Futuristic Scopes.

As the technology will grow then the noise in the transmission of data will decrease in the same pace, than at that moment we can use the generalized even parity generator for n bits.



Conclusion

Checking the validity of data is a must case before processing that data. and parity generators / checkers help is a boon in this case and for Even parity bit for any no. of bits require only XOR gate.

Reference

- Wikipedia
- Google Image Search