VLSI SYSTEM DESIGN LAB(ECE3001)

(BY PROF.JAGANNADHA NAIDU K)

TASK-2

CMOS INVETRER AND 2INPUT NOR GATE ANALYSIS

SLOT-L23+L24

NAME:SIDDHANT AGARWAL

REGISTER NO:-17BEC0431

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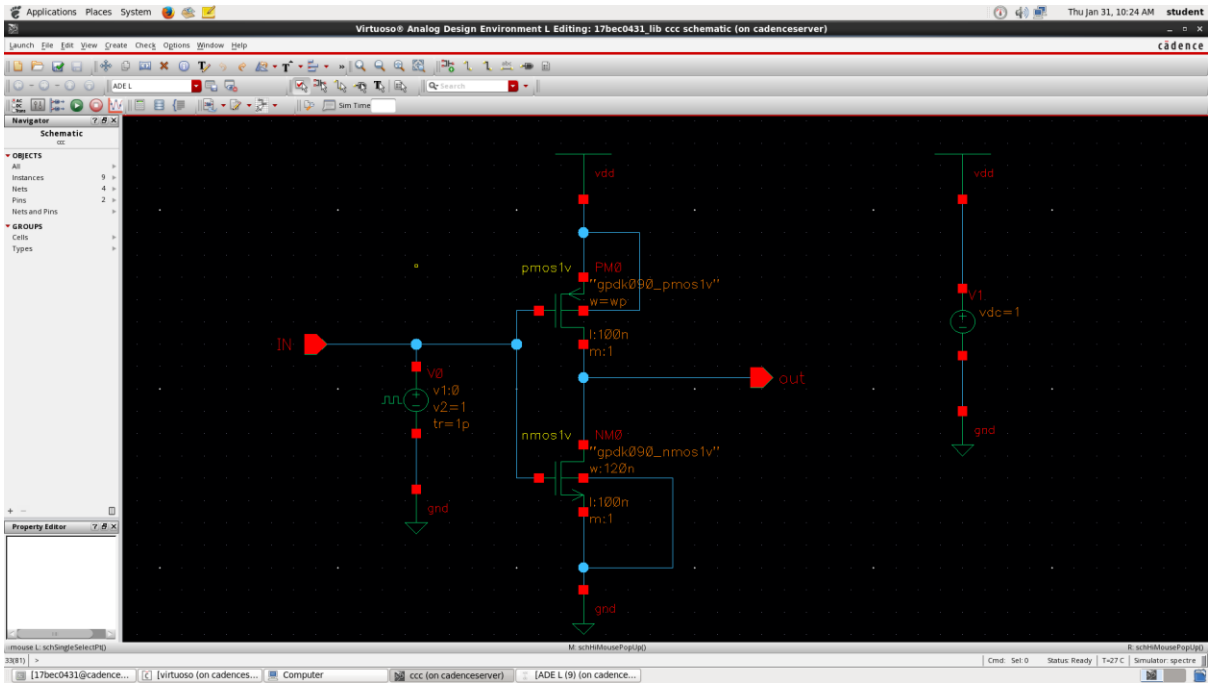
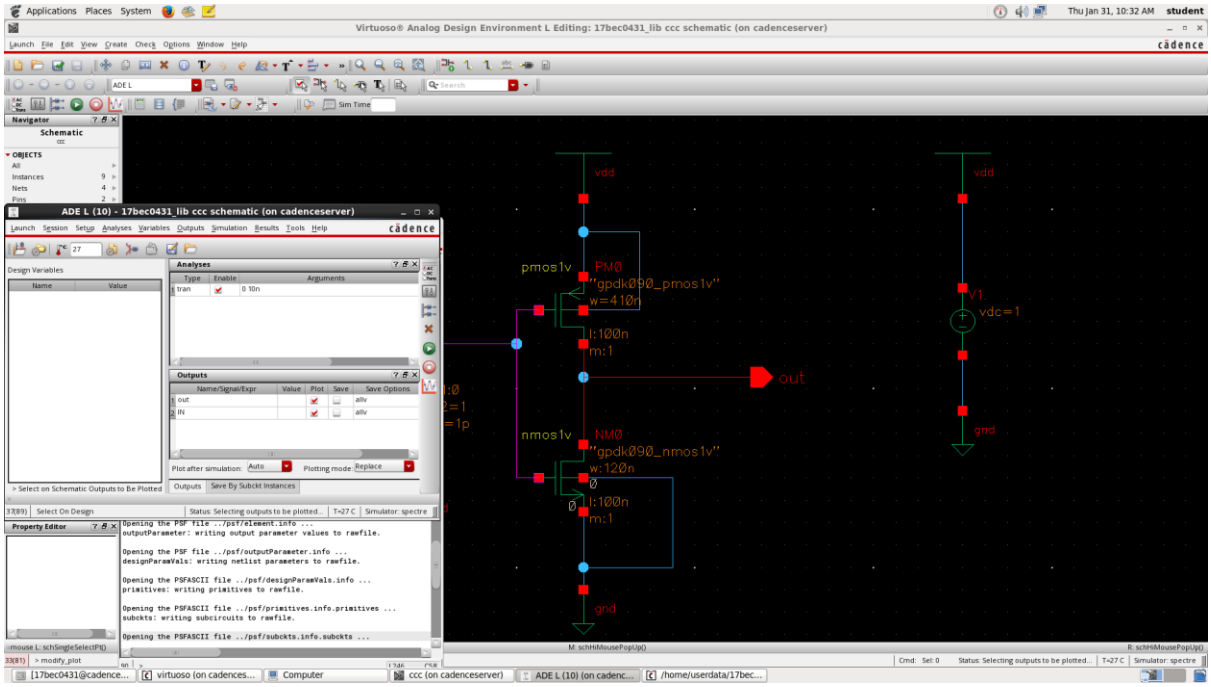
TASK-2A

AIM:TO measure the voltage transfer characteristics of CMOS inverter and measure the time delay and average power dissipation.

CIRCUIT DIAGRAM





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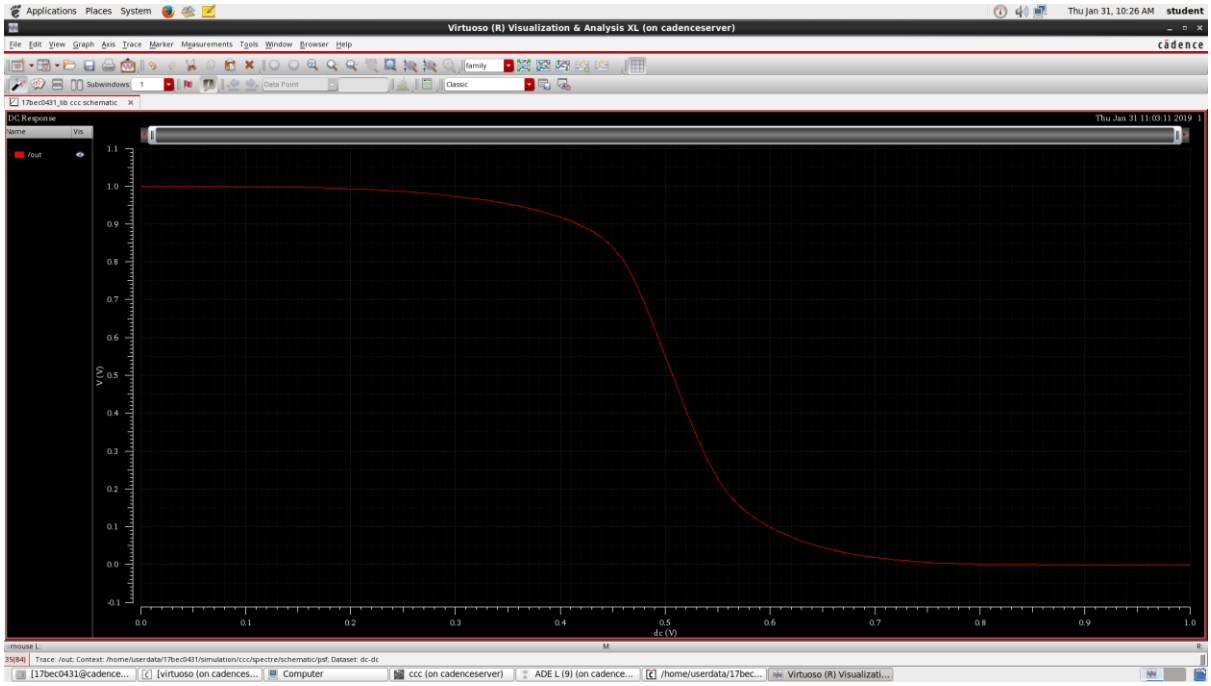
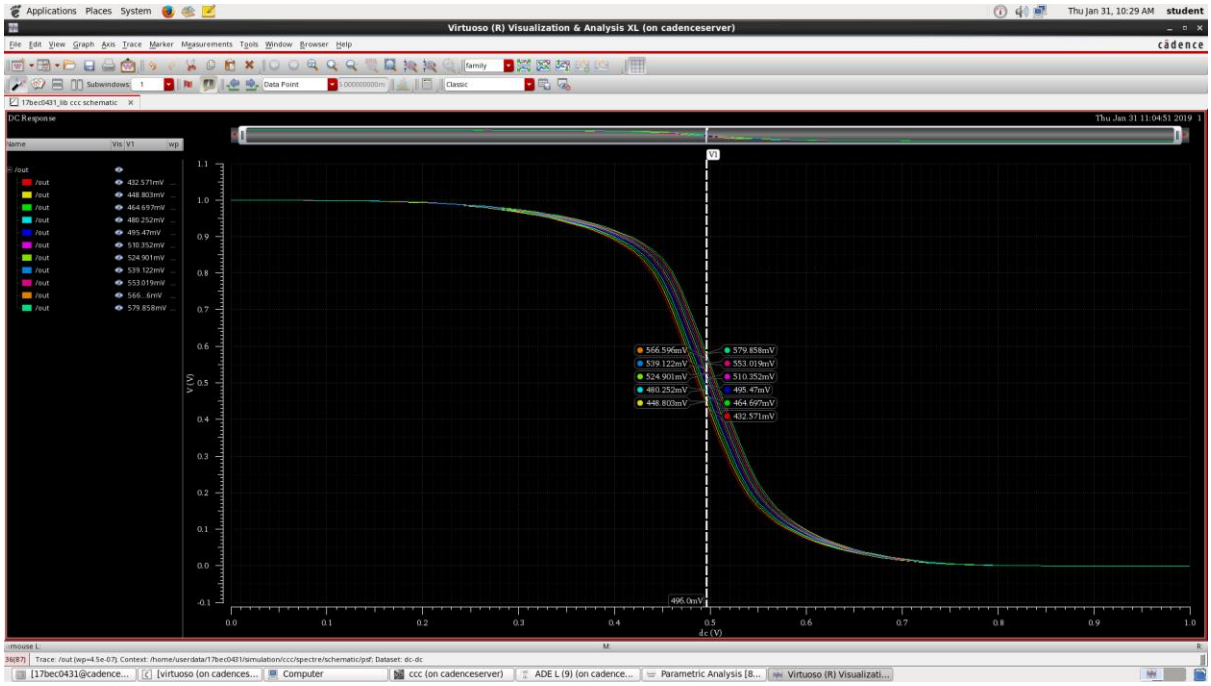
PLOTS:

DC TRANSFER CHARACTERISTICS



PARAMETRIC ANALYSIS FOR W_P



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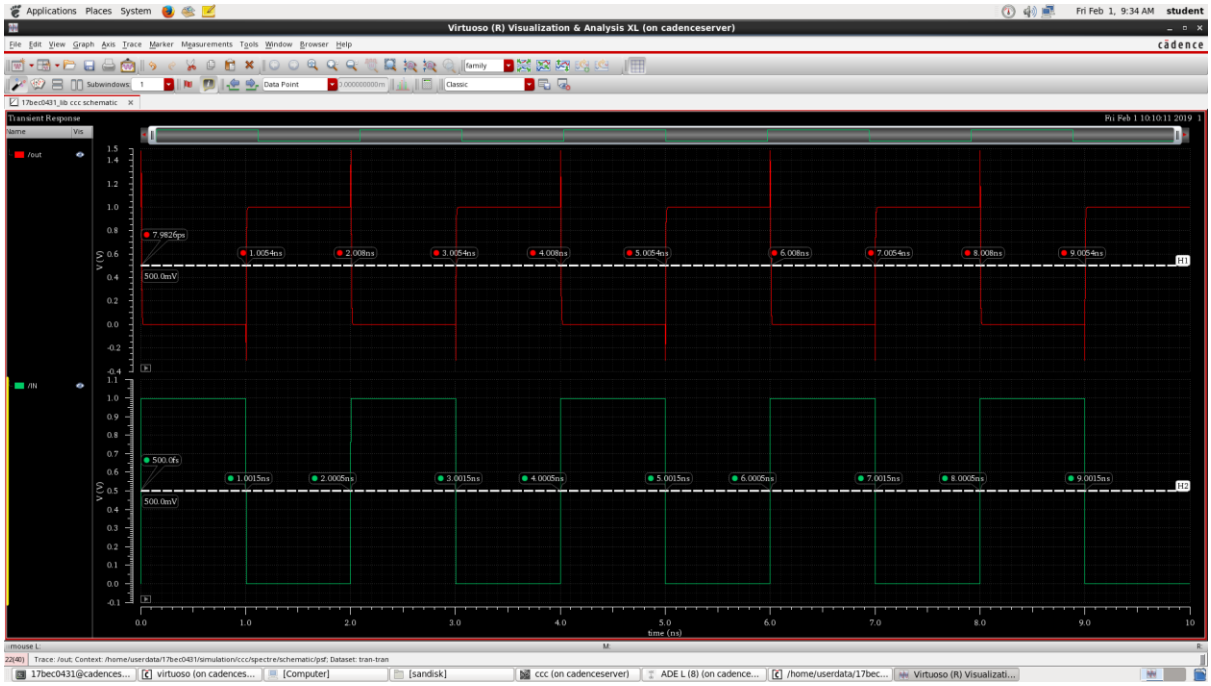
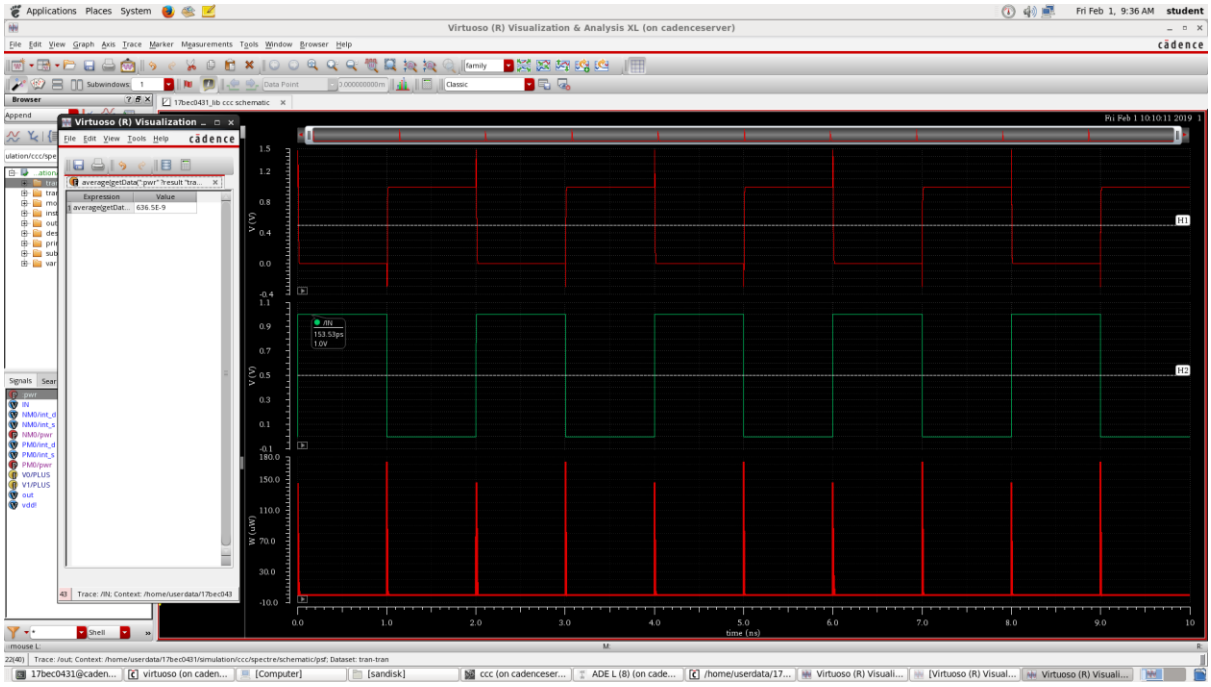
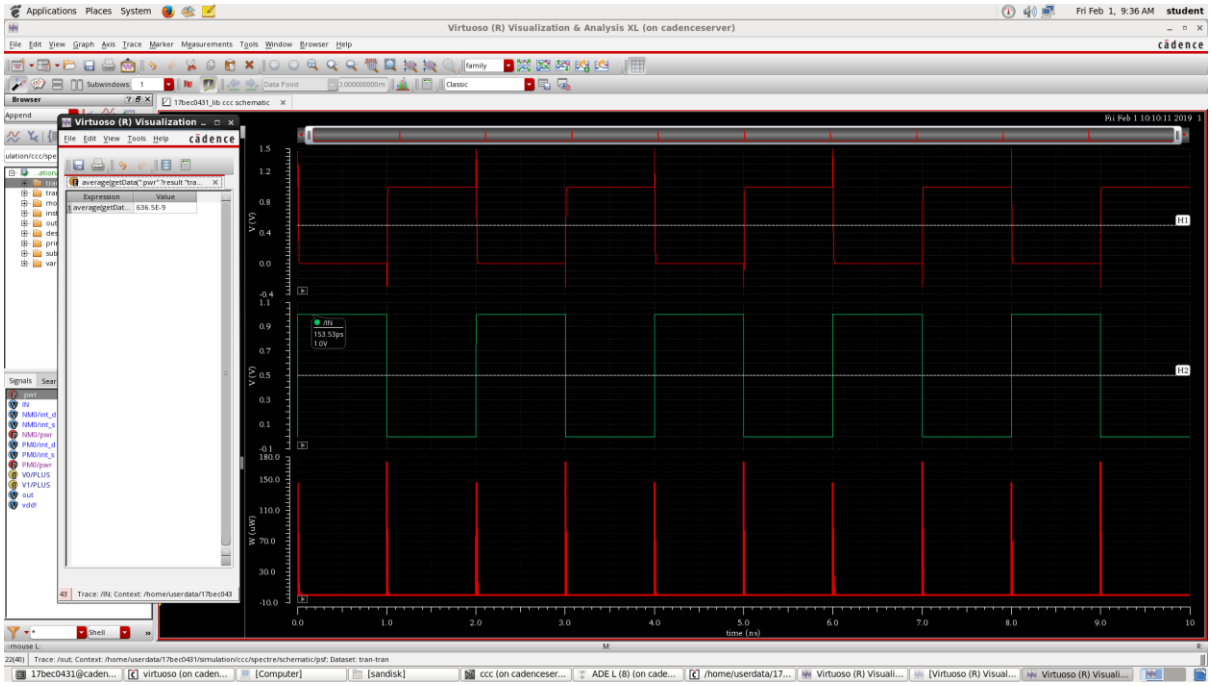
TIME DELAY



POWER CLACULATION GRAPH USING .PWR SIGNAL





FOLLOWING ARE THE OBSERVATIONS TAKEN FROM ABOVE GRAPHS

(Rising falling delay) T_{pdrf}=7.483ps

(Falling rising delay) T_{pdfr}=3.91ps

Propagation delay=(T_{pdrf}+T_{pdfr})/2 =5.69ps

Average power dissipation=636.5 X10^-9

INFERENCE

We GET $V_{IN}=V_{DD}/2=V_{OUT}$

At $B_n=B_p$

RESULT

(Rising falling delay) T_{pdrf}=7.483ps

(Falling rising delay) T_{pdfr}=3.91ps

Propagation delay=(T_{pdrf}+T_{pdfr})/2 =5.69ps

Average power dissipation=636.5 X10^-9

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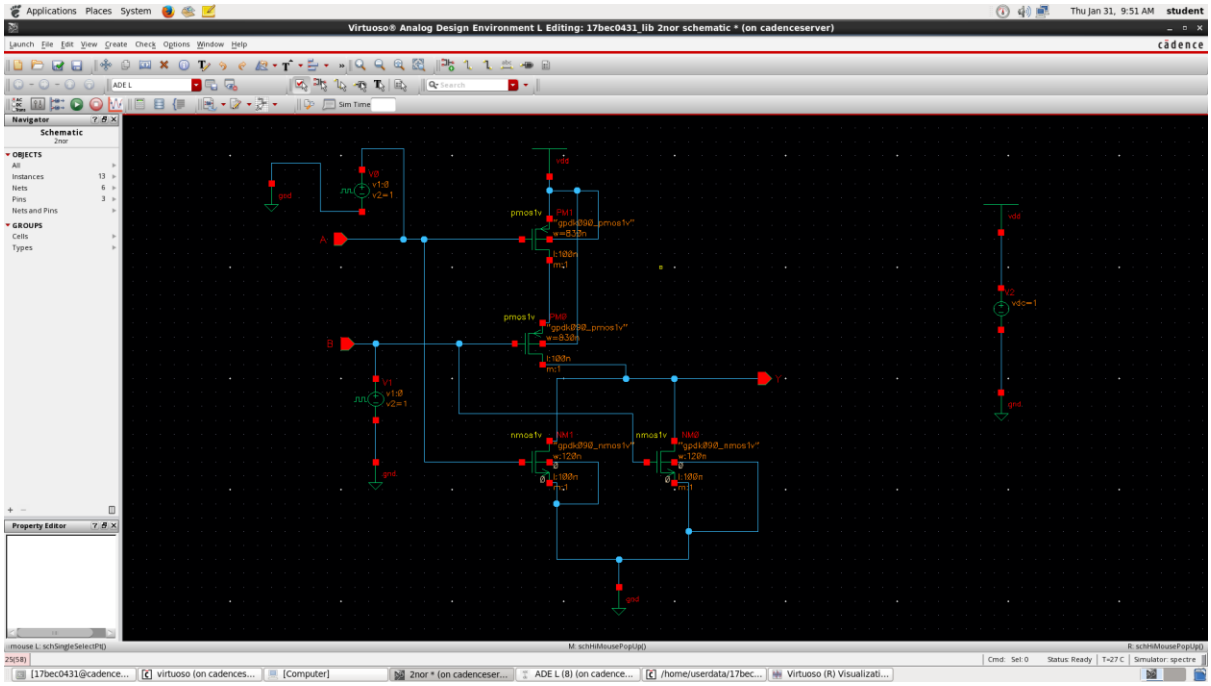
TASK2-B

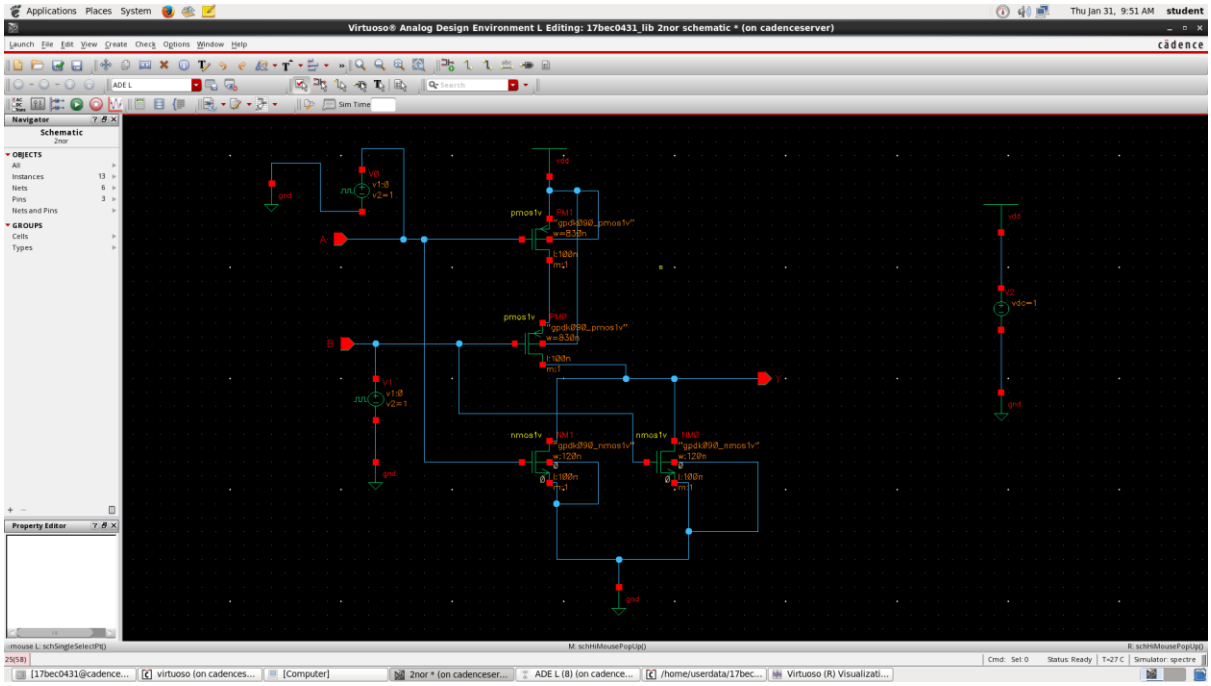
AIM :To examine the transient characteristic of CMOS 2 input NOR gate and also to calculate the delay and average power.

CIRCUIT DIAGRAM

When both A and B are varying(tphl)



When only A is varying and B is set to 0V dc(tphl)



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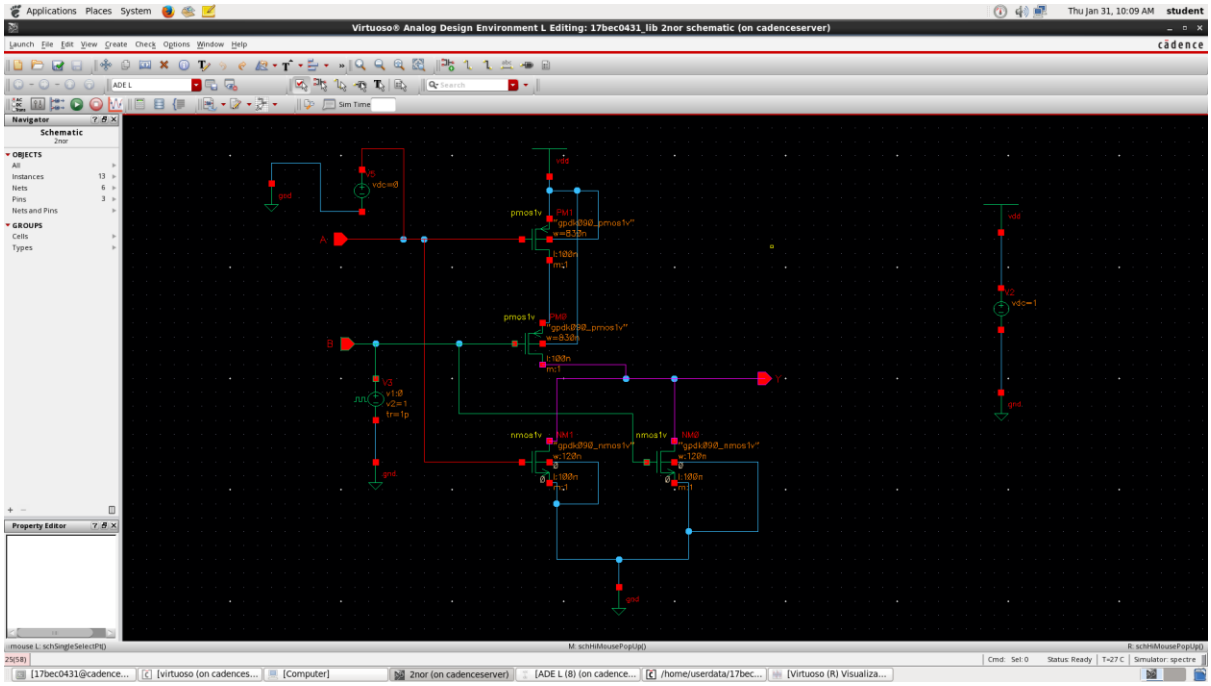
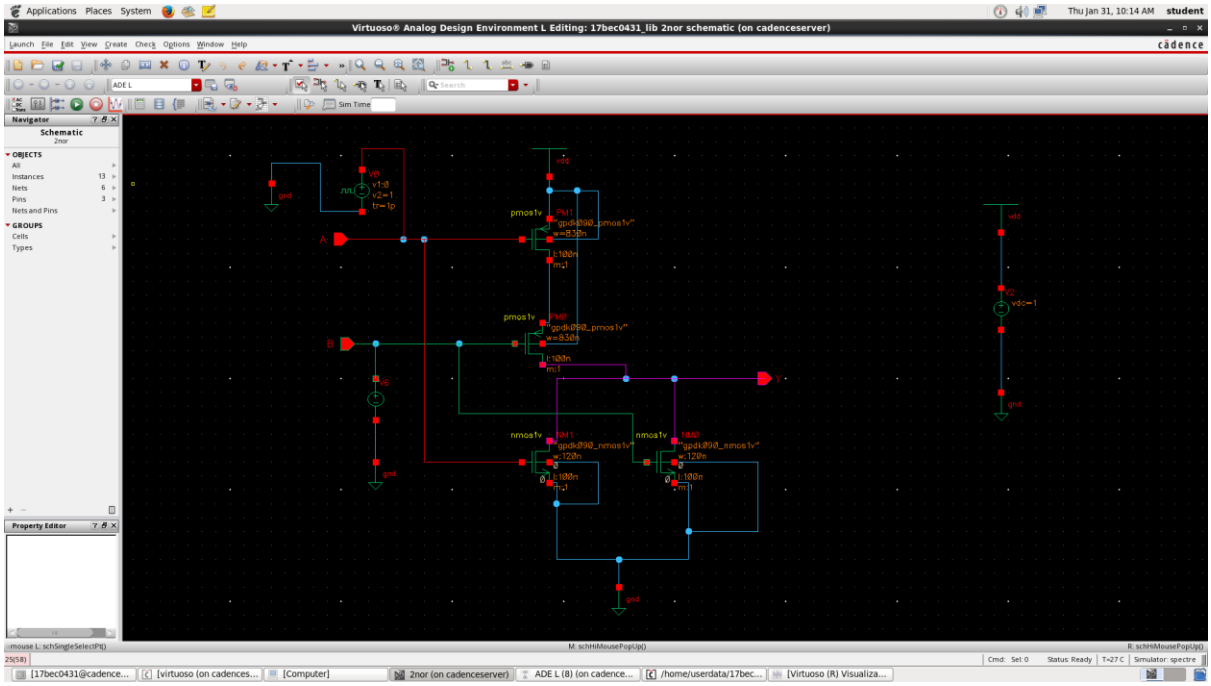
When A is set to 0V dc and B is varying(tplh)



When A is varying and B is set to 0V(tplh)



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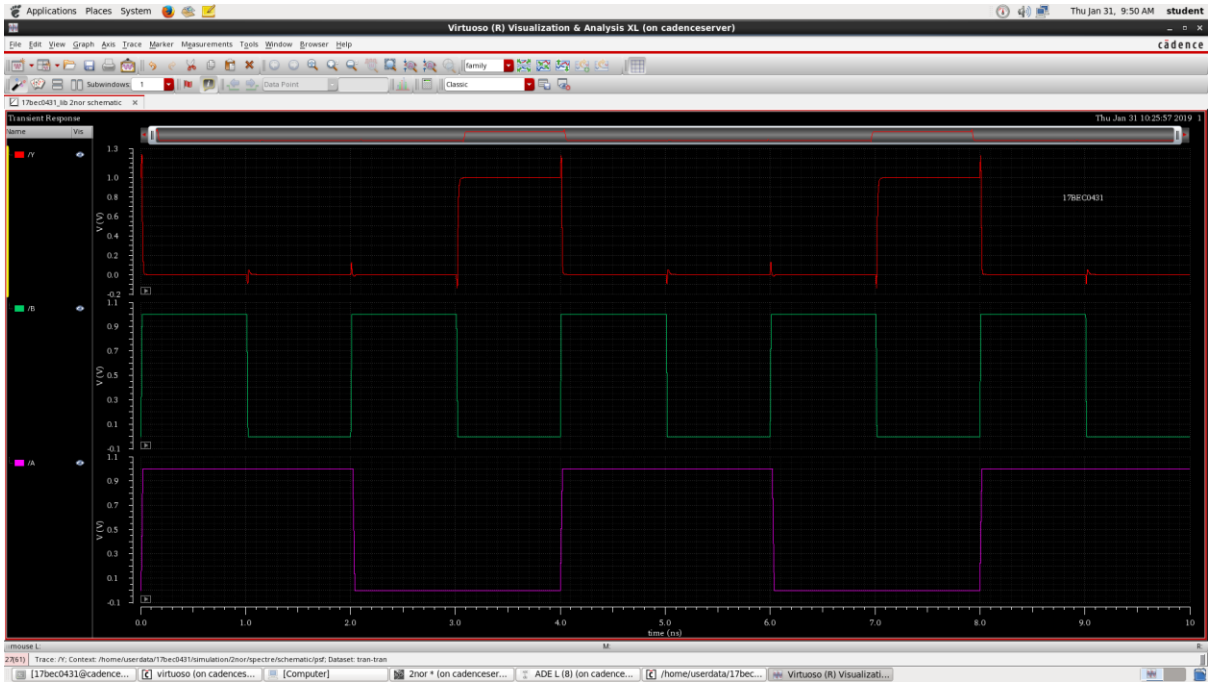
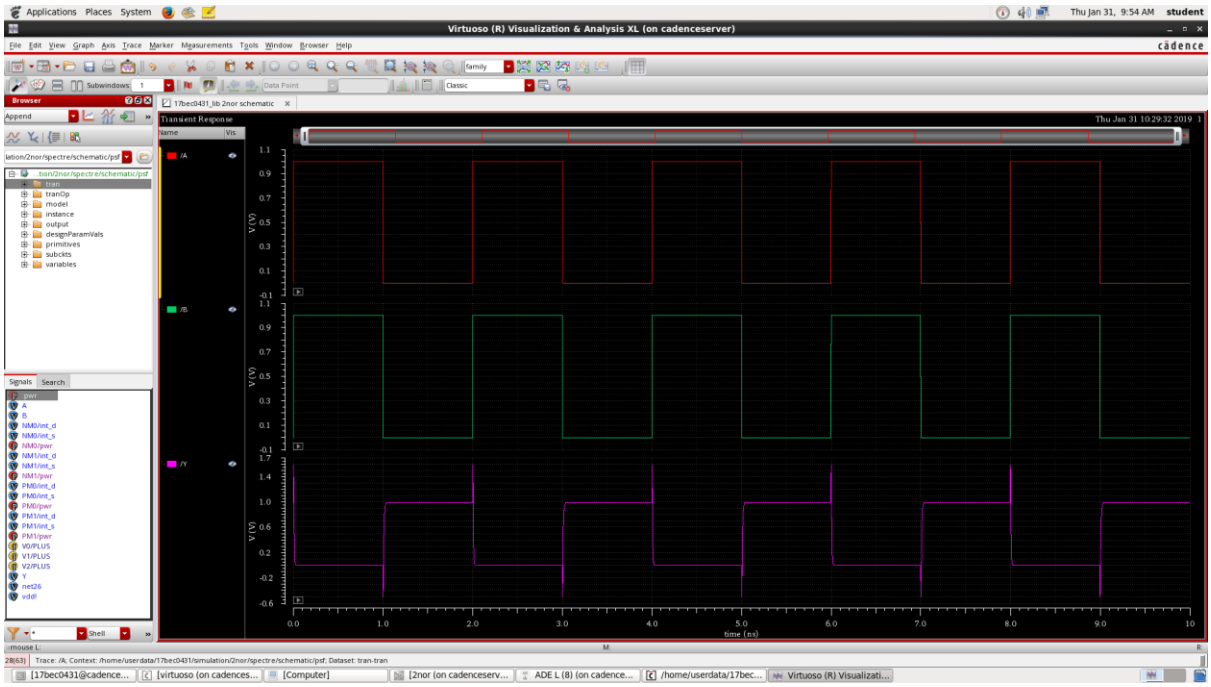
PLOTS

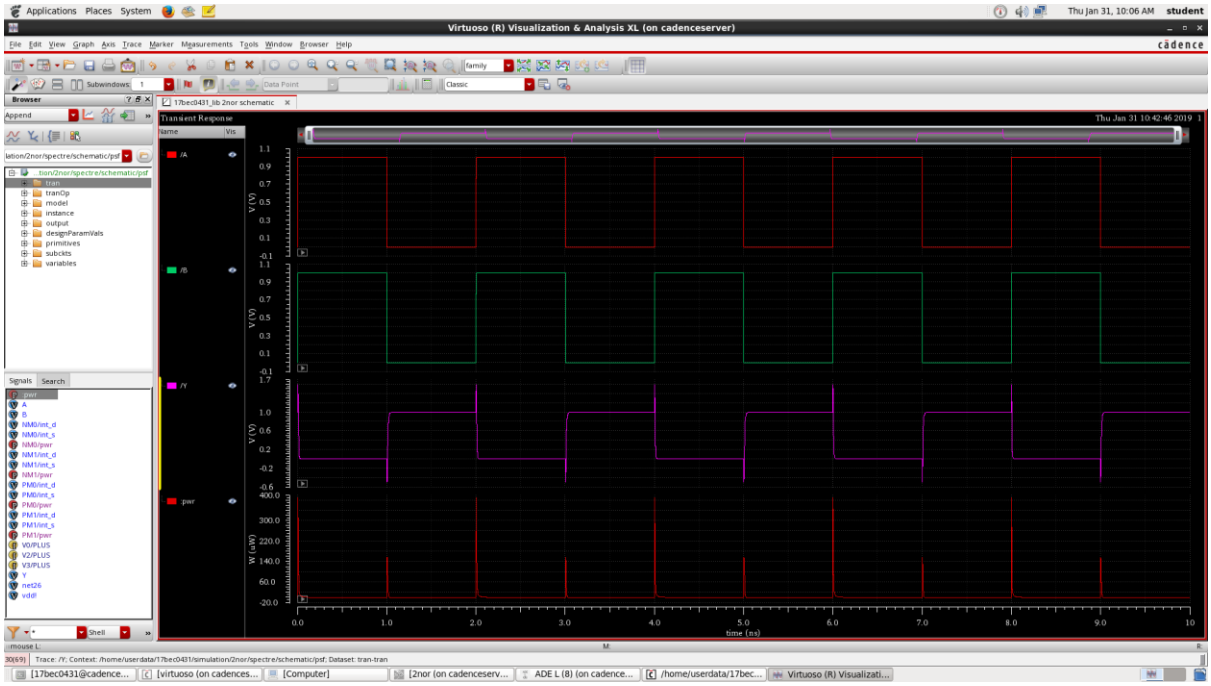
FUNCTIONALITY(WHERE A AND B ARE INPUTS AND Y IS OUTPUT)



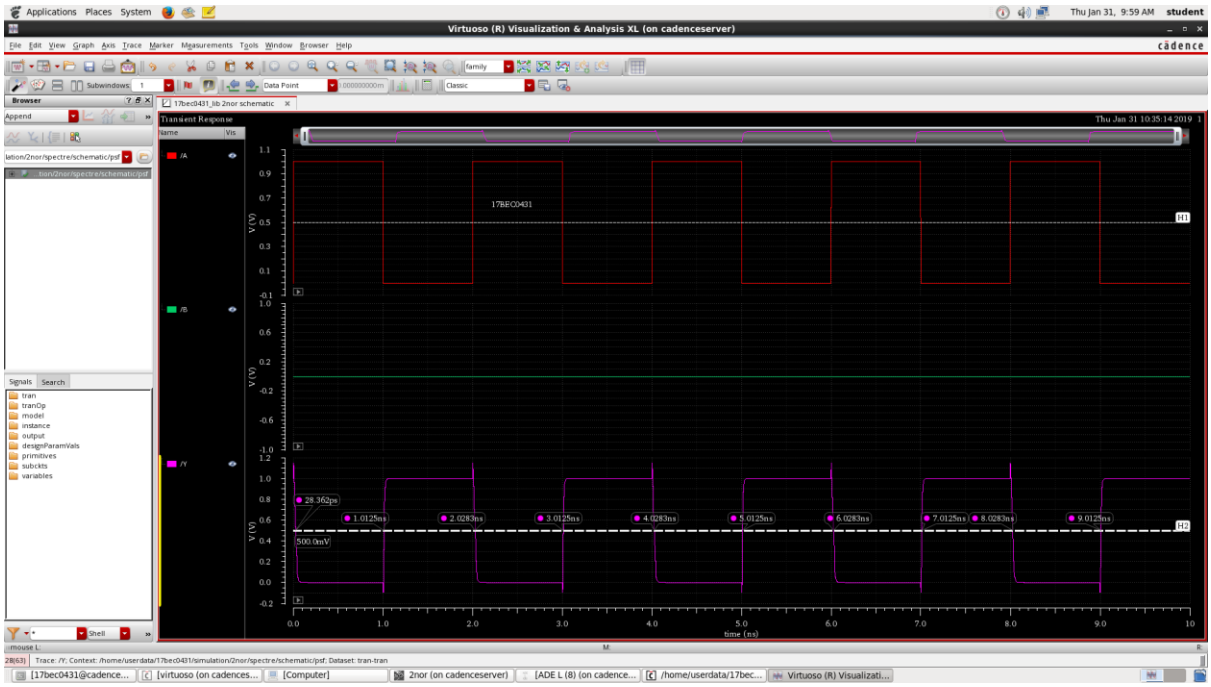
CASE1: (00 TO 11)(T_{phl})



Case1 with .pwr signal



Case2 (00->10)(T_{phl})



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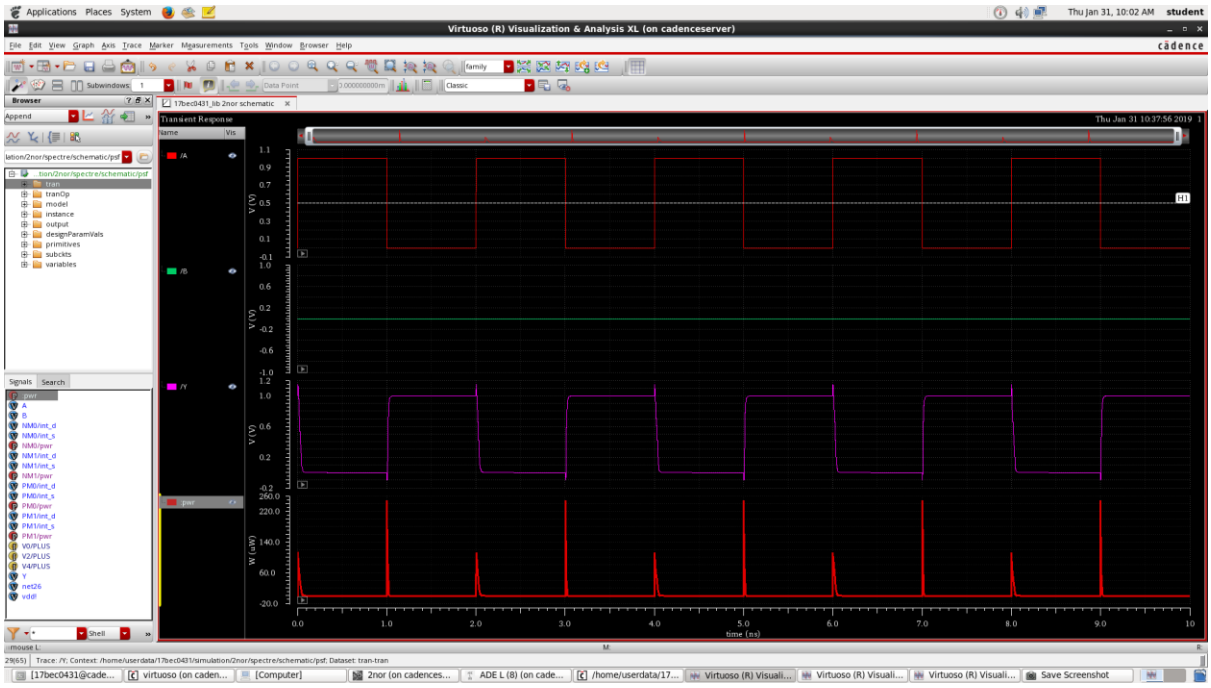
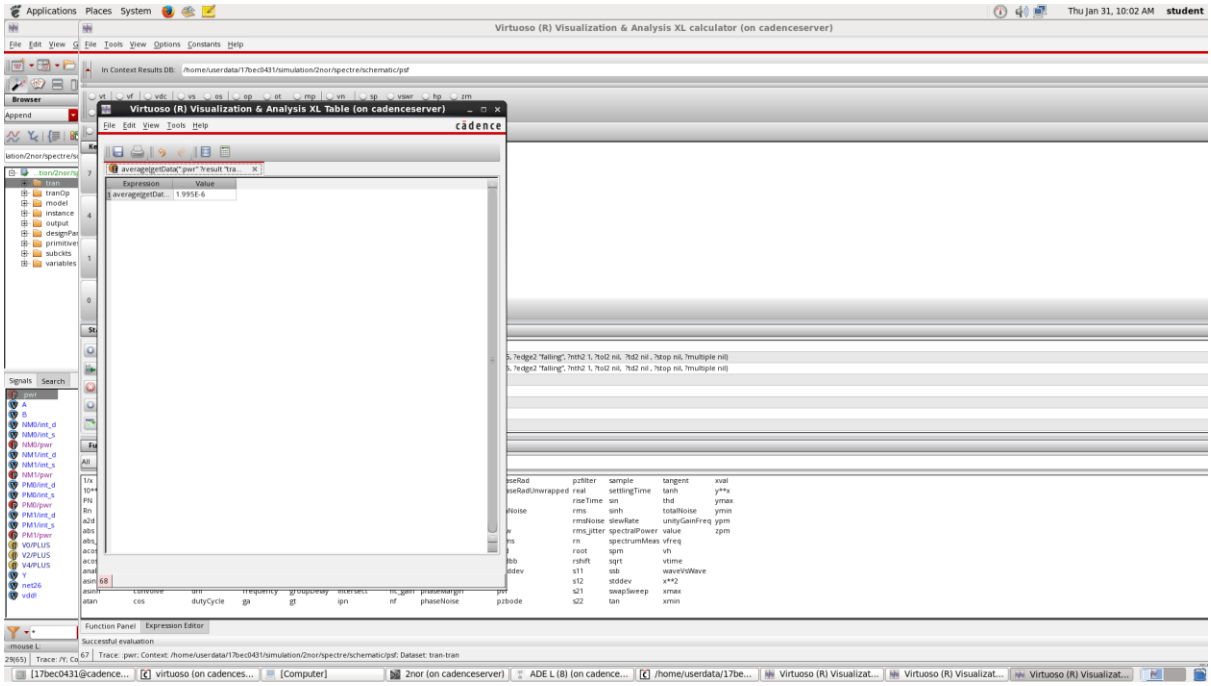
Case2:with .pwr signal



Case2:calculated average power



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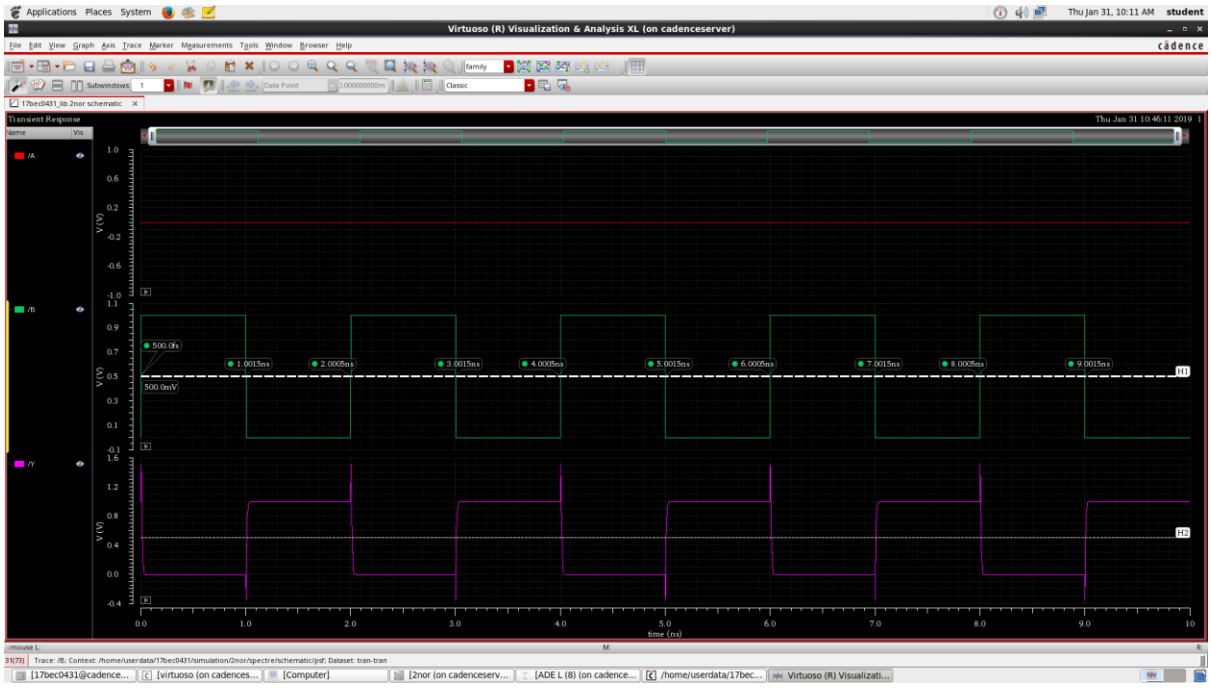
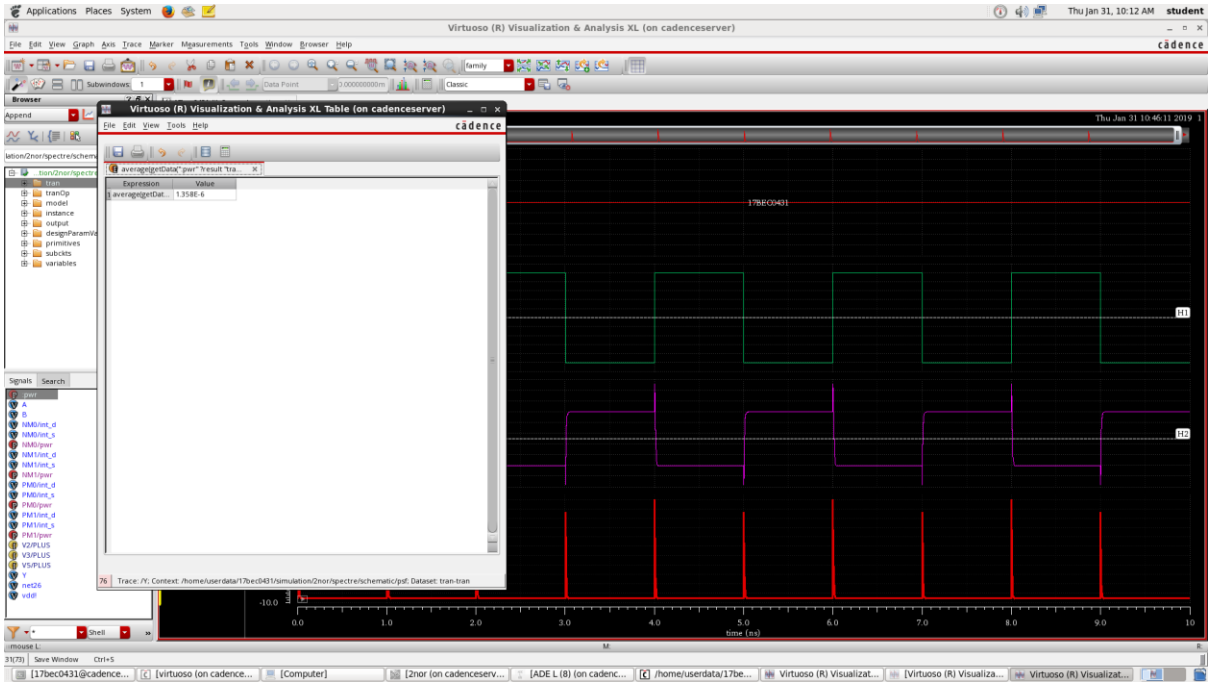
Case3 (10->00)(T_{plh})



Case3:with .pwr and average power



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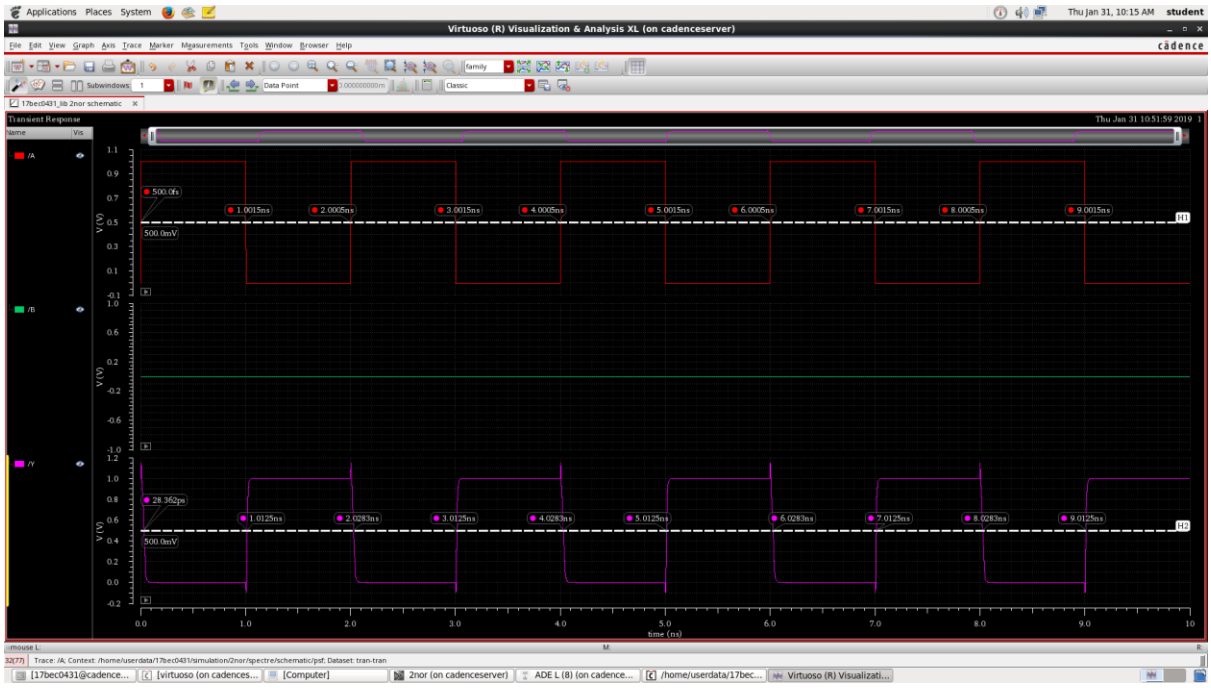
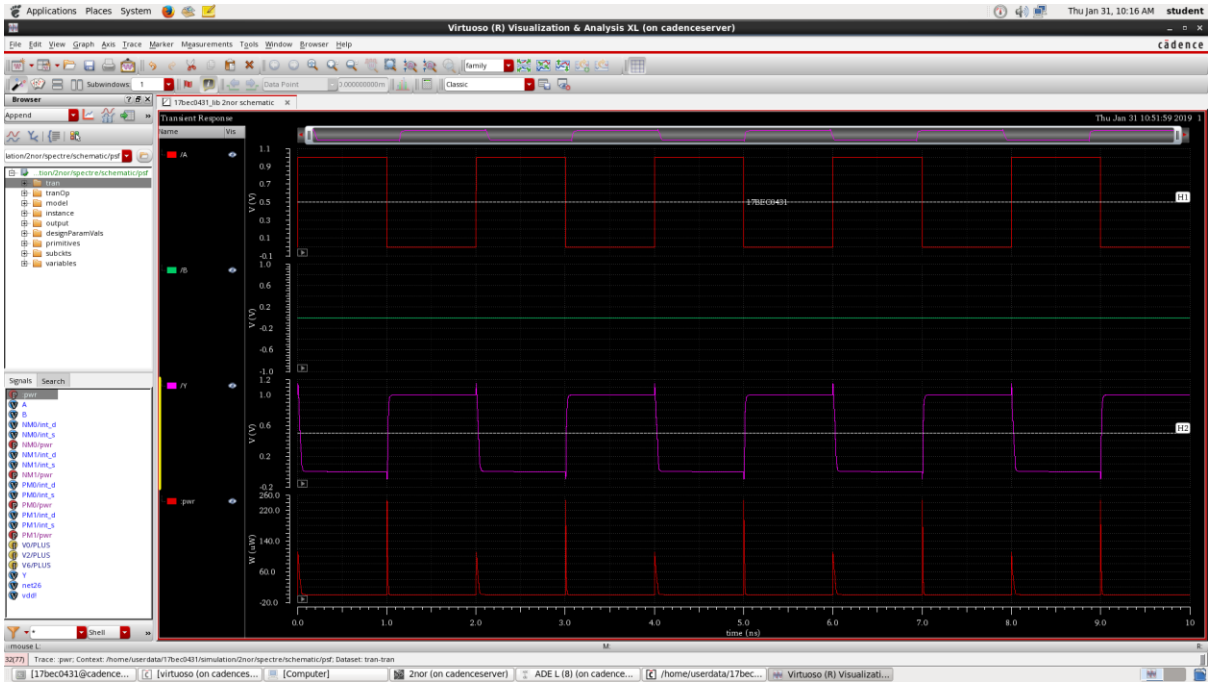
Case4: (10->00)(T_{plh})



Case4:with .pwr signal



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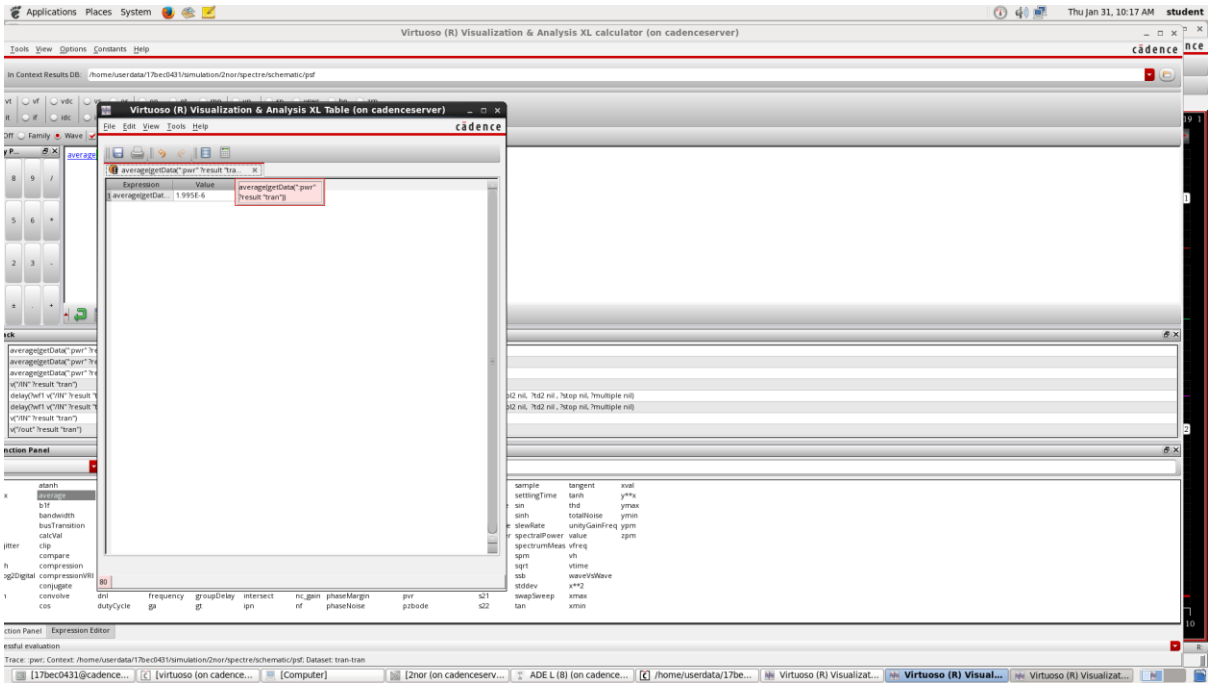
Case4: calculated average power



OBSERVATION

INPUT COMBINATIONS	SIGNAL MODE	TIME DELAY	AVERAGE POWER
00->11(A->Y)	Tp->high to low	9.4ps	2.18x10^-6
00->10(A->Y)	Tp->high to low	23.3ps	1.995x10^-6
01->00(B->Y)	Tp->low to high	7.6ps	1.35x10^-6
10->00(A->Y)	Tp->low to high	11ps	1.995x10^-6

INFERENCE:

When both the inputs are varying ,the average power is higher than other inputs.

Result:

Case1:time delay 9.4ps **average power** 2.18x10^-6

Case2: time delay 23.3ps **average power** 1.995x10^-6

Case3: time delay 7.6ps **average power** 1.35x10^-6

Case4: time delay 11ps **average power** 1.995x10^-6