VLSI SYSTEM DESIGN LAB(ECE3001)

(BY PROF.JAGANNADHA NAIDU K)

LAB TASK-5

SUB-SYSTEM DESIGN ALU

SLOT-A2

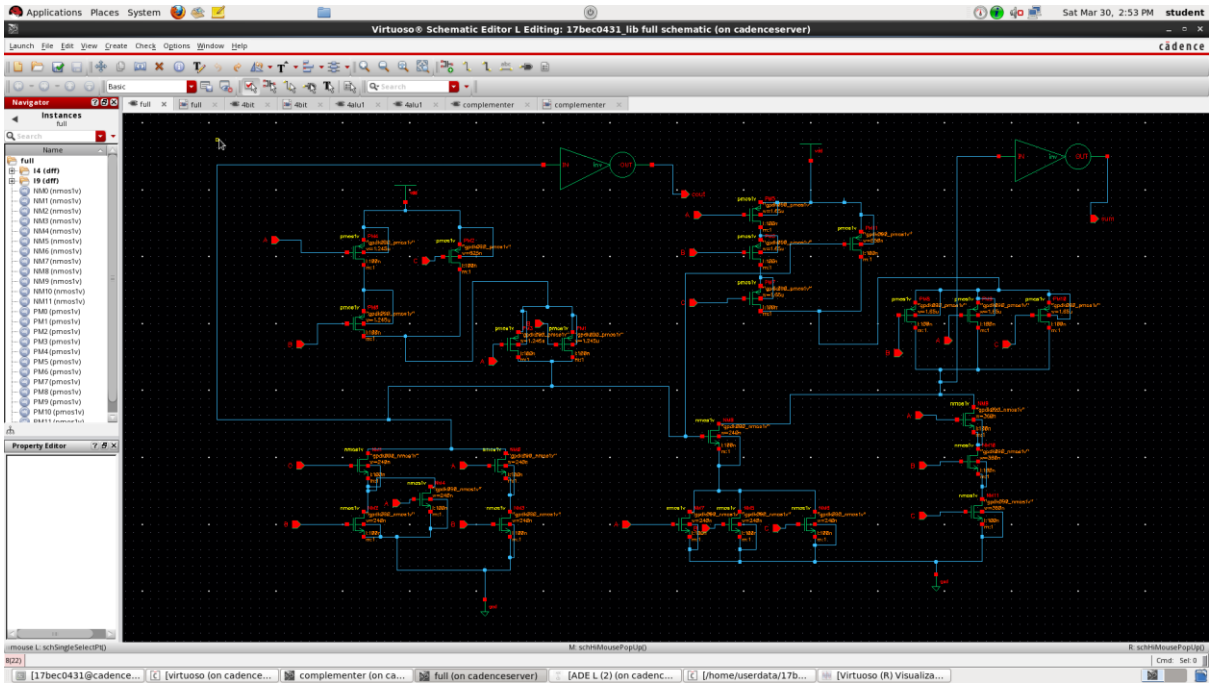
NAME:SIDDHANT AGARWAL

REGISTER NO:-17BEC0431

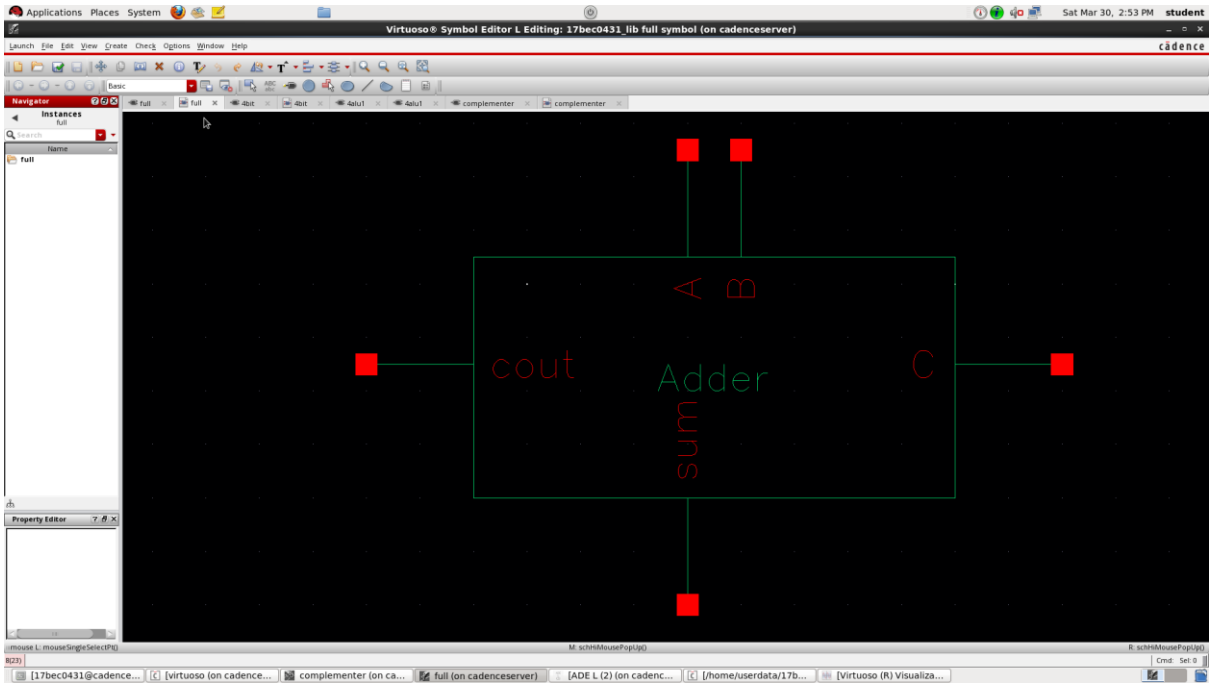
VLSI SYSTEM DESIGN **NAME:SIDDHANT AGARWAL**

REG NO:17BEC0431

FULL ADDER



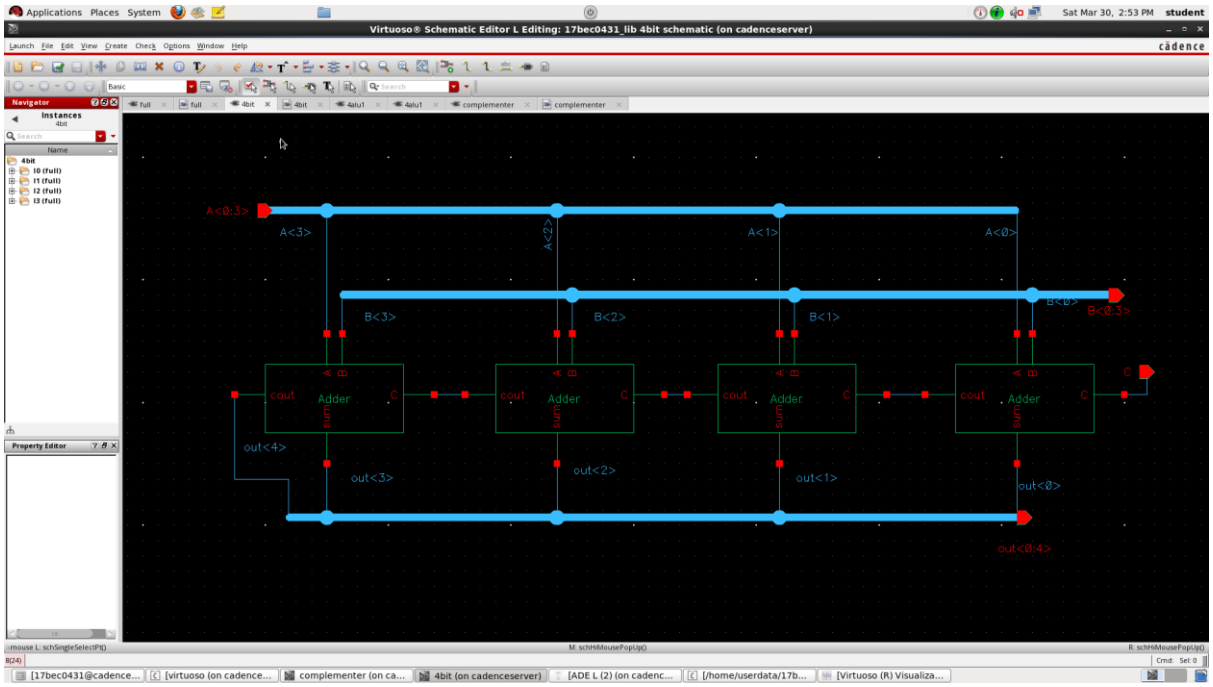
FULL ADDER SYMBOL



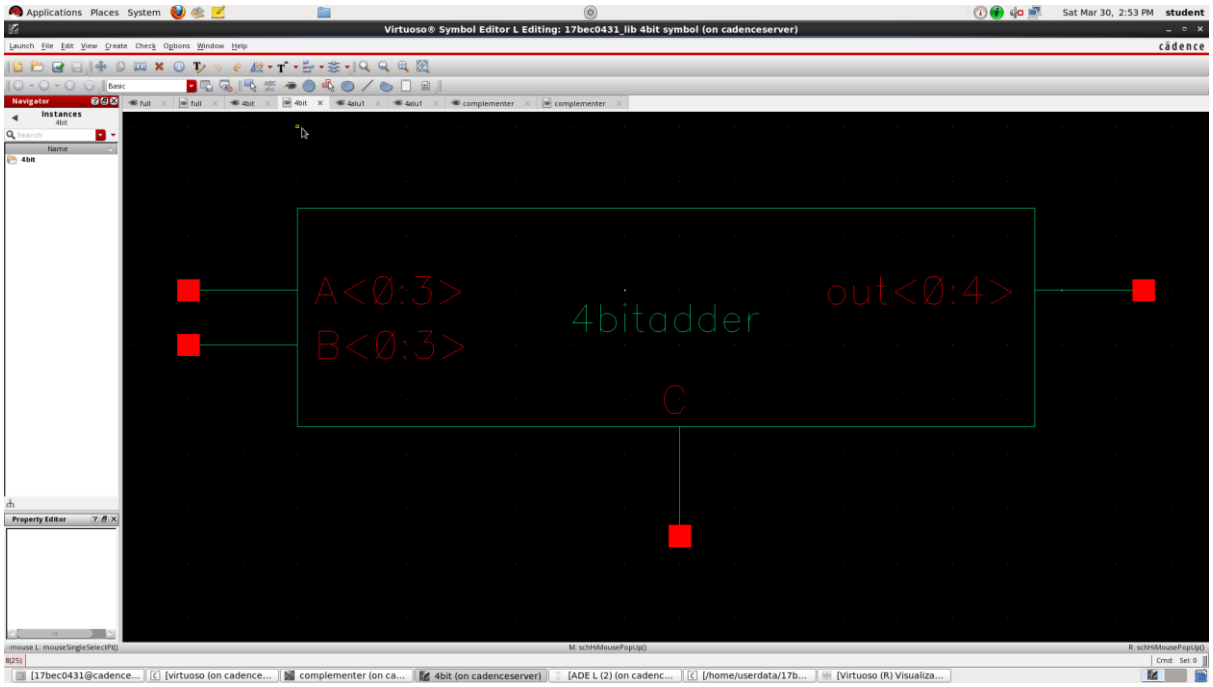
VLSI SYSTEM DESIGN **NAME:SIDDHANT AGARWAL**

REG NO:17BEC0431

4 BIT ADDER



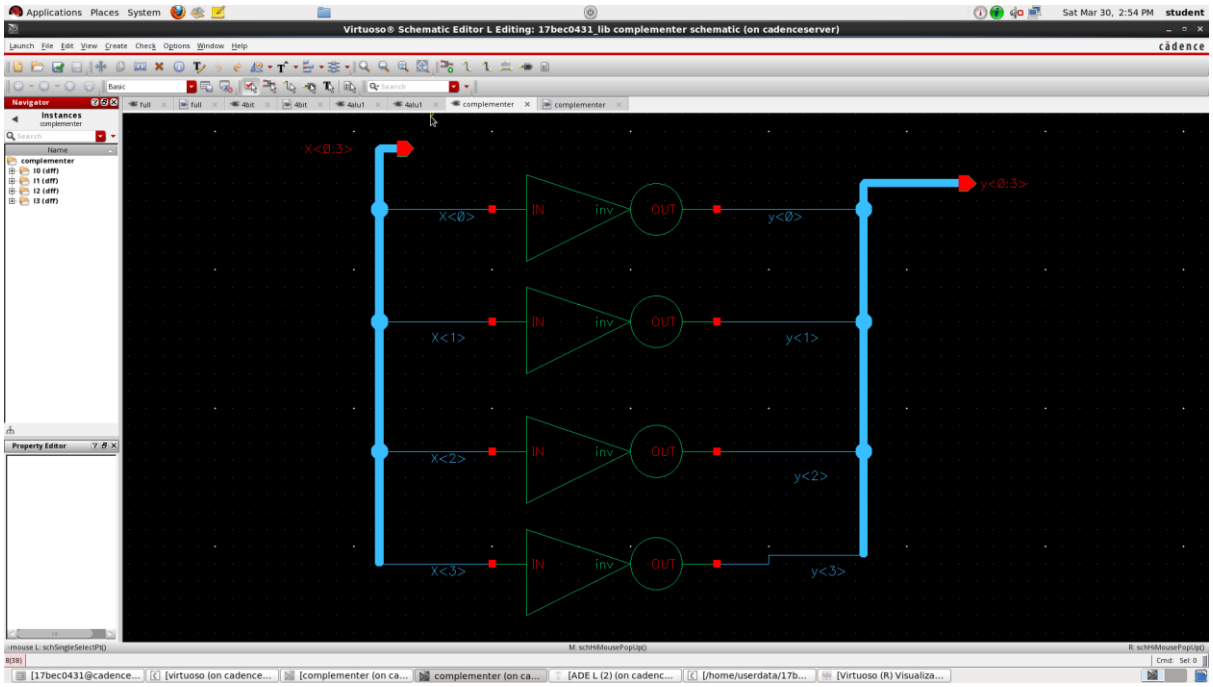
4 BIT ADDER SYMBOL



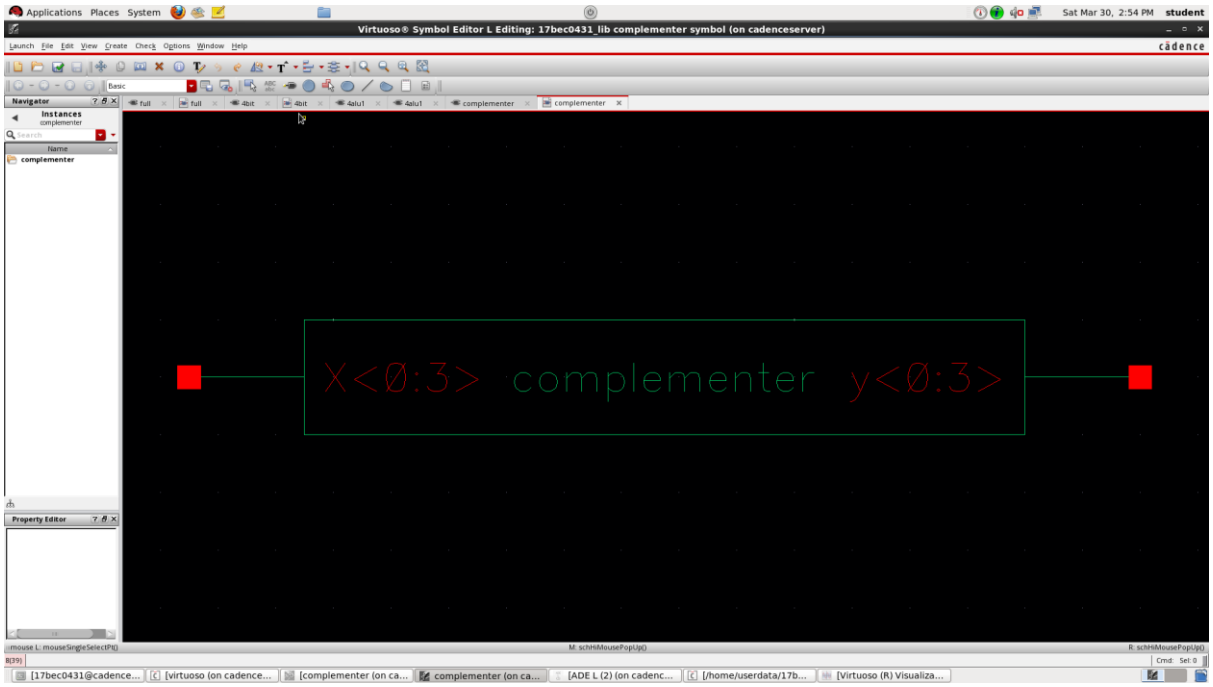
VLSI SYSTEM DESIGN **NAME:SIDDHANT AGARWAL**

REG NO:17BEC0431

COMPLEMENTER



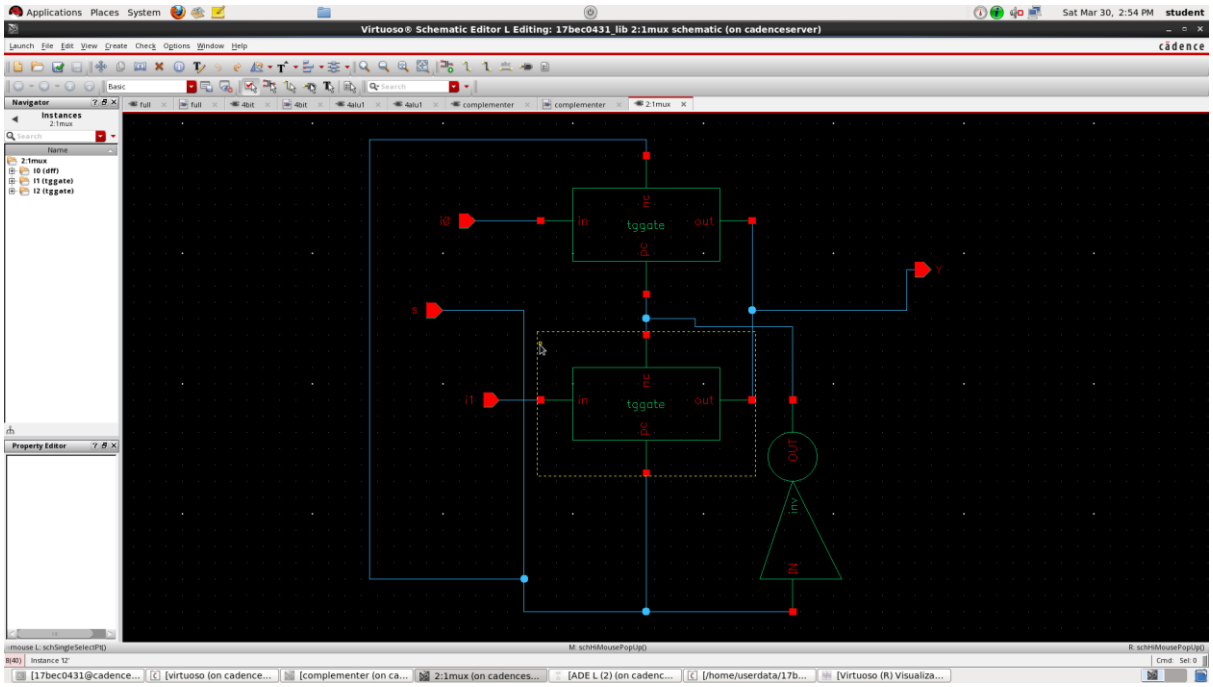
COMPLEMENTER SYMBOL



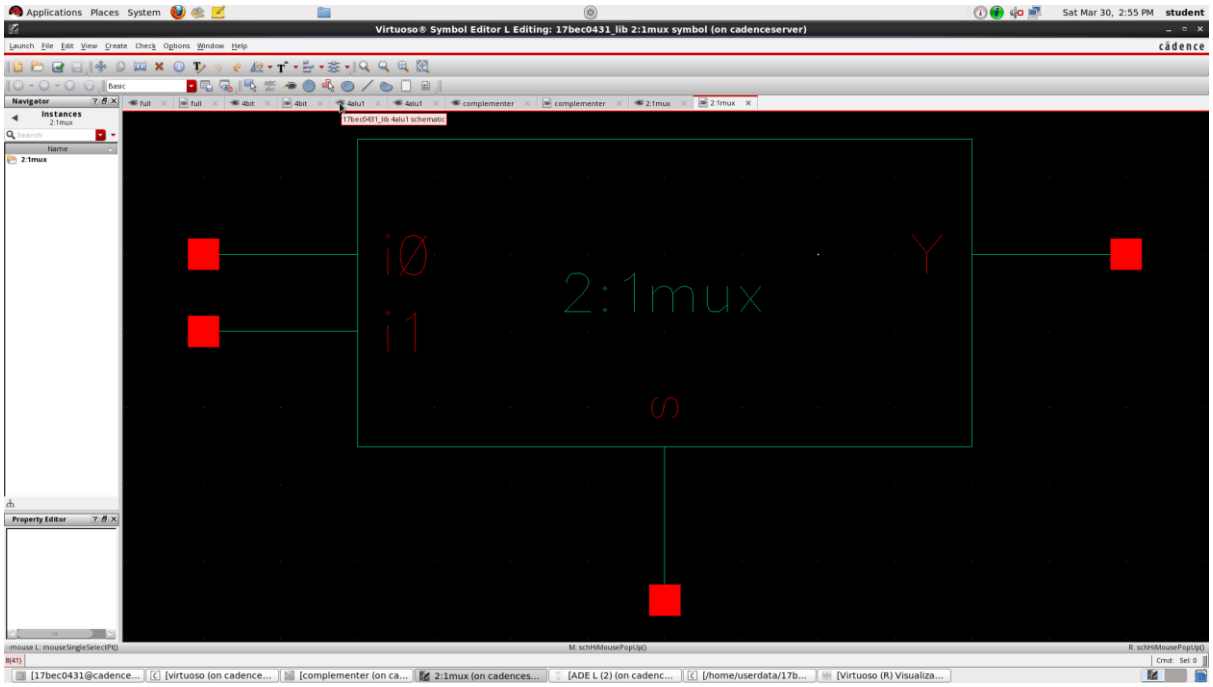
VLSI SYSTEM DESIGN

NAME:SIDDHANT AGARWAL
REG NO:17BEC0431

2X1 MUX



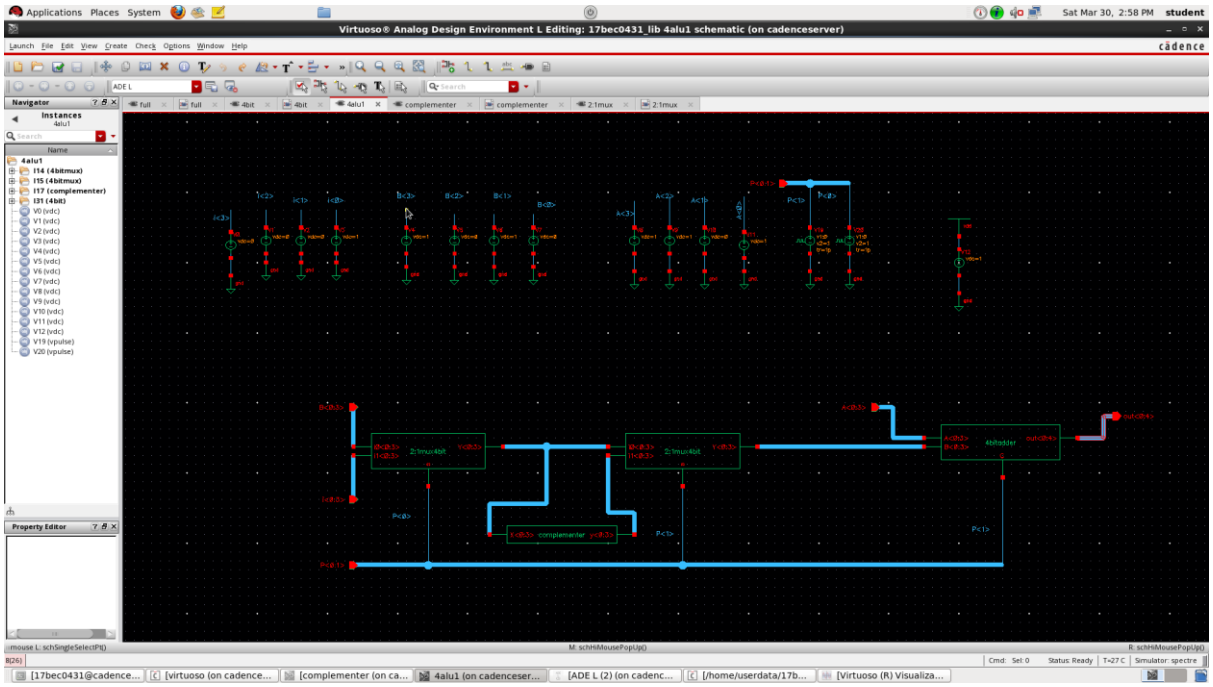
4 BIT 2X1 MUX



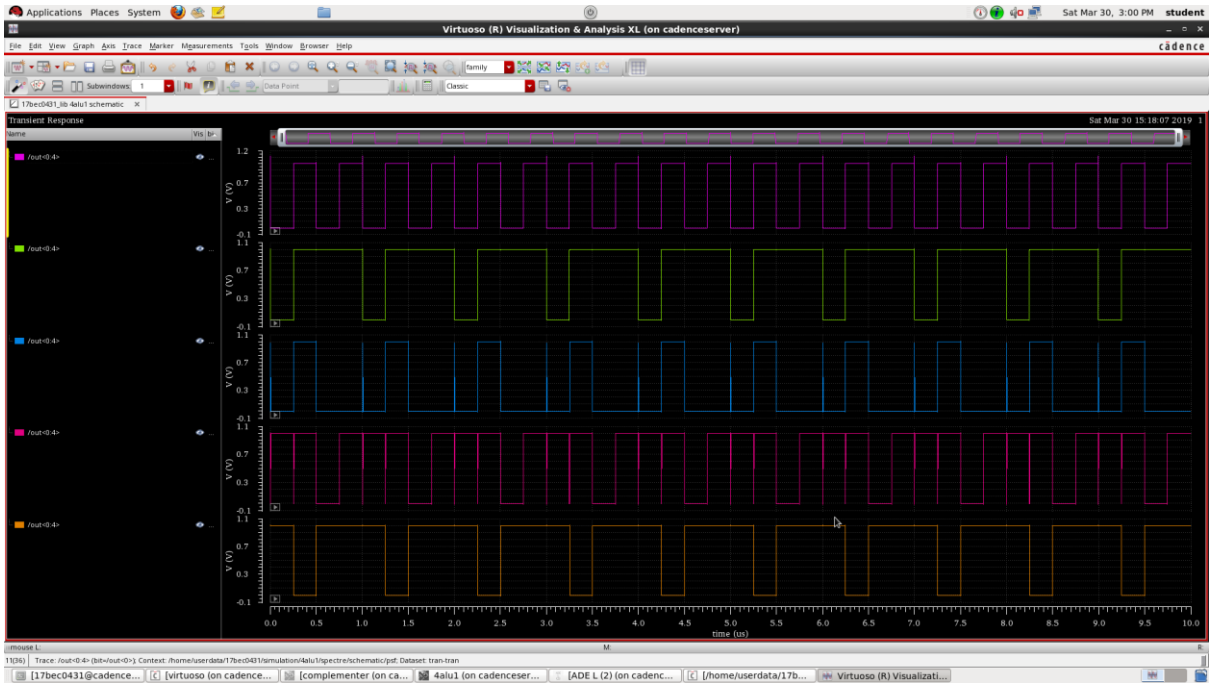
VLSI SYSTEM DESIGN

NAME:SIDDHANT AGARWAL
REG NO:17BEC0431

ALU DESIGN



OUTPUT ADEL SIMULATION



C<0:1>	OUT<0:4>
0 0	A+B
0 1	A-B
1 0	A+1
1 1	A-1

NAME:SIDDHANT AGARWAL
REG NO:17BEC0431