VLSI SYSTEM DESIGN LAB(ECE3001)

(BY PROF.JAGANNADHA NAIDU K)

TASK-1

NMOS AND PMOS V-I CHARACTERISTICS

SLOT-L23+L24

NAME:SIDDHANT AGARWAL

REGISTER NO:-17BEC0431

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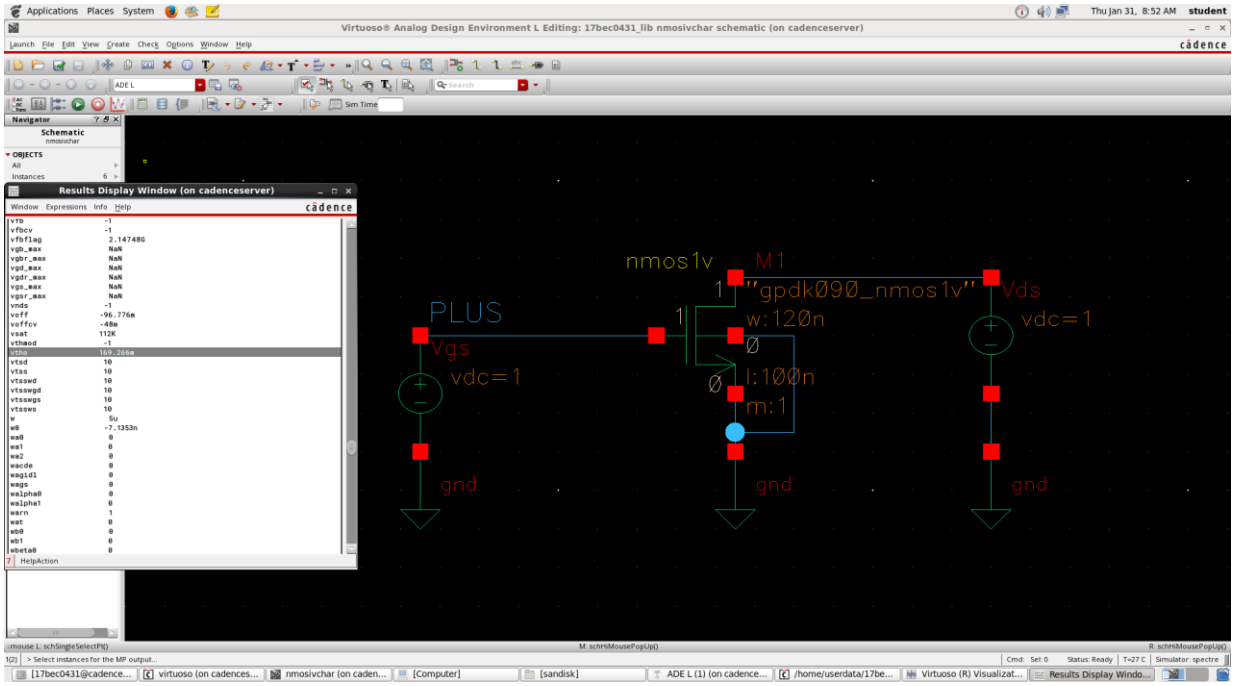
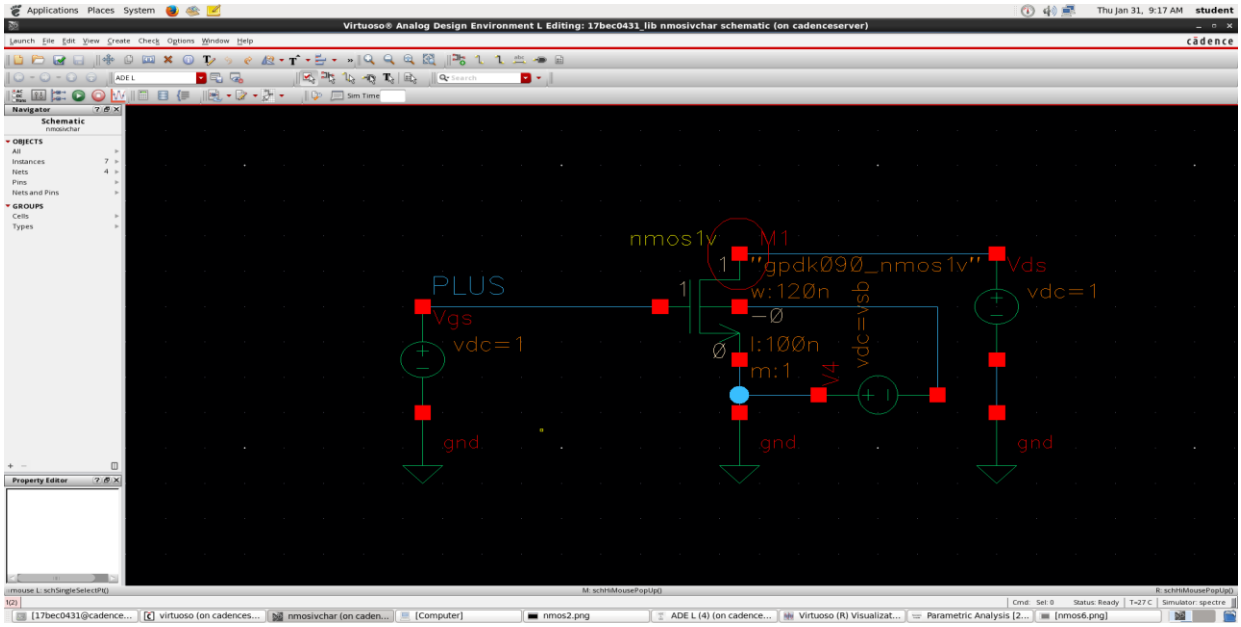
AIM:TO Plot the V-I characteristics of NMOS and PMOS transistors. Determine the region of operation for the MOSFET .Also calculate the threshhold voltage and the pinch off voltage.

CIRCUIT DESIGNS:



TRANSFER CHARACTERISTICS CIRCUIT



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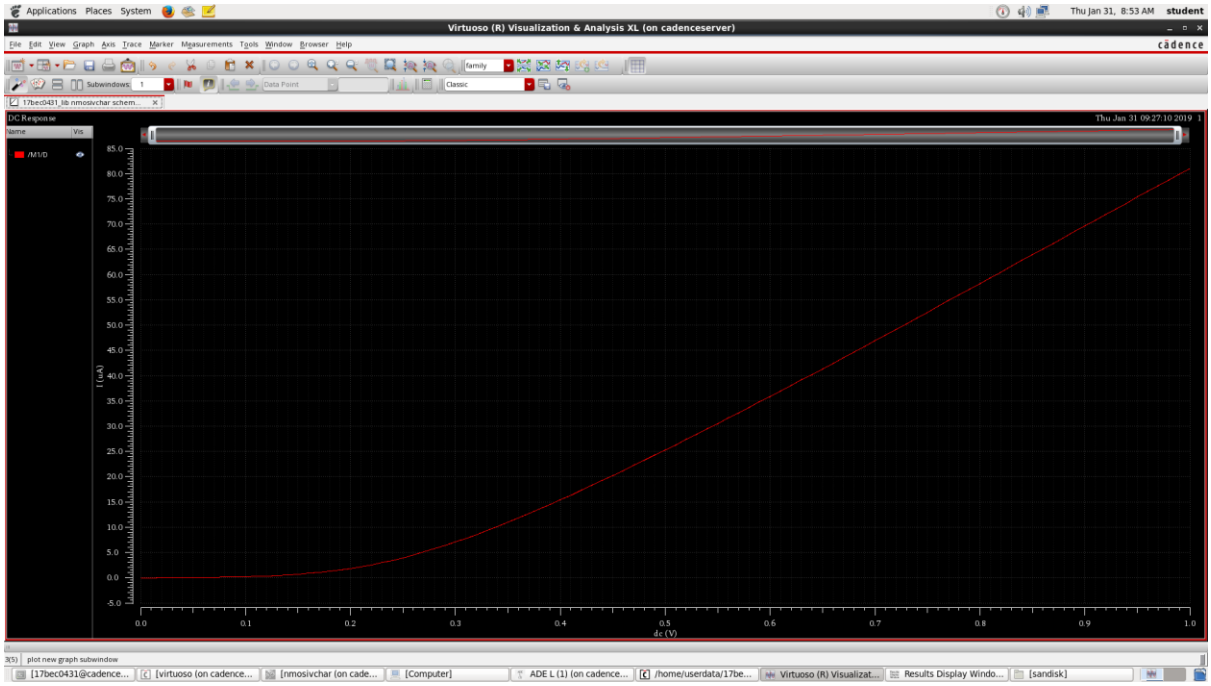
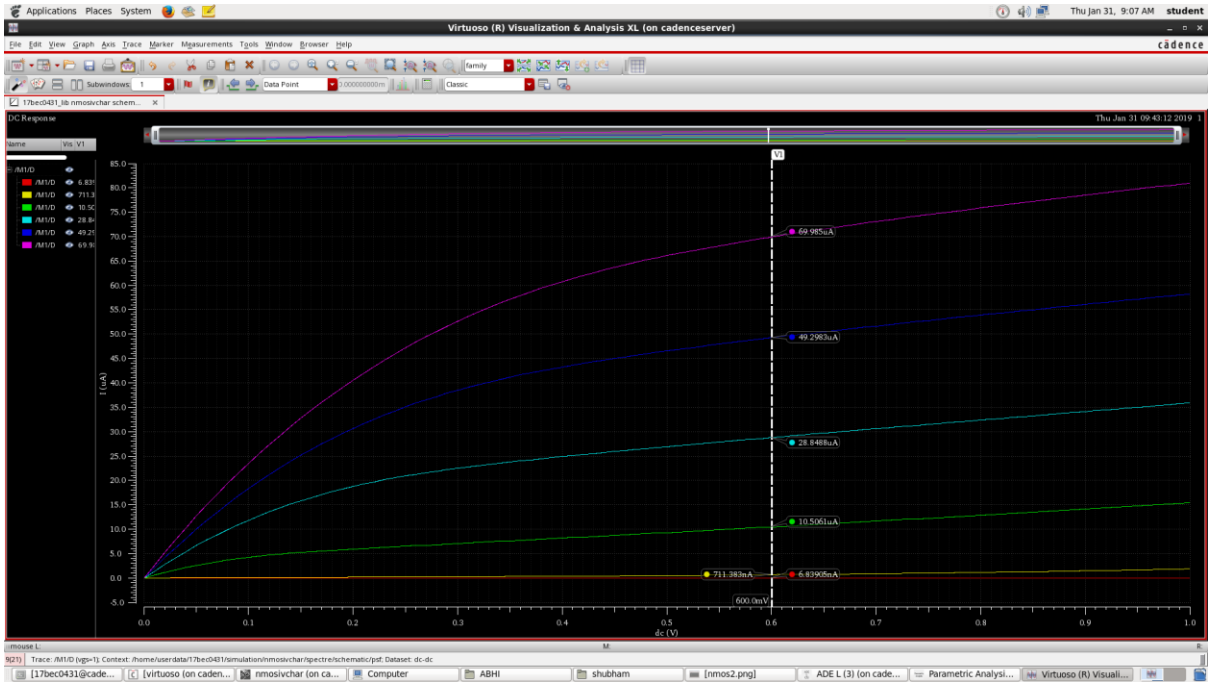
PLOTS:



OUTPUT CHARACTERSTICS



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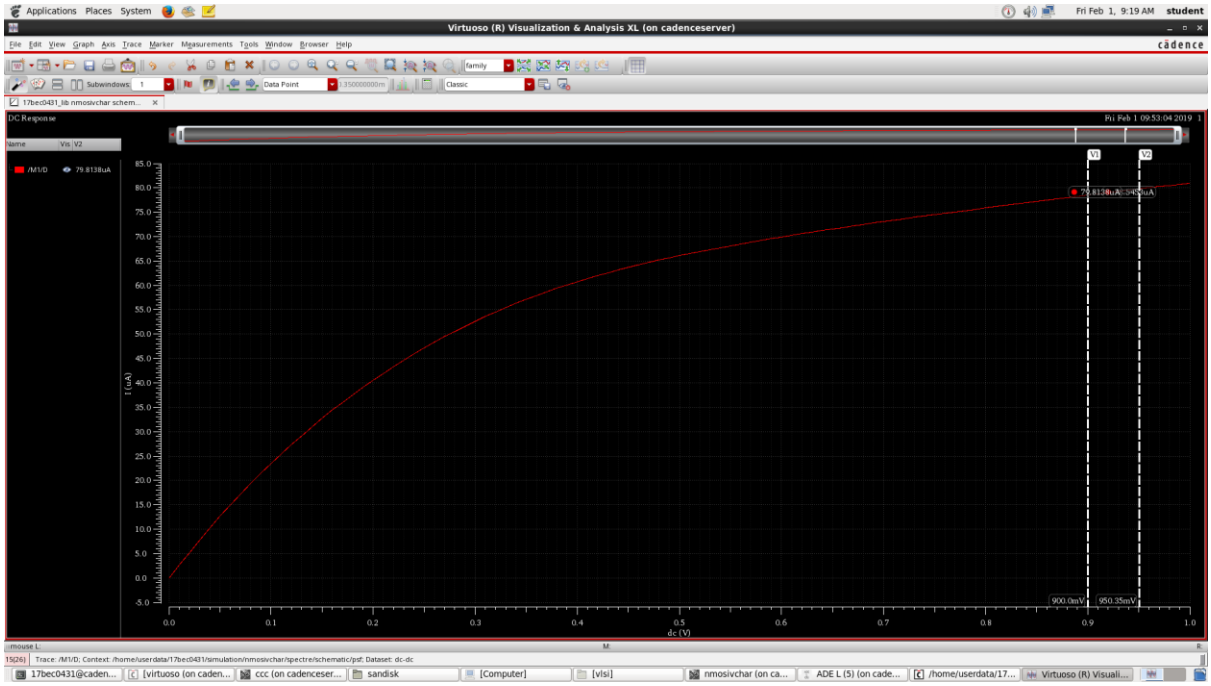
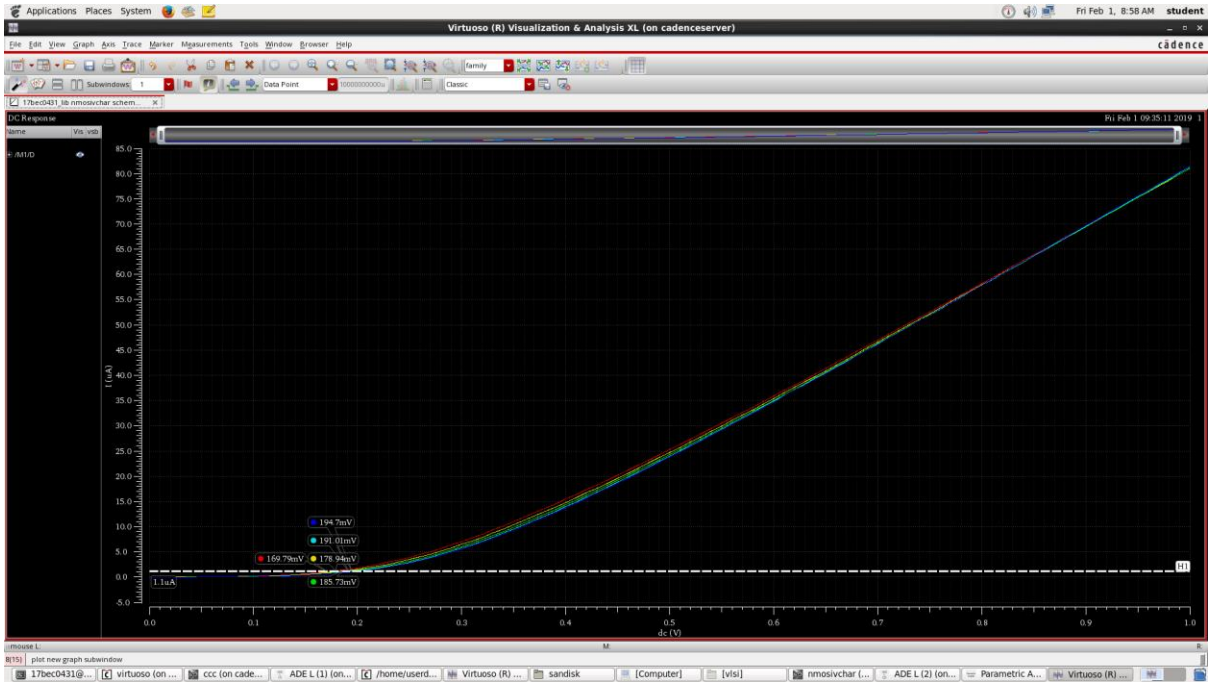
AT V_{gs}=1V OUTPUT TO CALCULATE LAMBDA



TRANSFER CHARACTERISTICS AT 1.1uA



OBSERVATION AND TABLE:

OUTPUT CHARACTERSTICS

VDS(SAT)(mV)	VGS(V)
-169.266	0
31	0.2
231	0.4
431	0.6

TRANSFER CHARACTERISTICS: At V_{gs}=1.1uA

V(t)(mV)	Vsb(V)
169.79	0
178.9	0.25
185.73	0.5
191.04	0.75
194.7	1

Calculation of (λ_n)

$$I_{ds1}=78.545uA \quad I_{ds2}=79.81uA$$

$$I_{ds1}=I_{ds}(1+\lambda_n V_{ds1})$$

$$I_{ds2}=I_{ds}(1+\lambda_n V_{ds2})$$

$$I_{ds1}/ I_{ds2}=((1+\lambda_n V_{ds1}))/ (1+\lambda_n V_{ds2})$$

We get

$$\lambda_n=0.6$$

VLSI LAB

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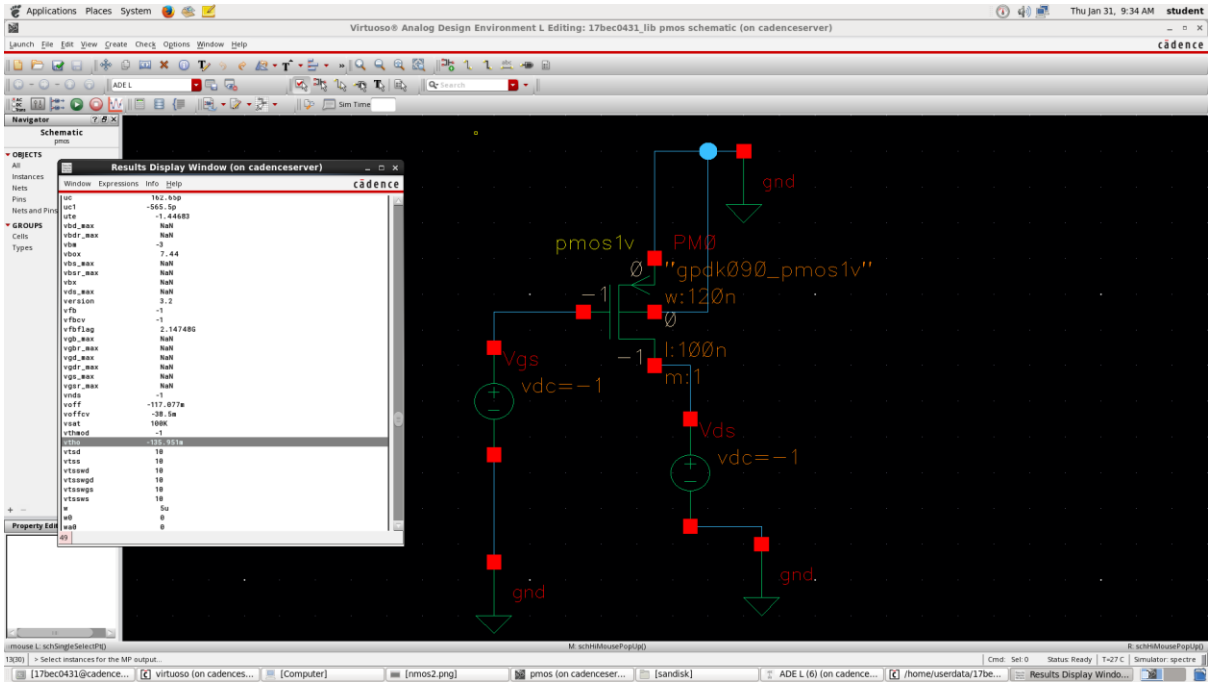
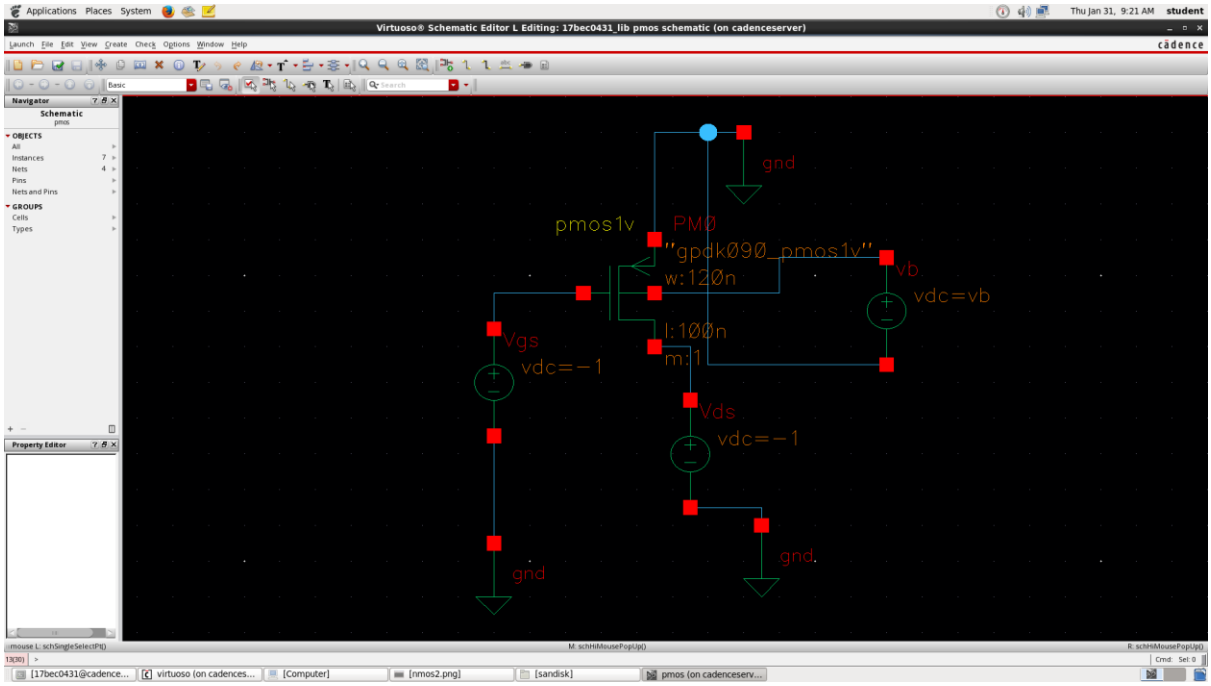
PMOS CHARACTERSTICS:

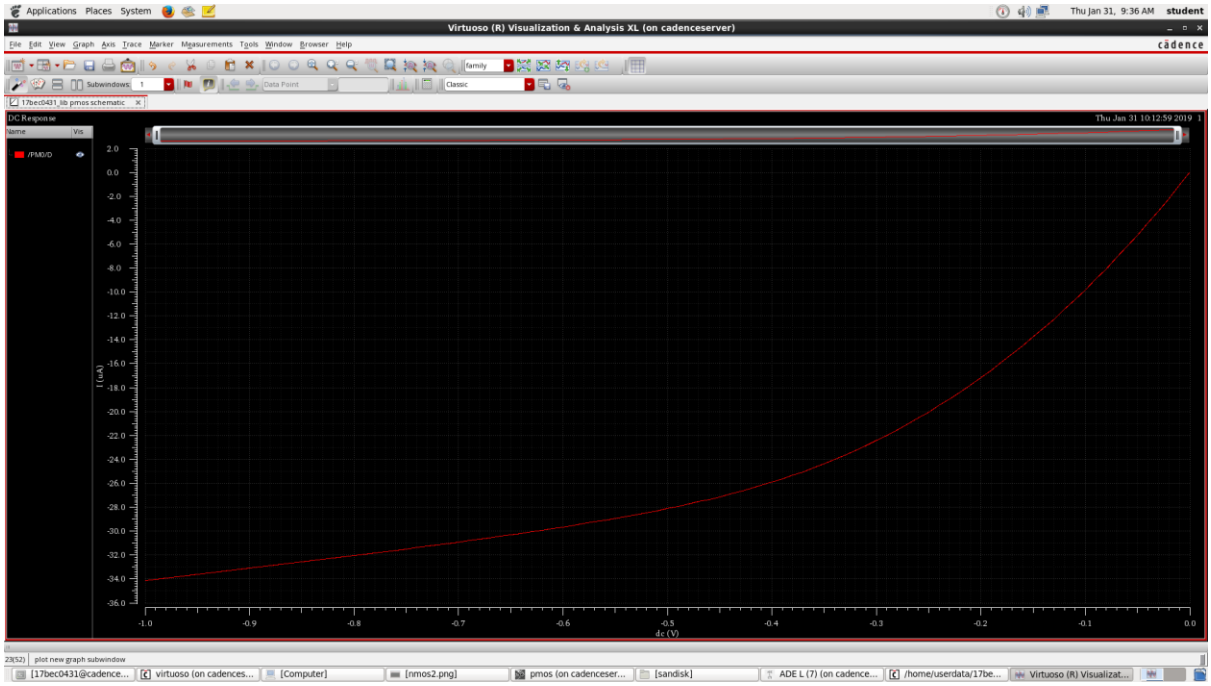
CIRCUIT DESIGNS:



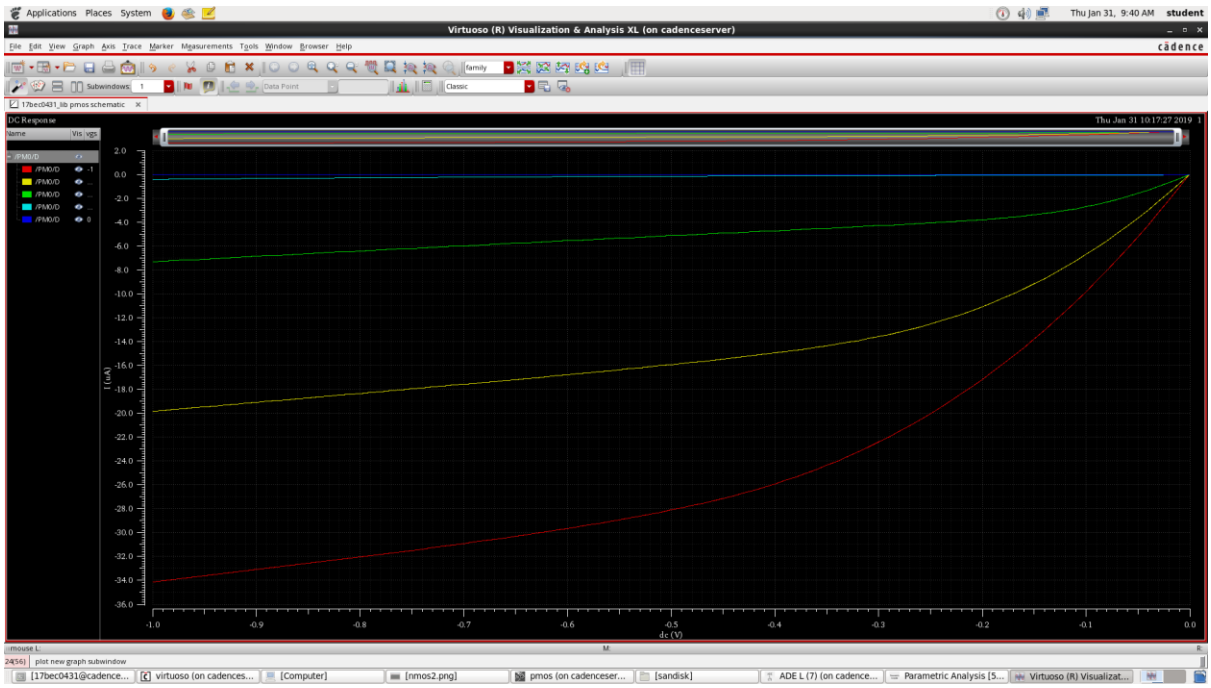
TRANFER CHARACTERISTICS CIRCUIT



PLOTS:



OUTPUT CHARACTERISTICS



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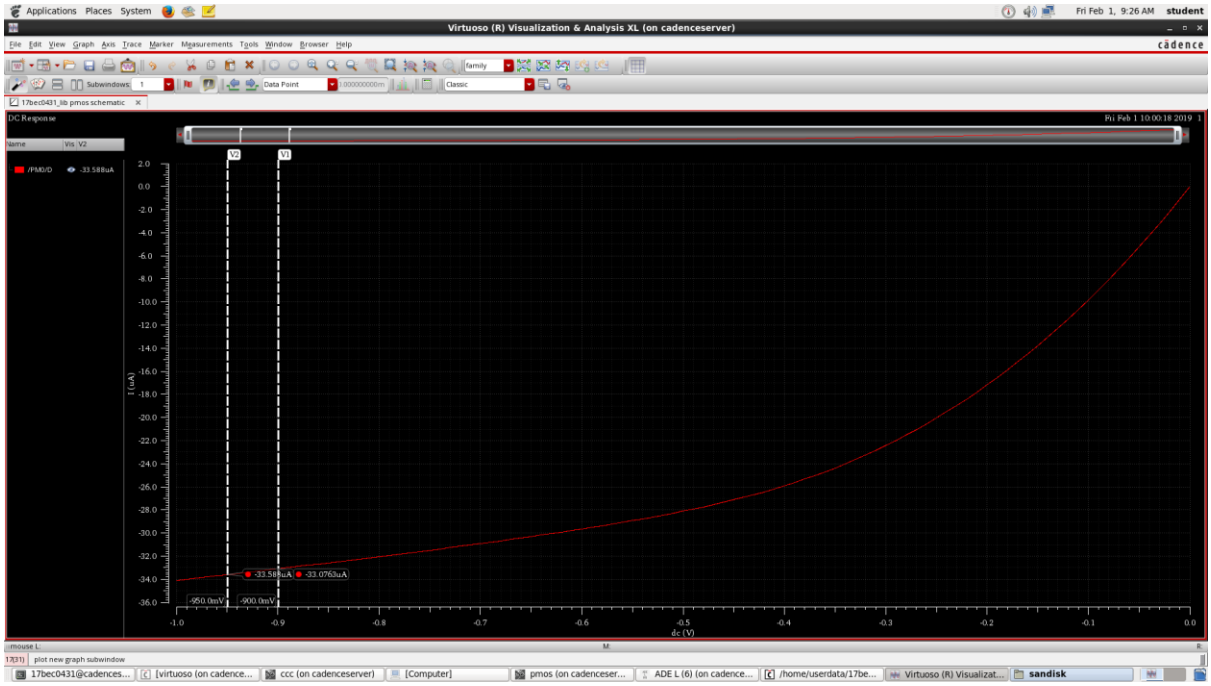
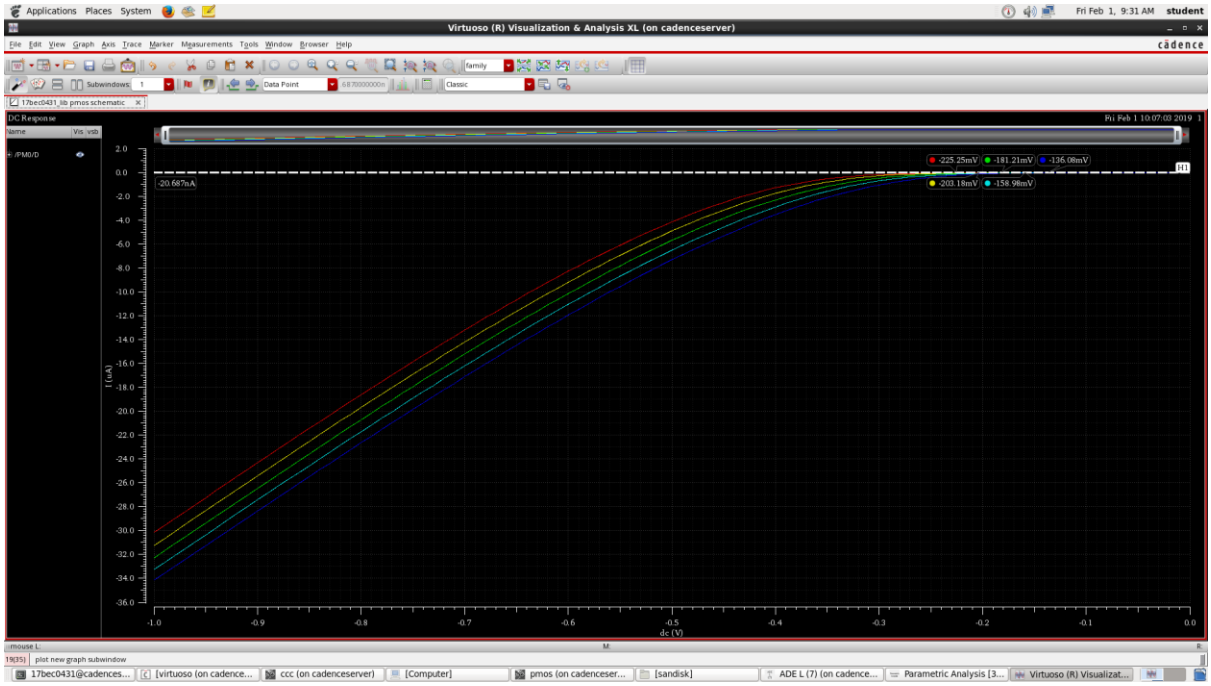
OUTUT CHARACTERISTIC AT V_{GS}=-1V TO CALCULATE LAMBDA



TRANSFER CHARACTERISTICS



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OBSERVATION AND TABLE:

OUTPUT CHARACTERSTICS

VDS(SAT)(mV)	VGS(V)
135	-0
-65	-0.2
-265	-0.4
-465	-0.6
-665	-0.8
-865	-1

TRANSFER CHARACTERSTICS:

V(t)(mV)	Vsb(V)
-136.08	0
-158.98	-0.25
-181.21	-0.5
-203.18	-0.75
-225.25	-1

Calculation of (λ_n)

I_{ds1}=-33.076uA I_{ds2}=-33.588uA

$$I_{ds1}=I_{ds}(1+\lambda_n V_{ds1})$$

$$I_{ds2}=I_{ds}(1+\lambda_n V_{ds2})$$

$$I_{ds1}/ I_{ds2}=((1+\lambda_n V_{ds1}))/ (1+\lambda_n V_{ds2})$$

We get

$$\lambda_p=0.6$$

INFERENCE

PMOS

In linear region the I_{DS} will increase linearly with increase in drain to source voltage (V_{DS}) whereas in saturation region the I_{DS} is constant and it is independent of V_{DS}.

ID, VGS, VDS, and VTH(P) are all negative for PMOS are positive for NMOS.

NMOS

ID, VGS, VDS, and VTH(P) are positive for NMOS.

V_{GS} increases, even the saturation current flowing through the device also increases.

I_{DS1} as $V_{GS2} > V_{GS1}$, I_{DS3} is greater than I_{DSS2} as $V_{GS3} > V_{GS2}$, so on

RESULT

THRESHOLD VOLTAGE

PMOS:-135.951mV

NMOS:169.266mV

PINCH-OFF VOLTAGE

NMOS: AT V_{GS}=0.6v pinch off voltage =231mV

PMOS: At V_{gs}=-1V pinch off voltage=865mV