VLSI SYSTEM DESIGN LAB(ECE3001)

(BY PROF.JAGANNADHA NAIDU K)

TASK-4

D FLIP FLOP AND FULL ADDER

SLOT-L23+L24

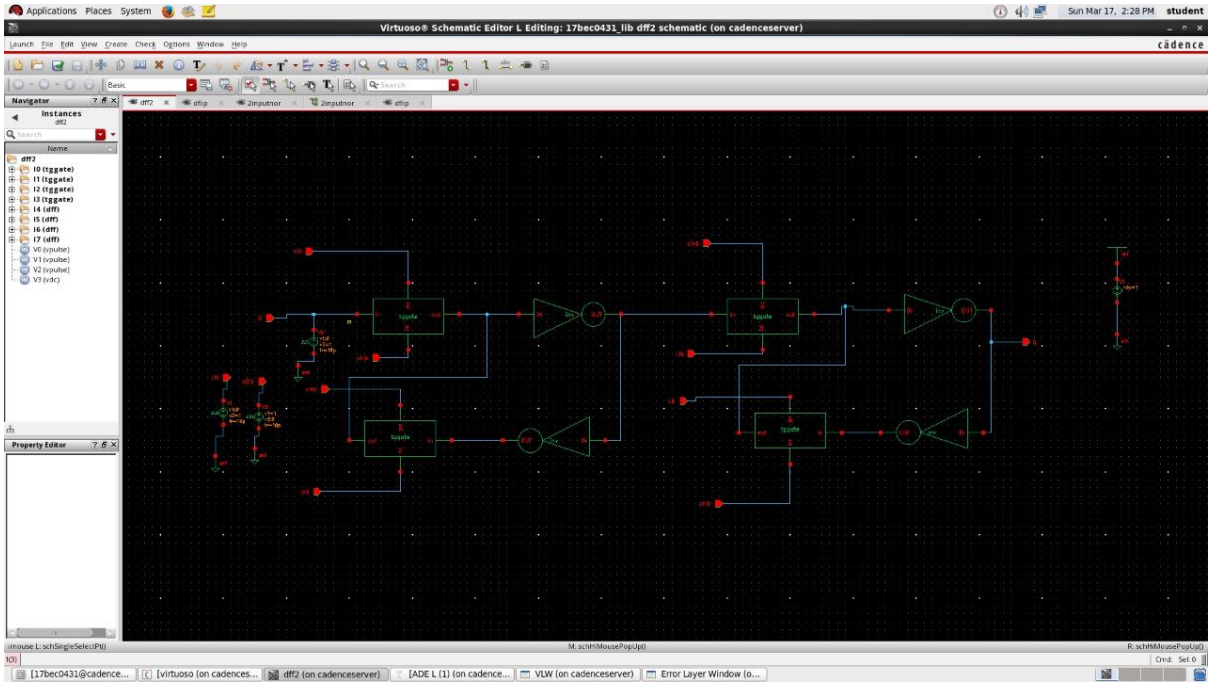
NAME:SIDDHANT AGARWAL

REGISTER NO:-17BEC0431

VLSI SYSTEM DESIGN **NAME:SIDHANT AGARWAL**
REG NO:-17BEC0431

AIM: To create CMOS dflip flop and perform transient analysis.

SCHEMATIC



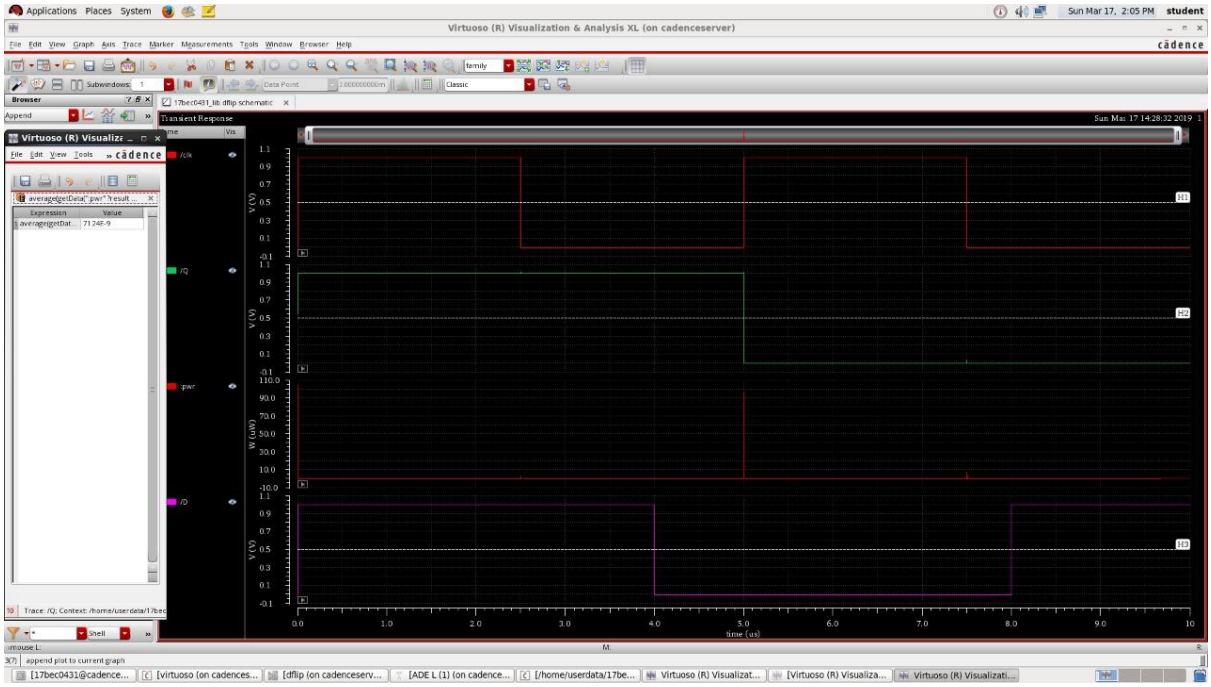
FUNCTIONALITY

VLSI SYSTEM DESIGN **NAME:SIDHANT AGARWAL**

REG NO:-17BEC0431

DELAY

POWER ANALYSIS



OBSERVATION/Result

Tpdrf=0.2us Tpdrf=0.107us

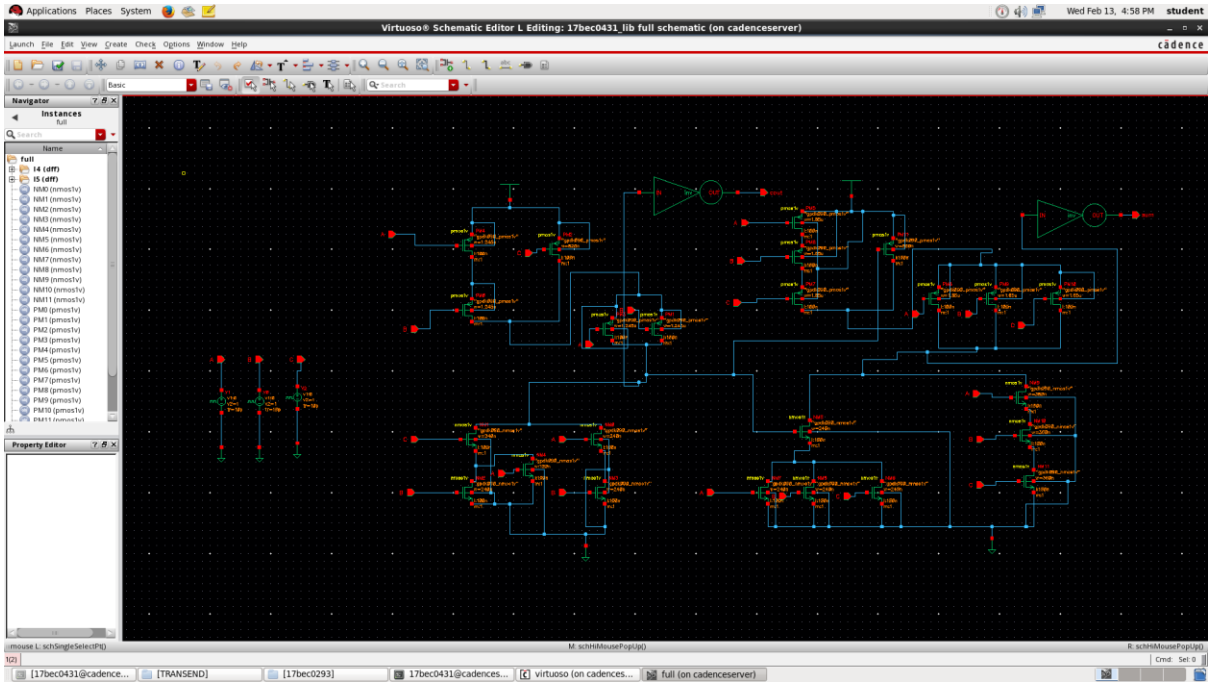
Total delay=(Tpdrf+Tdfr)/2=0.1535us

AVG POWER=71.24nW

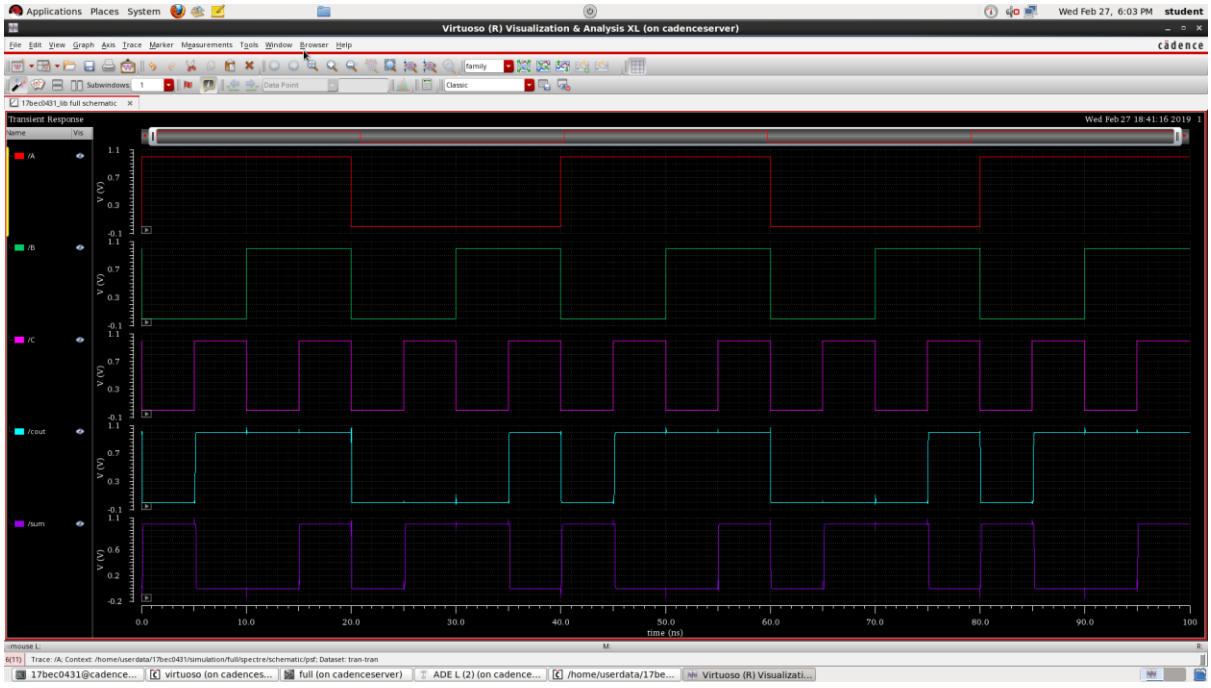
VLSI SYSTEM DESIGN **NAME:SIDHANT AGARWAL**
REG NO:-17BEC0431

AIM: To create CMOS full adder and perform transient analysis.

SCHEMATIC



FUNCTIONALITY



VLSI SYSTEM DESIGN **NAME:SIDHANT AGARWAL**
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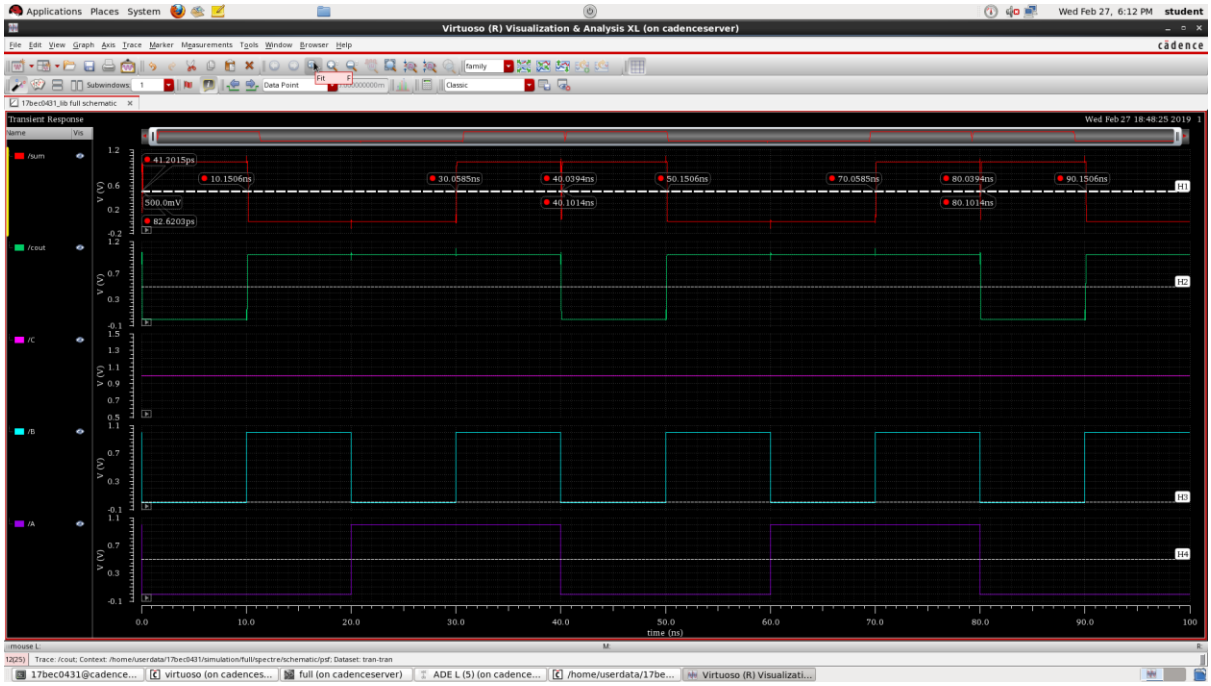
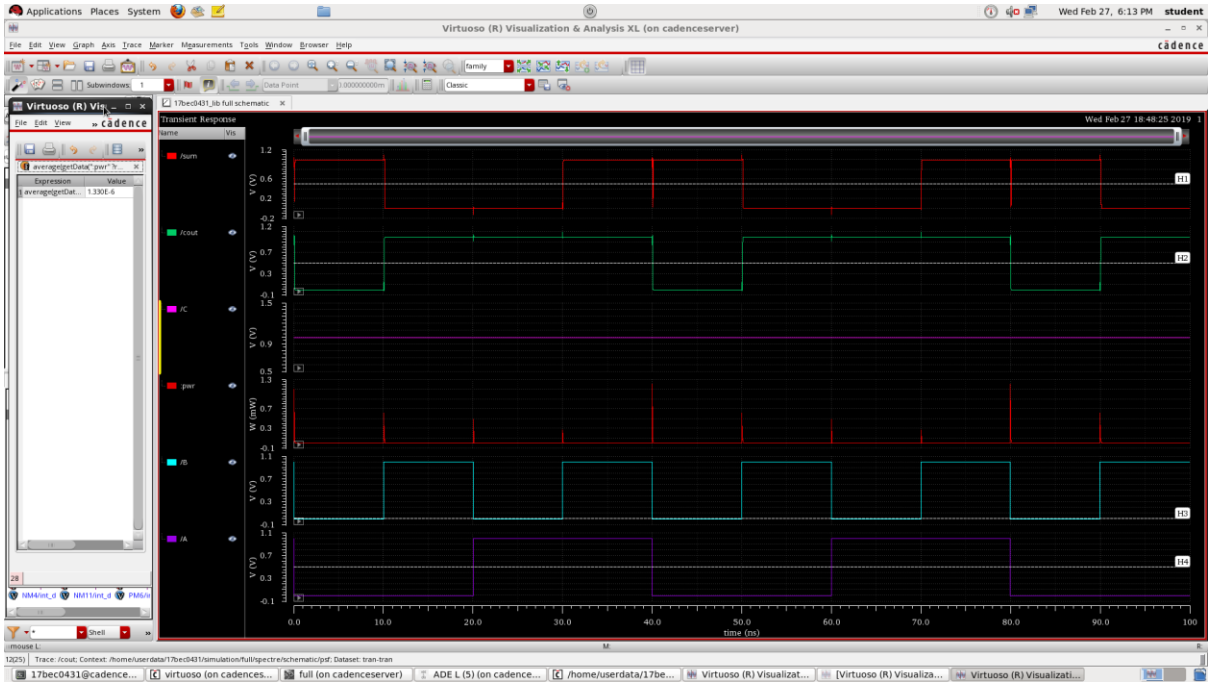
Case:111-001(ABC)



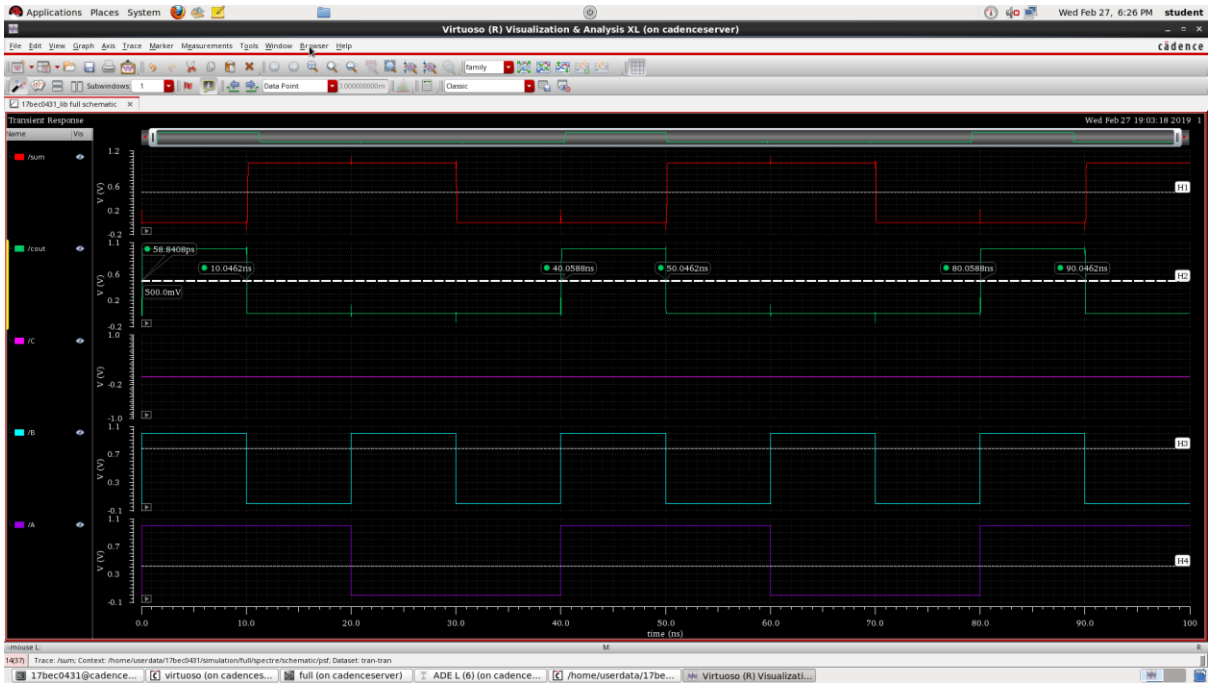
POWER



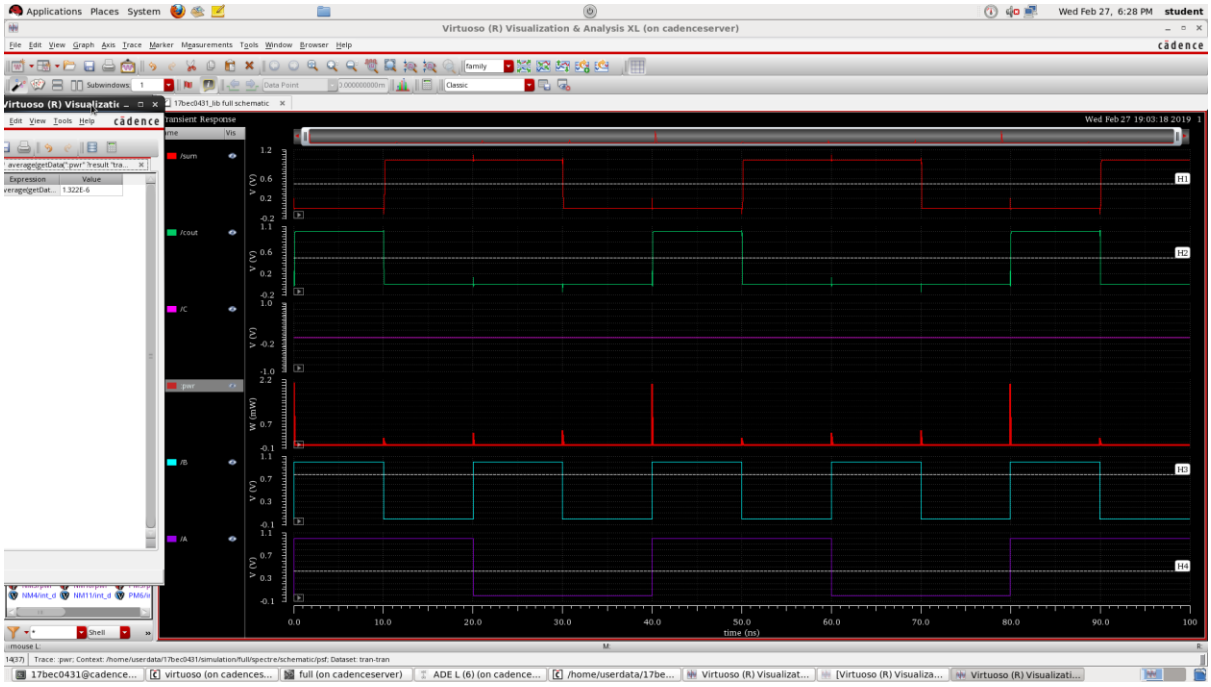
VLSI SYSTEM DESIGN **NAME:SIDHANT AGARWAL**

REG NO:-17BEC0431

CASE:000-110(ABC)



POWER



OBSERVATION/RESULT

PROPAGATION DELAY(SUM)

INPUT PATHS	DELAY	POWER(AVG)(microwatt)
111-001(ABC)	82ps	1.33
000-110(ABC)	79ps	1.322

PROPAGATION DELAY(CARRY)

INPUT PATHS	DELAY	POWER(AVG)(microwatt)
111-001(ABC)	10.09ns	1.33
000-110(ABC)	10.05ns	1.322