VLSI SYSTEM DESIGN LAB(ECE3001)

(BY PROF.JAGANNADHA NAIDU K)

TASK-3

SLOT-L23+L24

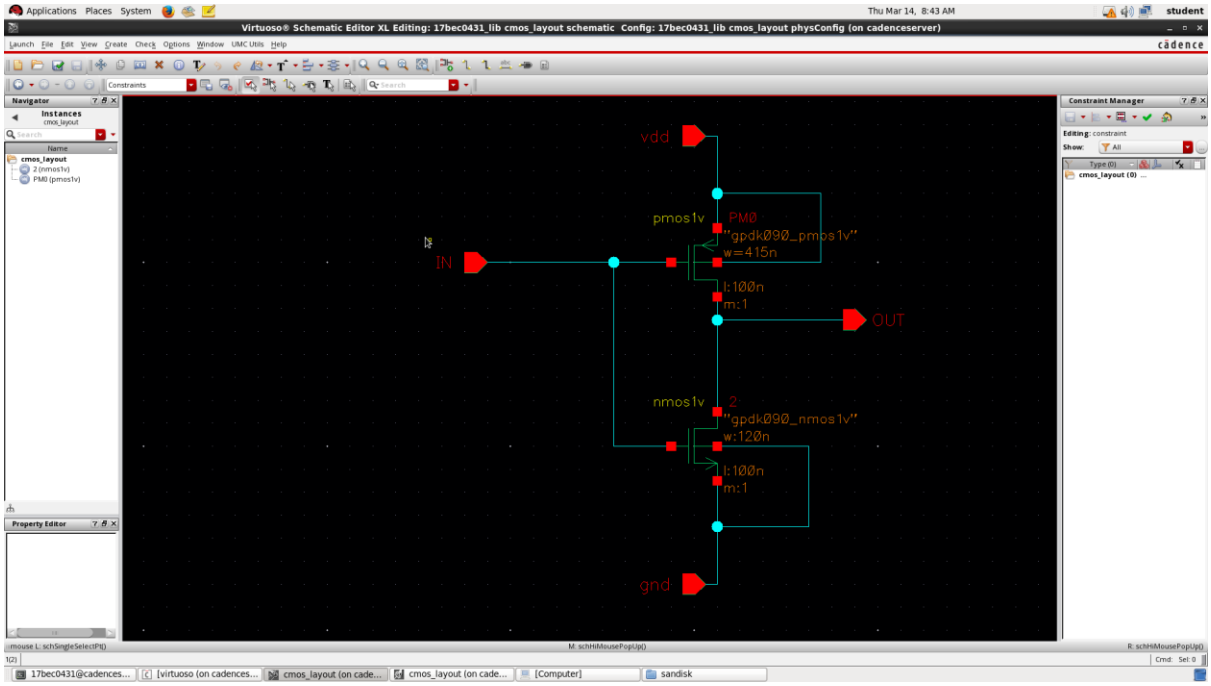
NAME:SIDDHANT AGARWAL

REGISTER NO:-17BEC0431

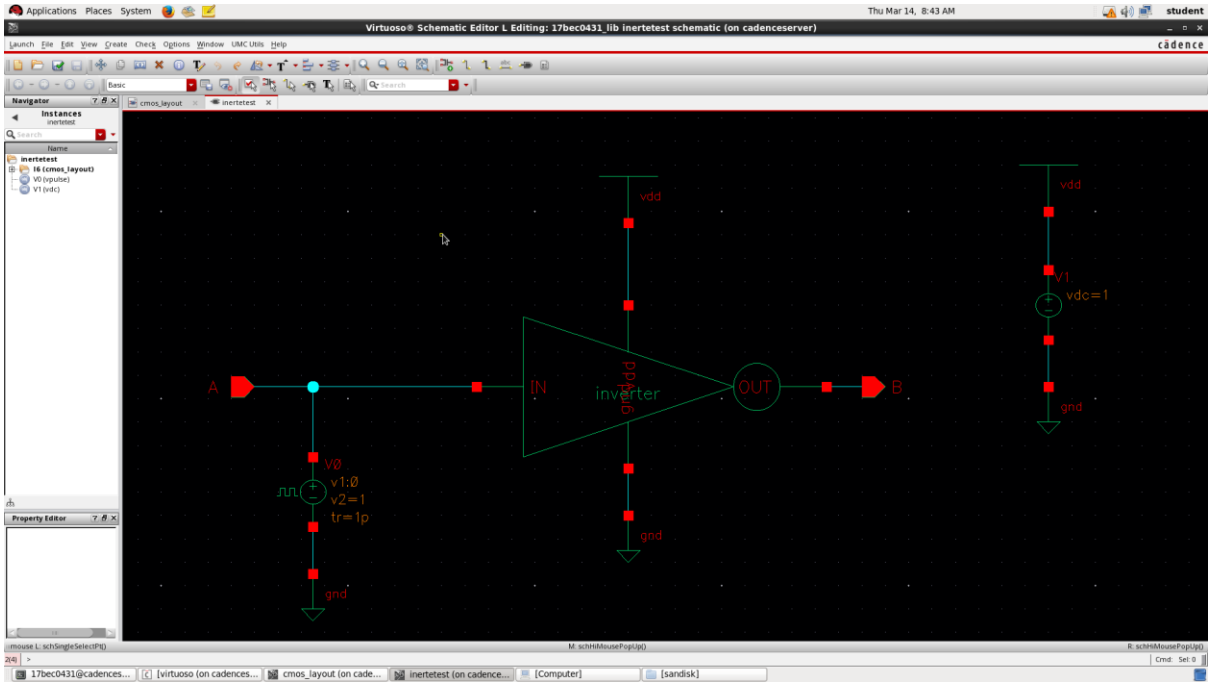
VLSI SYSTEM DESIGN **NAME:SIDDHANT AGARWAL**
REG NO:-17BEC0431

AIM:TO use cadence virtuoso to make CMOS inverter layout and transient analysis.

SCHEMATIC :-



SYMBOL LAYOUT TEST



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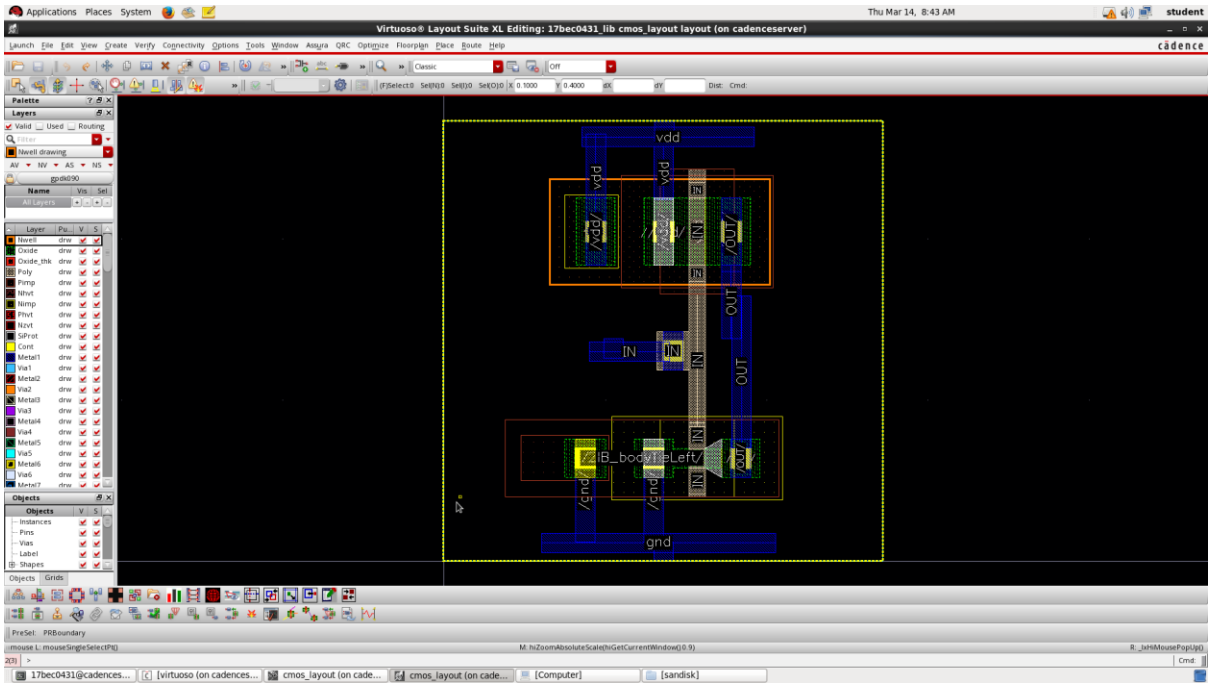
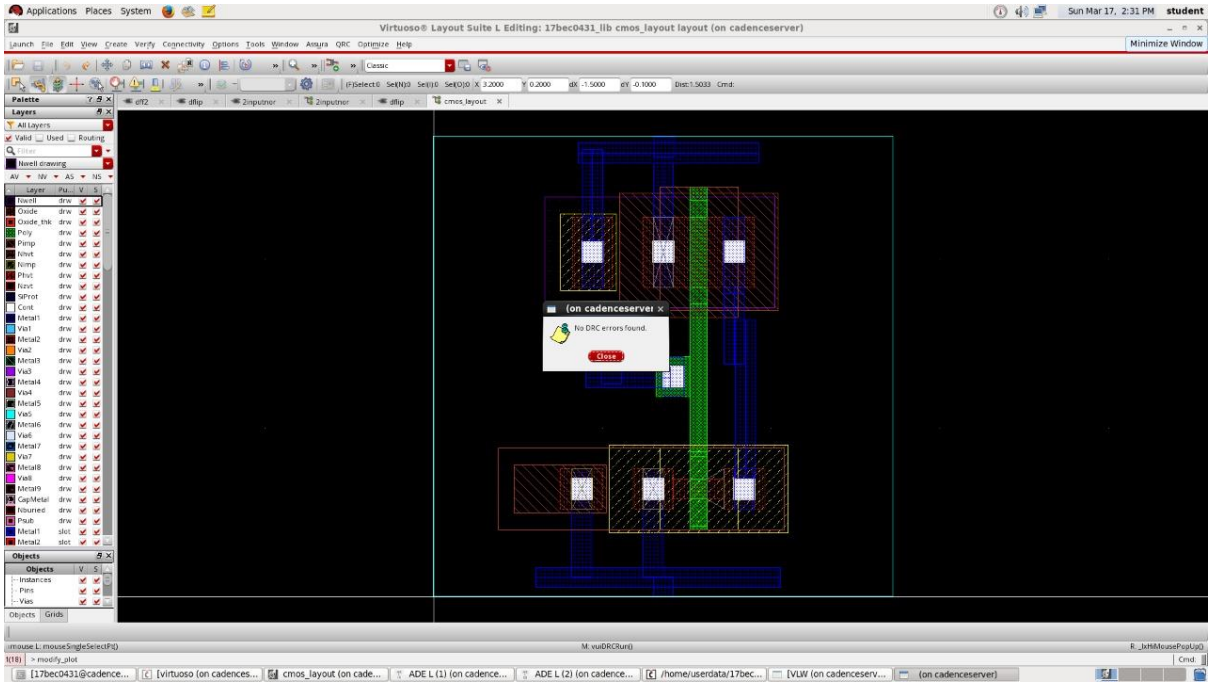
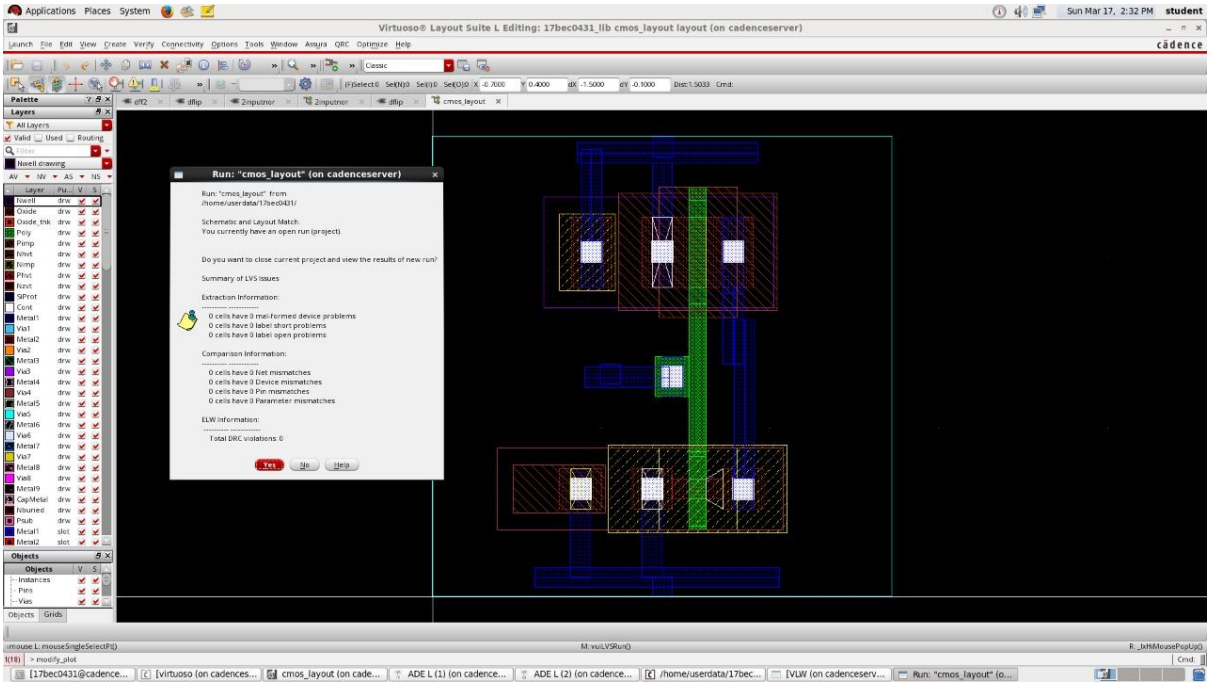
Inverter LAYOUT



OUTPUT VERIFICATION

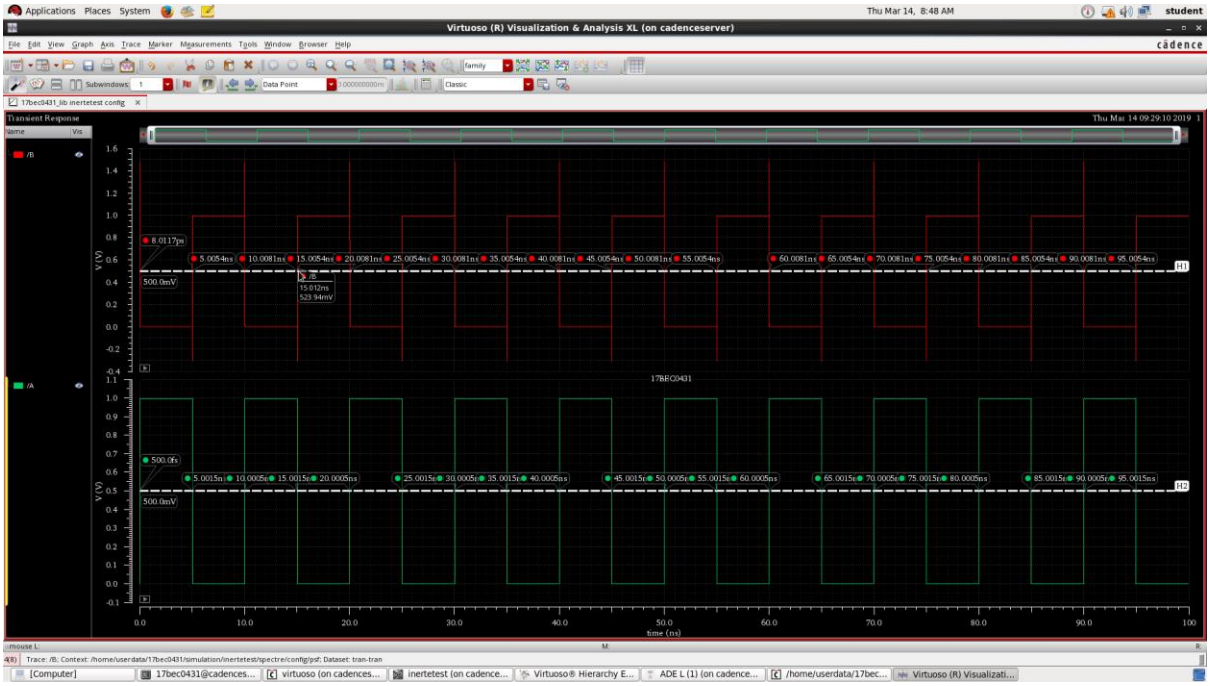


LVS RUN



GRAPHICAL OBSERVATION

FOR SCHEMATIC



VLSI SYSTEM DESIGN

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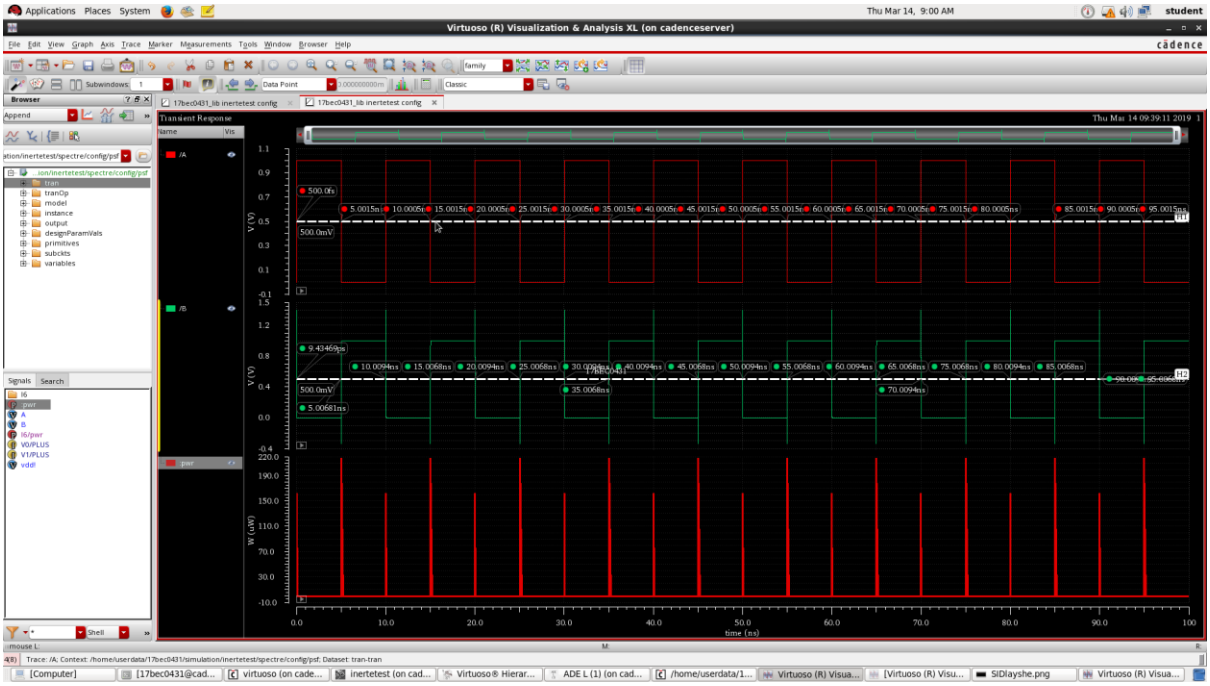
SCHEMATIC POWER ANALYSIS

FOR AVEXTRACTED

AV EXTRACTED POWER ANALYSIS



OBSERVATION

Delay calculation(schematic):-

Tphl=3.1x10^{-12}s

T_{plh}=3.9x10^{-12}s

Delay=(tplh+tphl)/2 =3.5ps

Delay calculation(avextracted)

Tphl=8.9x10^{-12}s

T_{plh}=5.3x10^{-12}s

Delay=(tplh+tphl)/2 =7.1ps

POWER:-

At Schematic:- 138.6nW

At avextracted:-169.3nW

RESULT

At Schematic:-

Delay=(tplh+tphl)/2 =3.5ps

POWER:- 138.6Nw

At avextracted:-

Delay=(tplh+tphl)/2 =7.1ps

POWER:- 169.3nW