Siddhant Singh

+1 (217) 979-1310 | Redmond, WA | siddhant@siddhantsingh.org | linkedin.com/in/siddhantsingh-/ | siddhantsingh.org

WORK EXPERIENCE

Data I/O Corporation

Device Support Engineer *2023 – Present*

- Developed embedded programming solutions for a range of Integrated Circuits including CPLDs, NAND, SPI Flash, I2C devices, microcontrollers, etc. for high-throughput manufacturing systems.
- Partnered with Leading Semiconductor firms [Micron, Kioxia, Samsung, etc.] to extend pre-release test coverage of NAND flash memory, enabling early bug detection and improved compliance.
- Engineered and deployed a JTAG-based In-System Programming solution, achieving an ***8x*** reduction in programming time for CPLDs.
- Enhanced the eMMC-UniPro host engine on FPGA to align with the latest MIPI specifications, enabling support for higher data rates and improved reliability.
- Integrated new support for UFS 4.0/4.1 devices, addressing emerging requirements in automotive and mobile supply chains.
- Leading a cross-functional vulnerability investigation, identifying system-level inefficiencies to improve production yield and strengthen customer retention and acquisition.

SPEA S.p.A.

Test Engineering Intern for Semiconductor Power Devices *2022*

- Assessed AC/DC/Phase Isolation testability of high-power IGBT and MOSFET modules for industrial clients like Silan Microelectronics.
- Created optimized test programs to reduce cycle time while ensuring robust coverage and eliminating post-deployment field failures.
- Built a datalog parser for automated reporting, saving 10hrs/week in engineering effort and improving test transparency for customers.

PROJECTS

ASIC Design, RTL-to-GDSII *2024*

- Executed the full RTL-to-GDSII flow on SkyWater 130nm to implement a custom 2D matrix convolution accelerator for image processing.
- Leveraged BaseJump STL to design and verify ASIC logic and I/O interfaces, reducing lead time and accelerating development cycles.
- Performed STA, PPA, DRC, LVS, and PEX across corners and modes to ensure a clean, signoff-ready layout with zero functional defects.

Superscalar Out of Order RV32IM Processor *2023*

- Designed and verified a superscalar RV32IM out-of-order processor with Tomasulo's algorithm in SystemVerilog on Quartus from scratch.
- Improved latency by ***60%*** using parameterized set-associative caches, arbitration logic, and stream-buffer-based instruction prefetching.
- Integrated a dynamic branch predictor achieving ***~89.39%*** accuracy on branch-intensive workloads.
- Built a parallel, software-driven verification model to detect bugs in memory subsystems and processor logic under varied scenarios.
- Reduced program latency by ***11x*** compared to a single cycle core and ***3x*** compared to a 5-stage pipelined core.

Dissecting GPU Memory Hierarchy Through Microbenchmarking *2022*

- Developed microbenchmarking CUDA kernels to reverse-engineer the memory hierarchy of the NVIDIA Turing T4 GPU architecture
- Extracted cache replacement policies and analyzed throughput, latency across various memory structures for optimized performance.
- Achieved ***4.3x*** speedup in Sparse 2D Matrix Multiplication by utilizing read-only texture memory, trading off lower memory hit rate.

Integrated Circuit Fabrication *2022*

- Fabricated 1µm-process devices including BJTs, MOSFETs, capacitors, diodes, inverters, control structures, etc. on a 4” silicon wafer.
- Performed Cleaning, Oxidation, Etching, Photolithography, Diffusion and Metal Deposition to fabricate 15 devices on a 4” wafer.
- Conducted electrical testing using a 4-point probe and LCR meter to analyze C–V and I–V characteristics of fabricated devices.

RESEARCH

University of Illinois at Urbana Champaign

Undergraduate Research Assistant – Passat Group *2022*

- Collaborated on Model & Data Specific Design of Deeply Embedded Tiny Neural Network Accelerators under Professor Rakesh Kumar.
- Improved Python scripts used to generate fully and partially unrolled 1D and 2D Convolution hardware blocks in System Verilog.
- Preliminary results showed ***~365x*** throughput and ***~172x*** energy gains over Eyeriss on tinyCNN benchmarks using custom accelerators.

SKILLS

Programming: System Verilog, Verilog, C/C++, Assembly, Python, CUDA, OpenGL, C#, YAML, TCL

Tools: Intel Quartus, Questa, Modelsim, Xilinx Vivado & Vitis, Cadence Virtuoso, Genus, Tempus & Innovus, Synopsys VCS, SIEMENS Calibre

Relevant Skills: Computer Architecture, VLSI, IC Fabrication, Digital Systems, Embedded Systems, Operating Systems, Semiconductor Devices, Clock Domain Crossing (CDC), UVM, Testbenches, SPI, I2C, eMMC, UniPro, JTAG, Protocol Analyzer, Oscilloscope

EDUCATION

Master of Science in Electrical Engineering, *Computer Architecture and Digital VLSI*

University of Washington, Seattle

Bachelor of Science in Computer Engineering

University of Illinois at Urbana – Champaign