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## FPGA Computing Systems: Background Knowledge & Introductory Materials

**Quiz Answers** 

Week 4: Abstractions

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## **Quiz Answers**



1. What is the reason behind the choice of moving from VHDL/Verilog descriptions to higher languages?

To ease designers life without loosing (too much) in performance Correct

Using higher level of abstractions is definitely a way to ease designers life, but it has also, sometimes, the drawback of loosing a bit in final performance

To be less productive

To get closer to a gate-level description

To get closer to a more "software development" flow and, by doing this to allow the designers to work with familiar languages and frameworks

Correct

To open the access to FPGA acceleration to a wider audience of developers

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