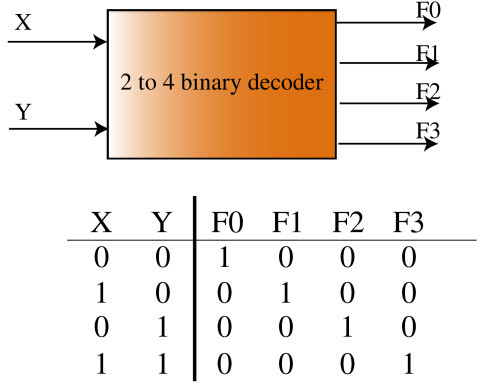
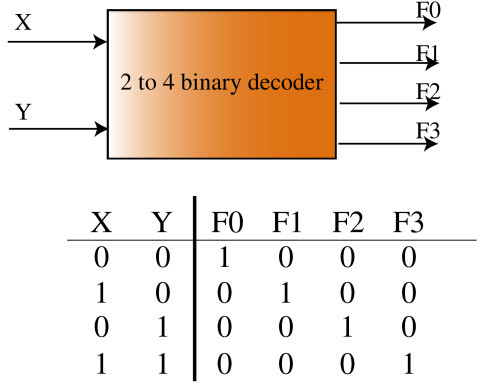
**PROBLEM : 2(2)** Write Verilog code for a 4-bit decoder.

**CIRCUIT DESIGN:**

****

**TRUTH TABLE:**

****

**VERILOG CODE:**

module decoder(A,Y);

input [1:0]A;

output reg [3:0]Y;

always@(A)

begin

case(A)

2'b00:Y= 4'b0001;

2'b01:Y = 4'b0010;

2'b10:Y = 4'b0100;

2'b11:Y = 4'b1000;

default: Y = 4'bxxxx;

endcase

end

endmodule

**TEST BENCH:**

module decodertb;

reg [1:0]a;

wire [3:0]y;

decoder uut(.Y(y),.A(a));

initial

begin

a=2'd0;

#100

a=2'd1;

#100

a=2'd2;

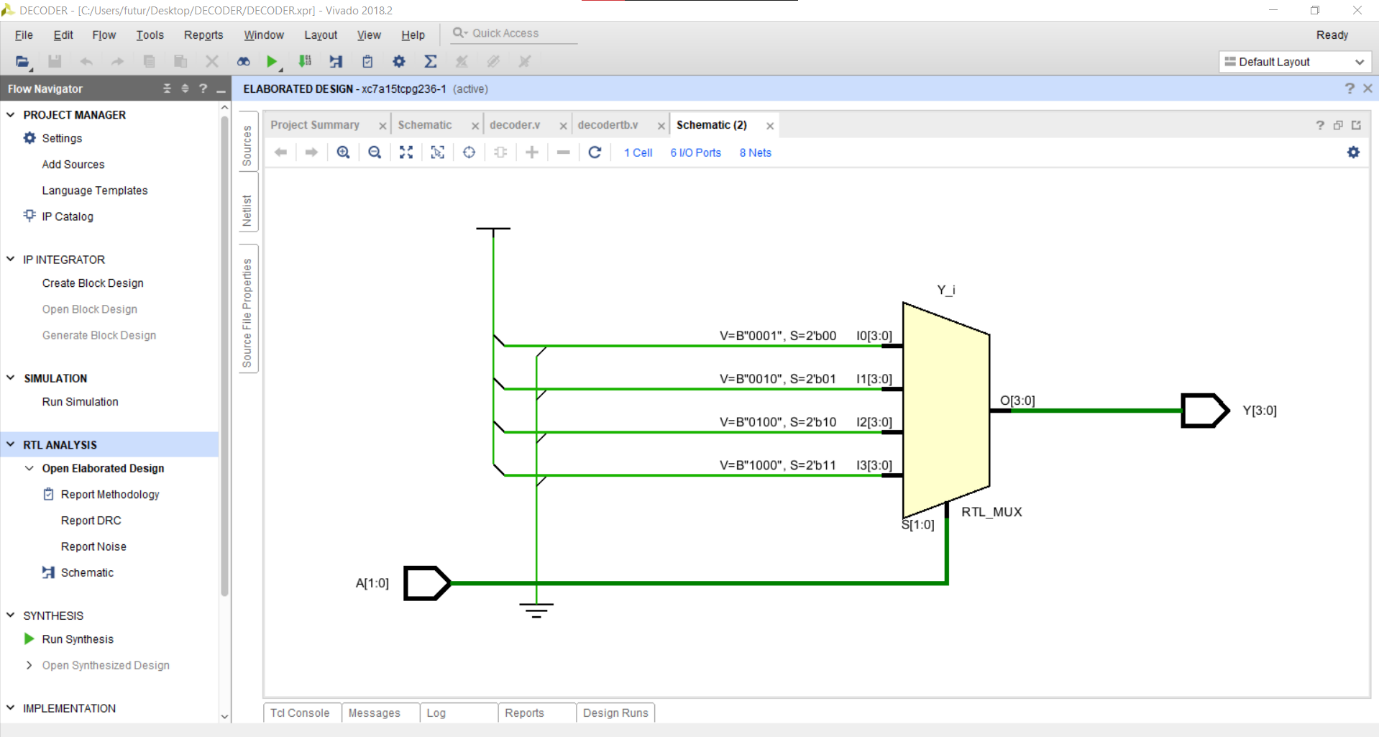
#100

a=2'd3;

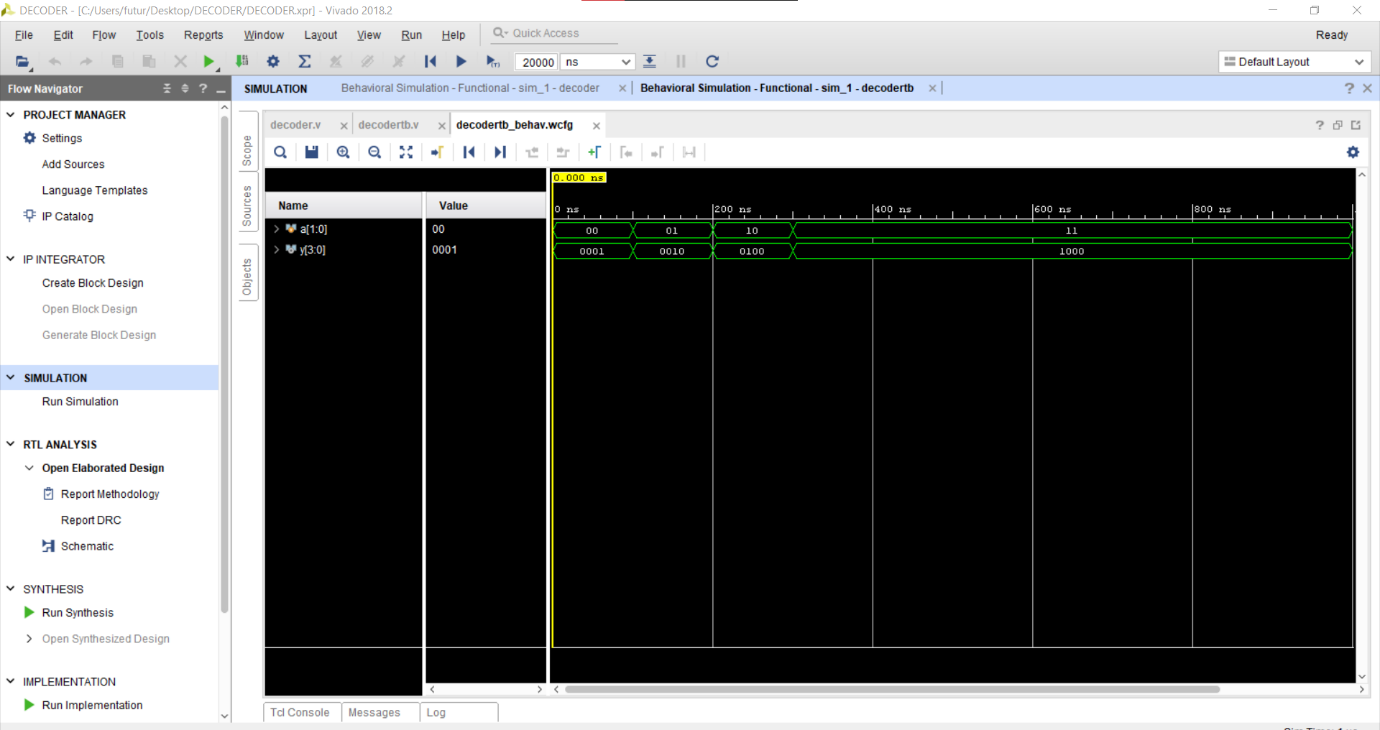
end

endmodule

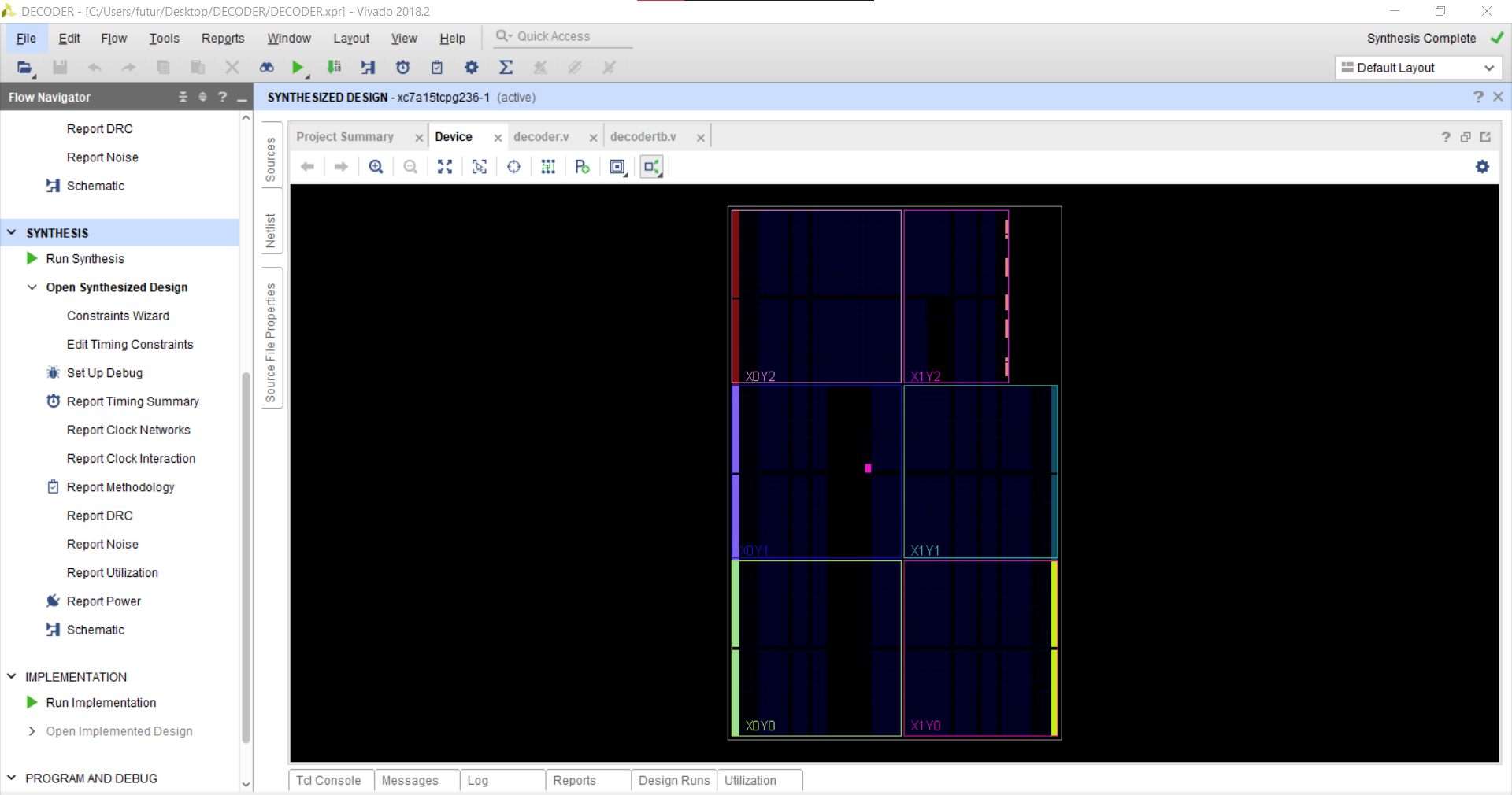
**CIRCUIT DIAGRAM:**



**OUTPUT:**



**REPORT UTILIZATION:**

****

**CONCLUSION :** We have learn 4 bit decoder using Verilog.