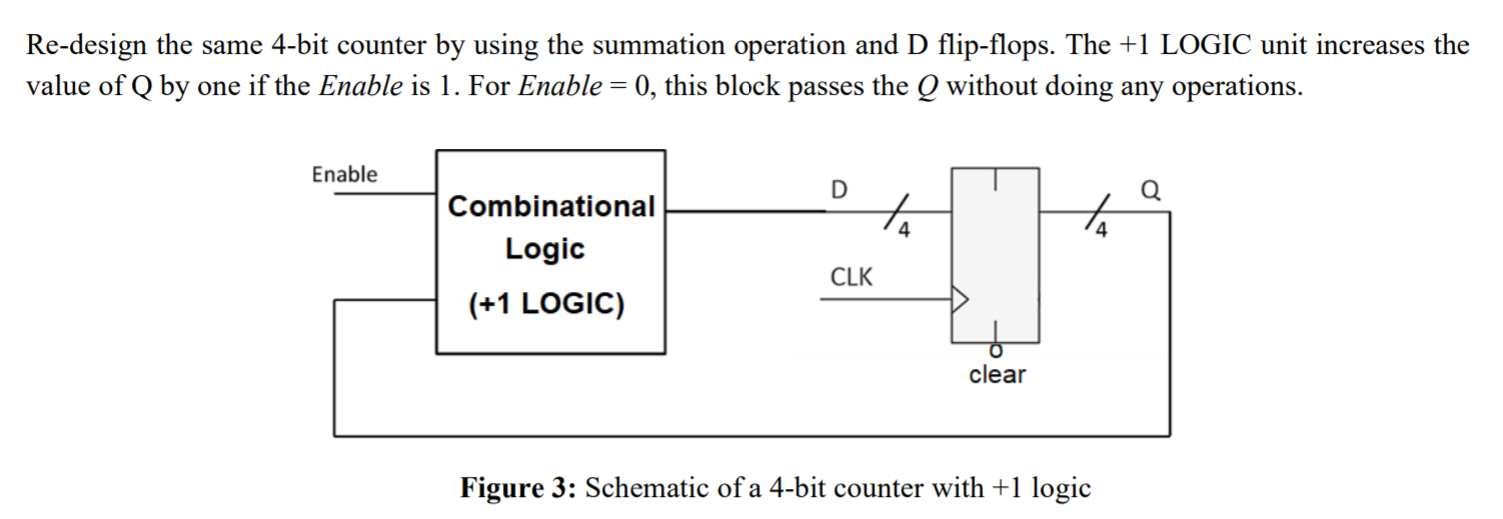
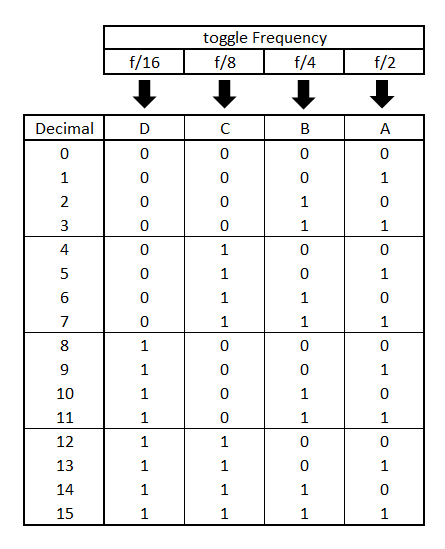
**PROBLEM** 4. Write Verilog code for down counter

**CIRCUIT DIAGRAM:**

****

**TRUTH TABLE:**

****

**VERILOG CODE:**

module DOWNCOUNTER(input rst,

input clk,

output [3:0] count

);

reg [3:0]r;

assign count=r ;

initial

begin

r=15;

end

always@(clk,rst)

begin

if (rst==1)

r<=15;

else

r= r-1;

if (r==-1)

r<=15;

end

endmodule

**TEST BENCH:**

module DOWNCOUNTER\_TB;

reg RST;

reg CLK;

wire [0:3]COUNT;

DOWNCOUNTER uut(.rst(RST),.clk(CLK),.count(COUNT));

initial

begin

CLK <=0;

end

always #10 CLK=~CLK;

initial

begin

RST=1;

#20

RST=0;

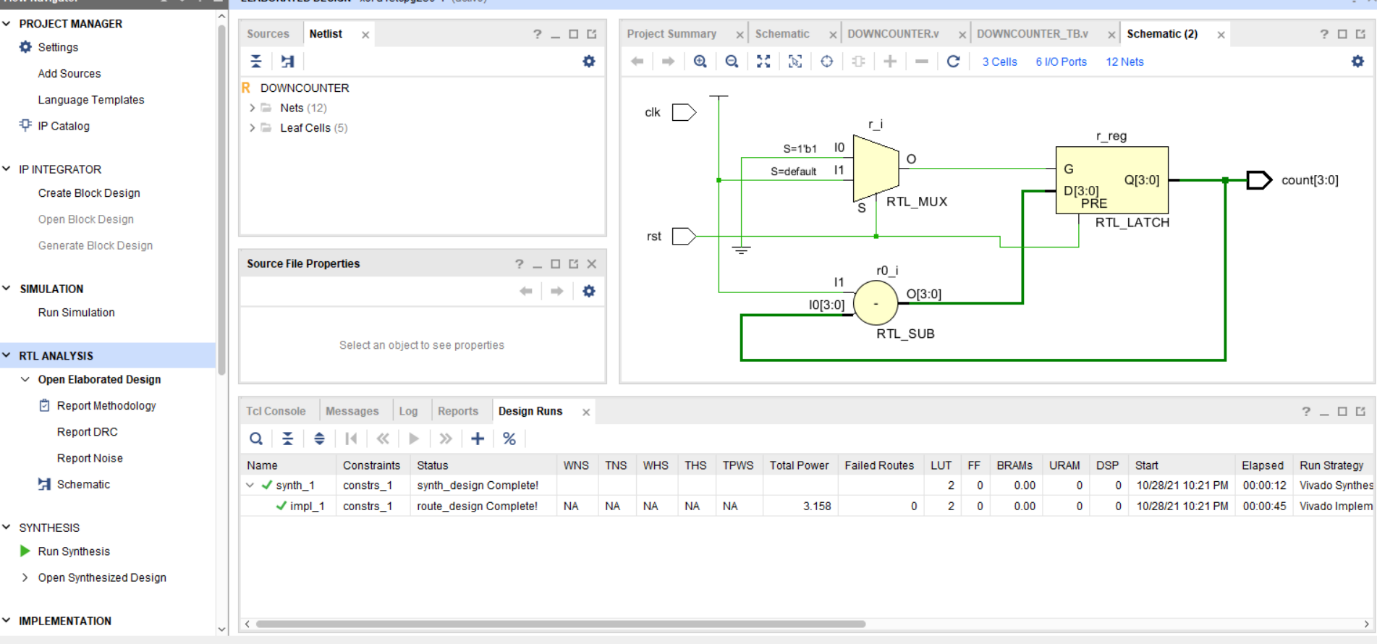
#250

RST=1;

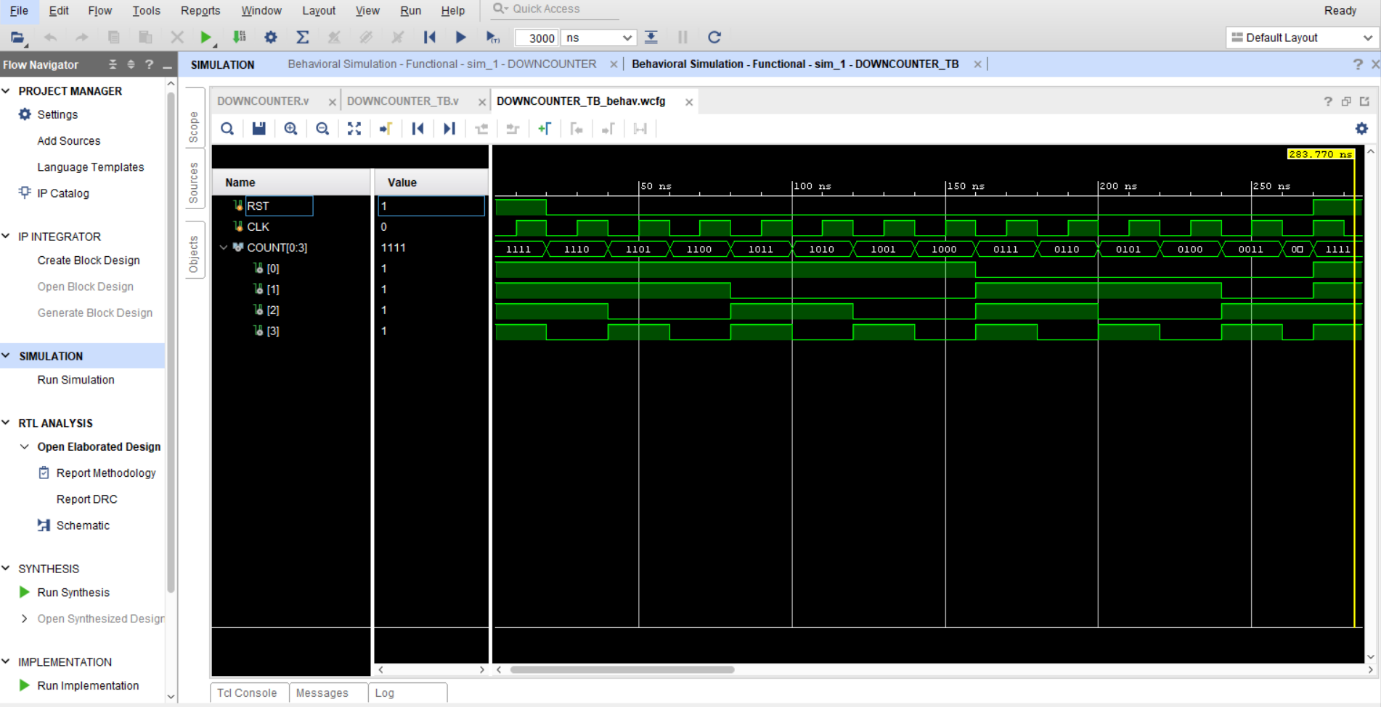
end

endmodule

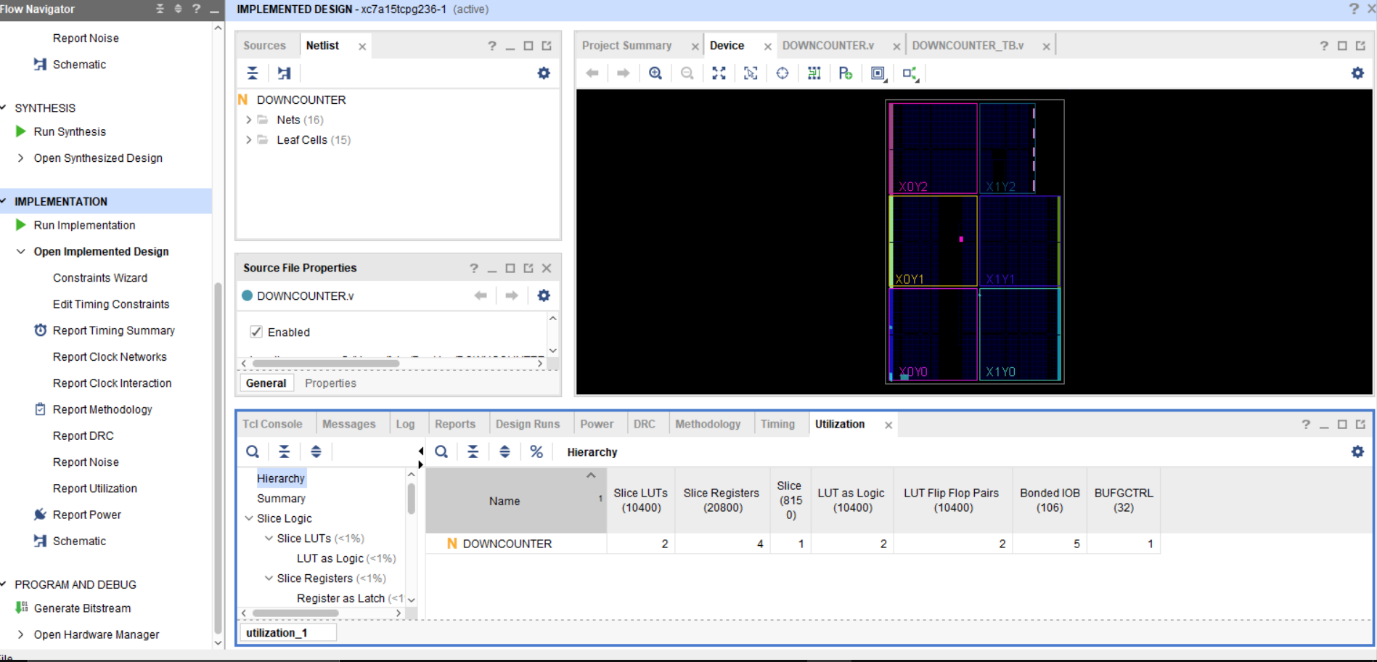
**SCHEMATIC DIAGRAM:**



**OUTPUT:**



**REPORT UTILIZATION:**



**CONCLUSION:** we have learn down counter design using Verilog code.