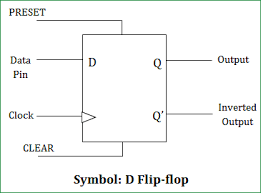
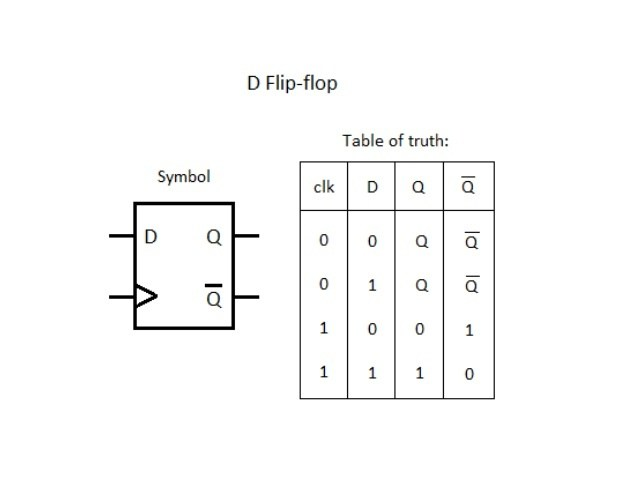
**PROBLEM** 1. Write Verilog code for D Flip-flop.

**CIRCUIT DIAGRAM:**

****

**TRUTH TABLE:**

****

**VERILOG CODE:**

module D\_FLIPFLOP(input d,

input rst,

input clk,

output reg q);

always @ (posedge clk )

case(rst)

1:q <= 0;

0:q <= d;

endcase

endmodule

**TEST BENCH:**

module D\_FLIPFLOPTB;

reg CLK;

reg D;

reg RST;

wire Q;

D\_FLIPFLOP uut( .d(D),.rst(RST),.clk(CLK),.q(Q));

initial begin

CLK <= 0;

D <= 0;

RST <= 0;

end

always #50 CLK = ~CLK;

initial

begin

RST=0;D=0;

#200

RST=0;D=1;

#200

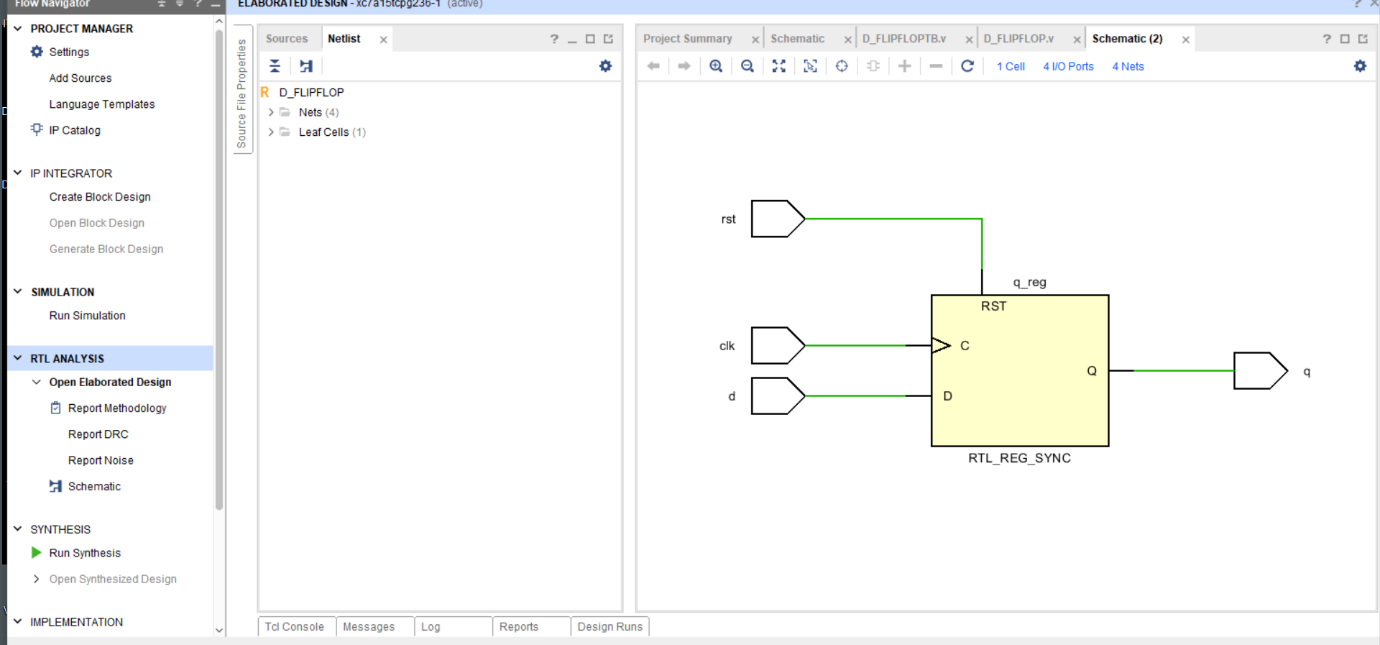
RST=1;D=0;

#200

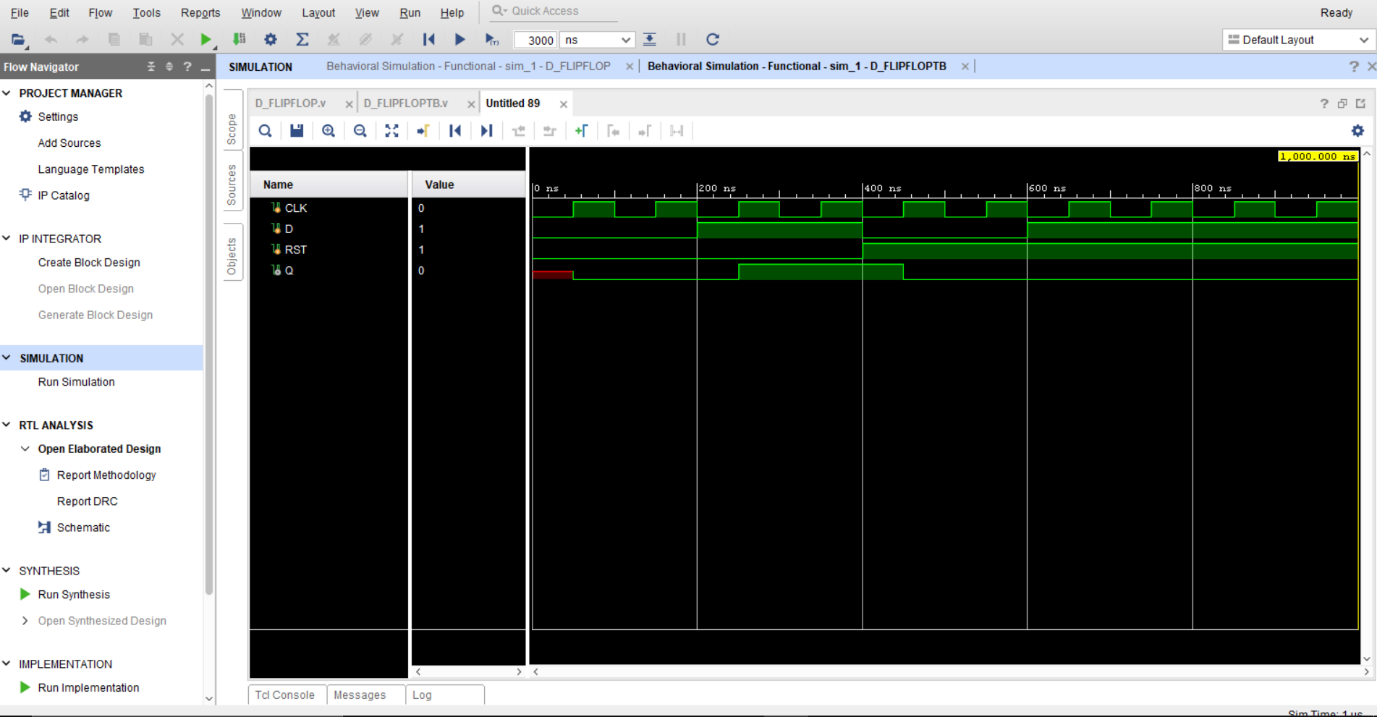
RST=1;D=1;

end

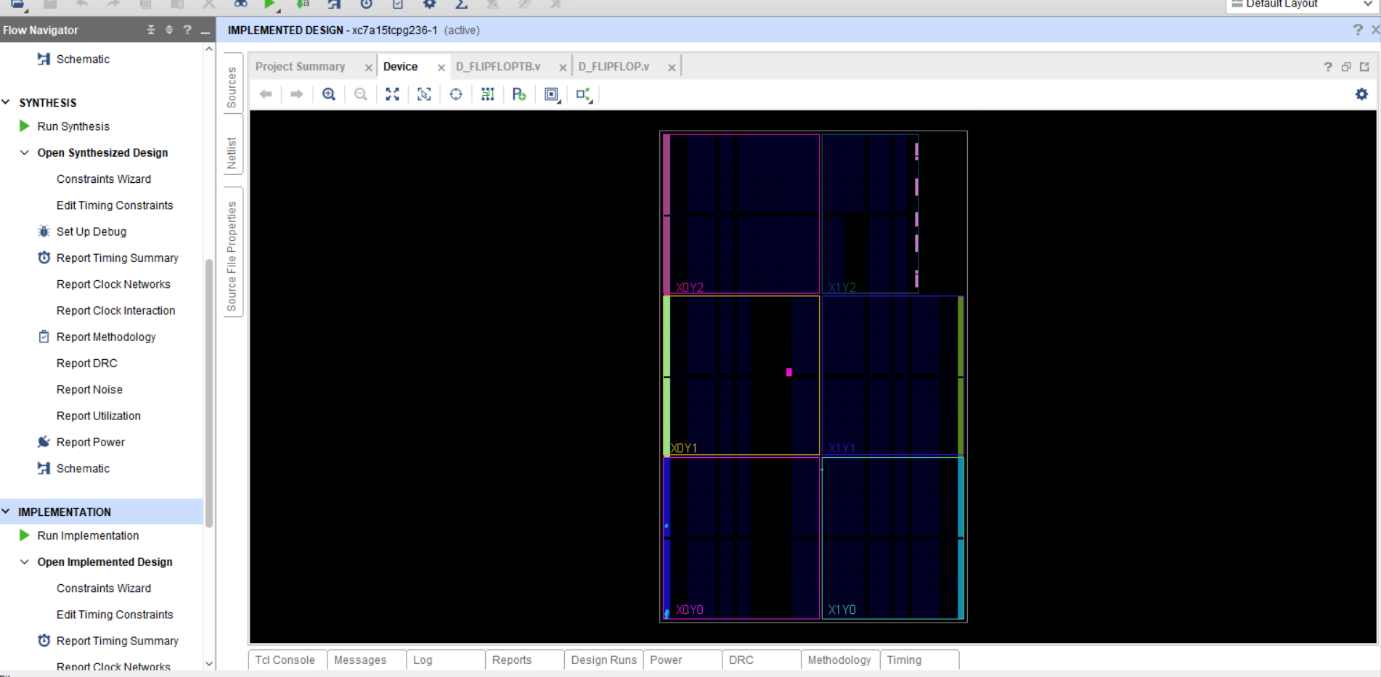
endmodule

**SCHEMATIC DIAGRAM:** 

**OUTPUT:**



**REPORT UTILIZATION:**



**CONCLUSION:** We have learn d flip flop design using Verilog code.