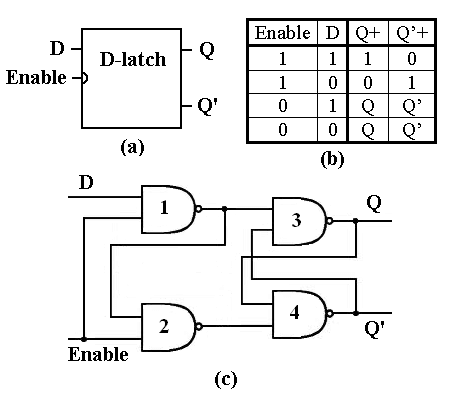
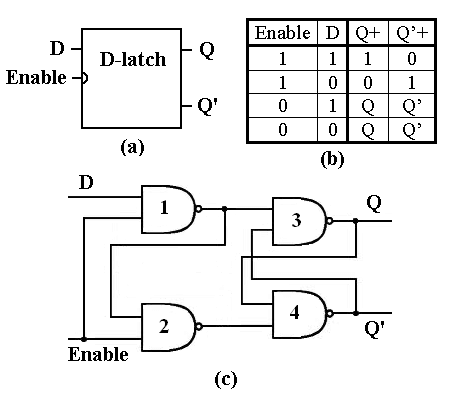
**Problem** : 6. Write Verilog code for Regular D Latch.

**CIRCUIT DIAGRAM:**

****

**TRUTH TABLE;**

****

**VERILOG CODE:**

module D\_LATCH

(input d,

input enable,

input clk,

output reg q,

output reg qbar);

always @ (posedge clk )

begin

case(enable)

0:q <= q;

1:q <= d;

endcase

qbar = ~q;

end

endmodule

**TEST BENCH:**

module D\_LATCHTB;

reg CLK;

reg D;

reg ENABLE;

wire Q;

wire QBAR;

D\_LATCH uut( .d(D),.enable(ENABLE),.clk(CLK),.q(Q),.qbar(QBAR));

initial begin

CLK <= 0;

D <= 0;

ENABLE <= 0;

end

always #50 CLK = ~CLK;

initial

begin

ENABLE=0;D=0;

#200

ENABLE=0;D=1;

#200

ENABLE=1;D=0;

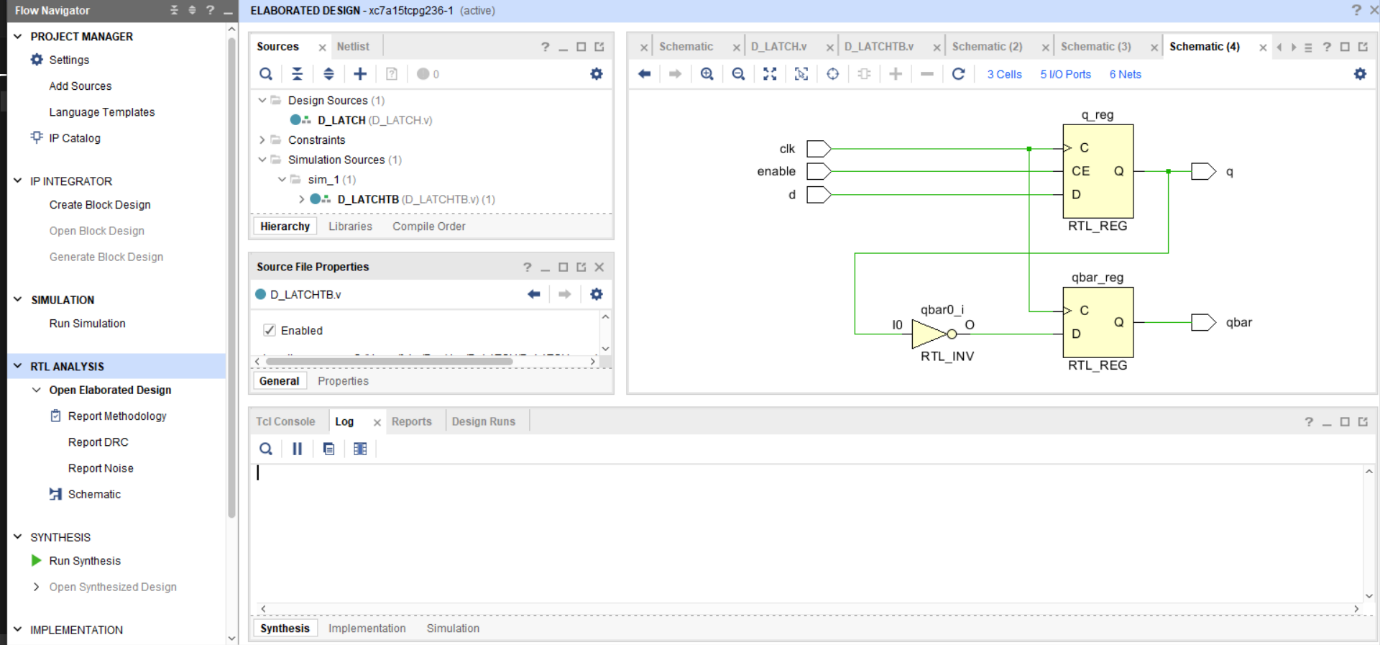
#200

ENABLE=1;D=1;

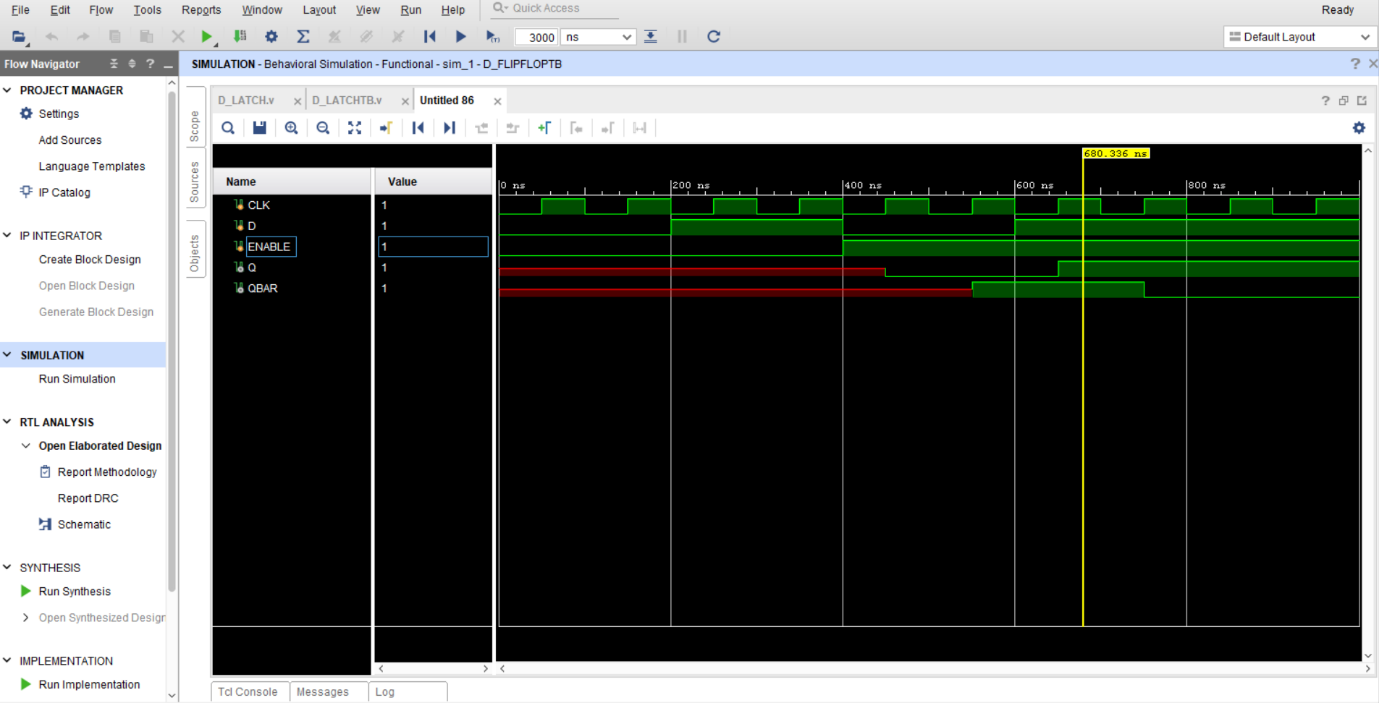
end

endmodule

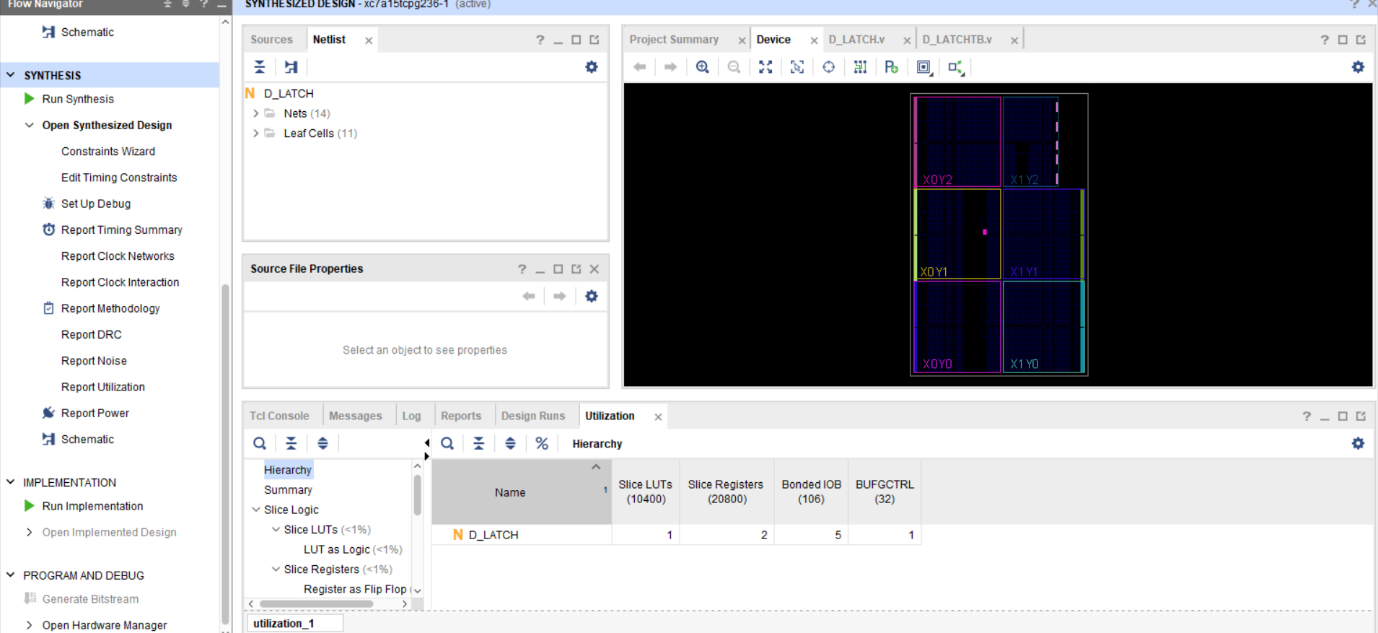
**SCHEMATIC DIAGRAM:**



**OUTPUT:**



**REPORT UTILIZATION:**



**CONCLUSION:** we have learn to design d latch using Verilog code.