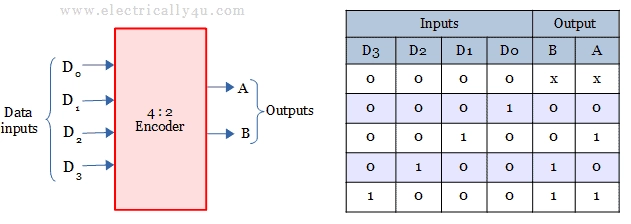
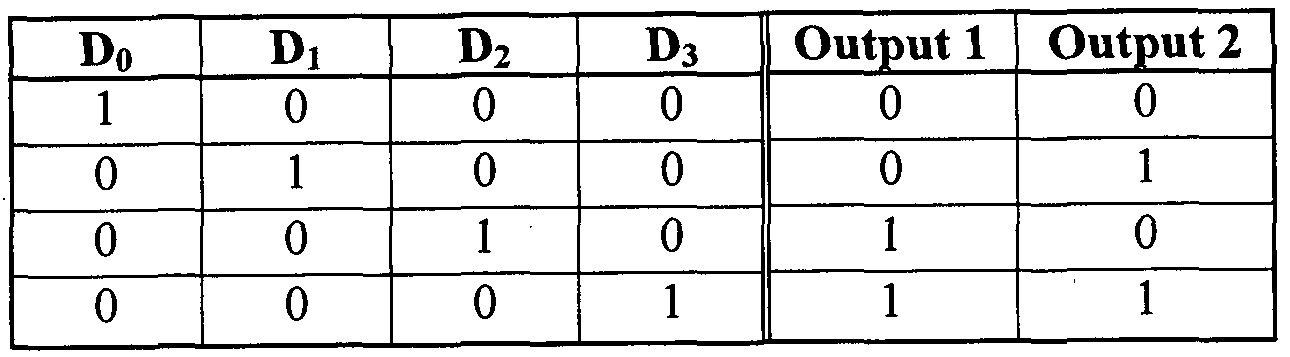
**Problem : 2(1)**  Write Verilog code for a 4-bit encoder

**Circuit design :**

****

**Truth table:**

****

**Verilog code:**

module encoder(A, Y);

input [3:0]Y;

output reg [1:0]A;

always@(Y)

begin

case(Y)

4'b0001:A = 2'b00;

4'b0010:A = 2'b01;

4'b0100:A = 2'b10;

4'b1000:A = 2'b11;

default: A = 2'bxx;

endcase

end

endmodule

**Test bench :**

module encodertb;

reg [3:0]y;

wire [1:0]a;

encoder uut(.Y(y),.A(a));

initial

begin

y=4'd0;

#100

y=4'd1;

#100

y=4'd2;

#100

y=4'd3;

#100

y=4'd4;

#100

y=4'd5;

#100

y=4'd6;

#100

y=4'd7;

#100

y=4'd8;

#100

y=4'd9;

#100

y=4'd10;

#100

y=4'd11;

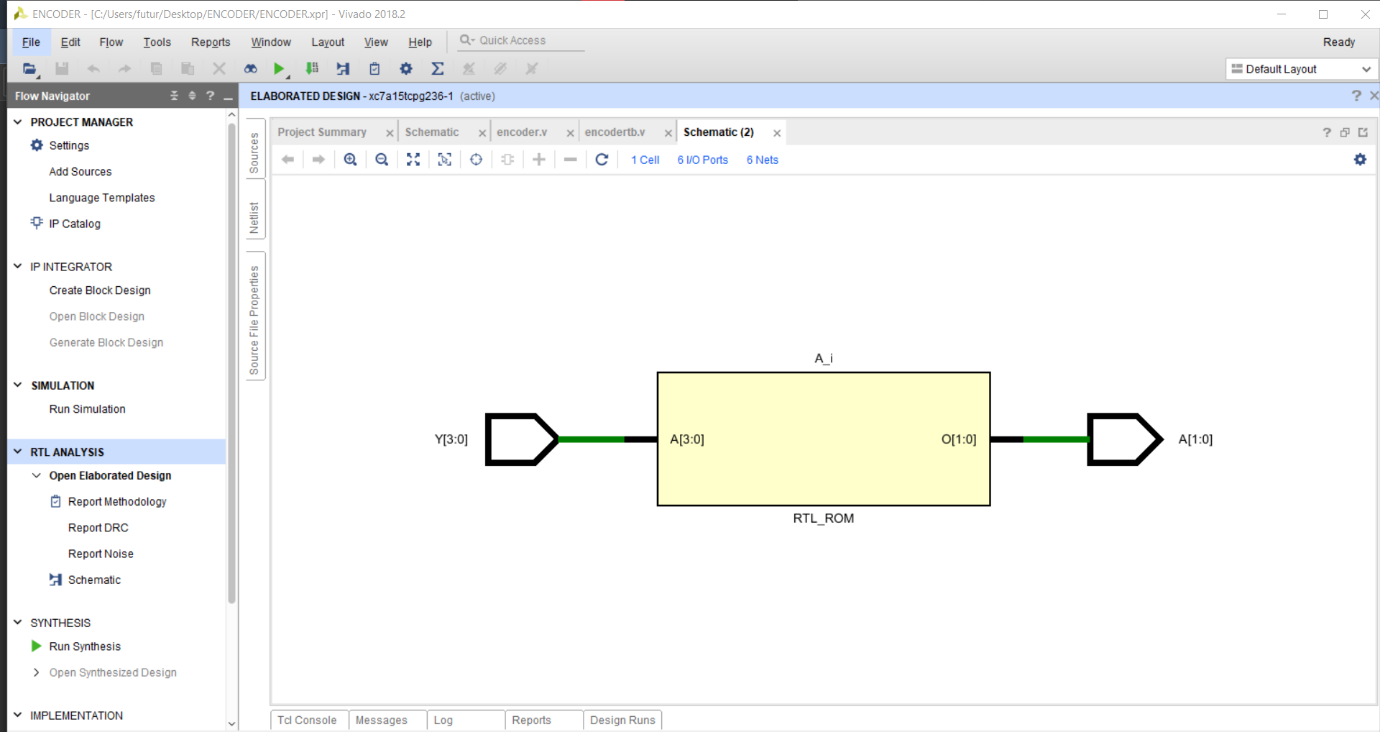
#100

y=4'd12;

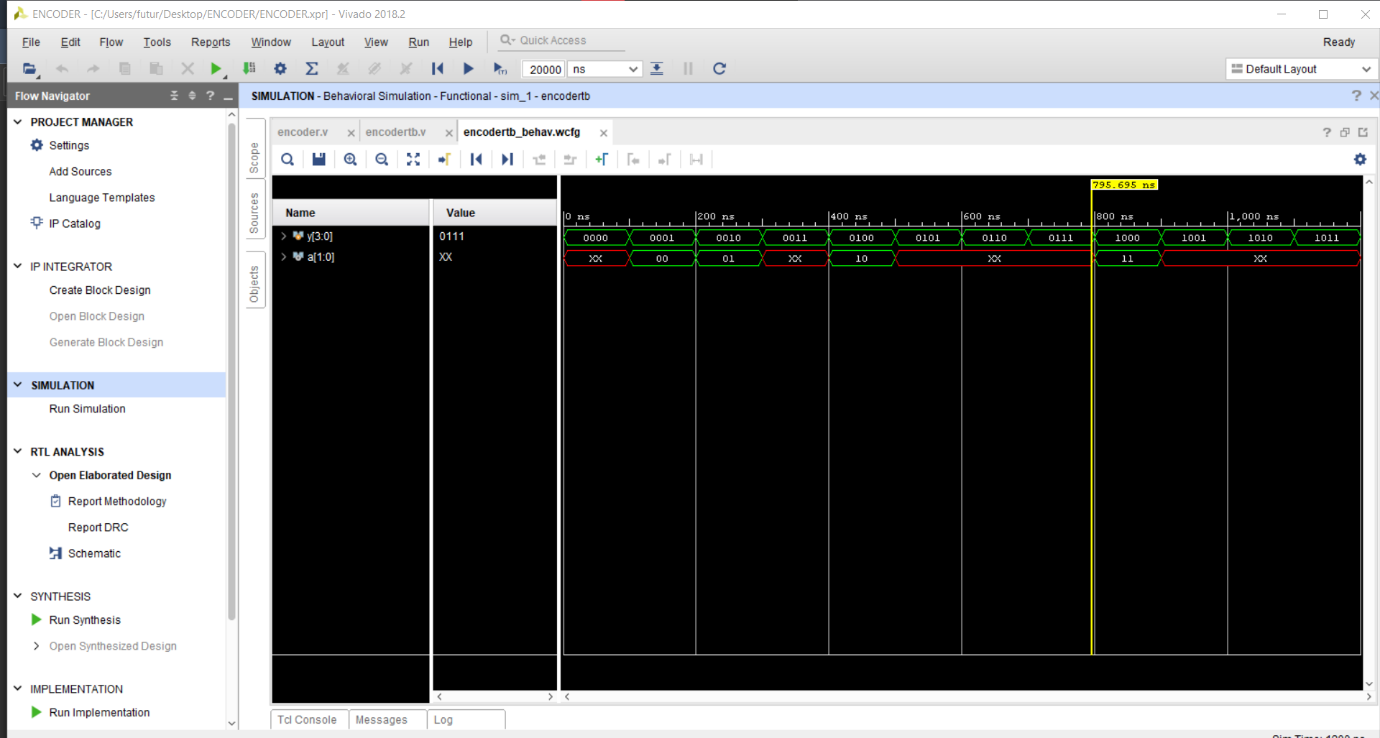
end

endmodule

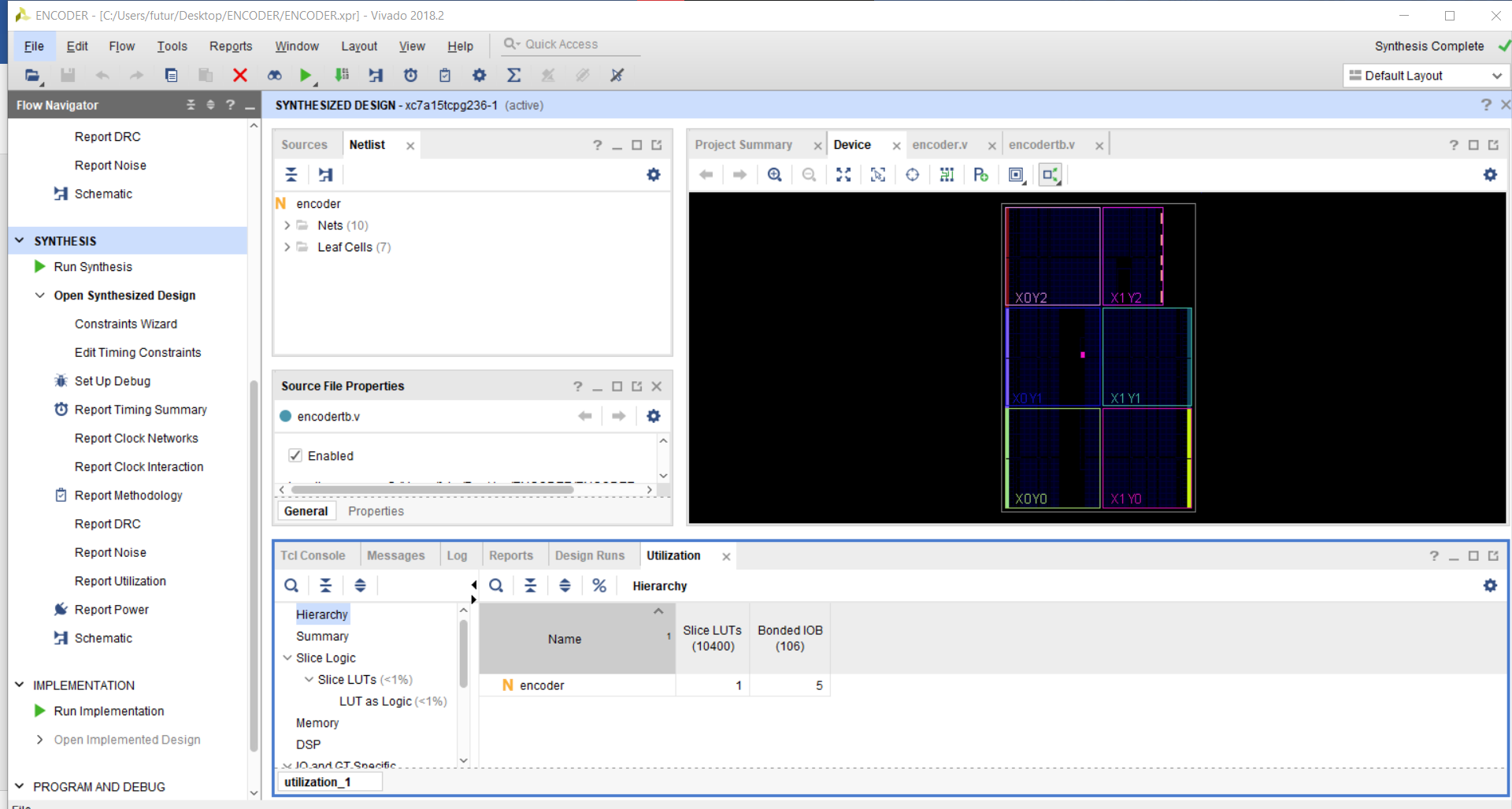
**SCHEMATICS DIAGRAM :**



**OUTPUT:**



**UTILIZATION REPORT :**

****

**CONCLUSION :** We have learn 4 bit encoder design using Verilog.