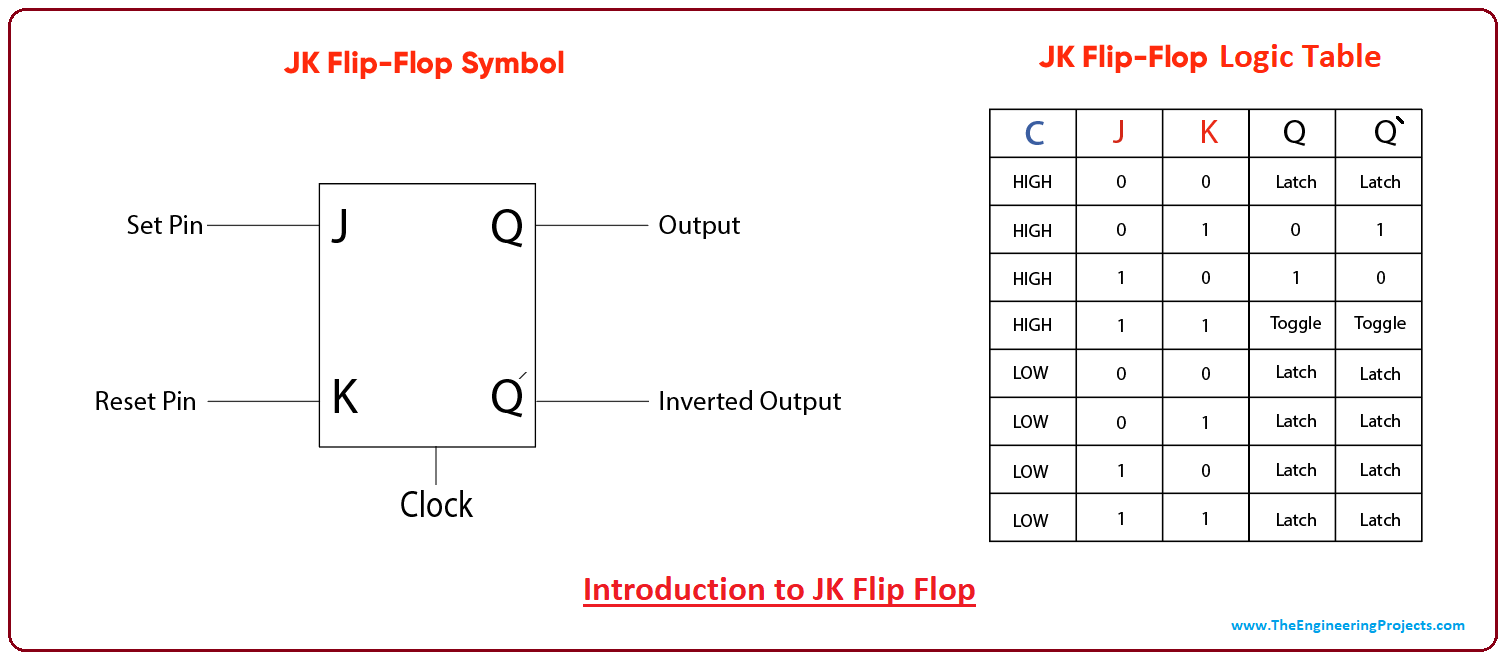
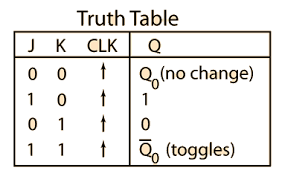
**PROBLEM:** 2. Write Verilog code for j-k Flip-flop

**CIRCUIT DESIGN:**

****

**TRUTH TABLE:**

****

**VERILOG CODE:**

module JK\_FLIPFLOP(j,k,clk,q,qb);

reg q,qb;

input clk;

input j,k;

output q,qb;

initial

begin

q<=0;

qb<=0;

end

always@(posedge clk)

begin

case({j,k})

00:q<=q;

01:q<=0;

10:q<=1;

11:q<=qb;

endcase

qb=~q;

end

endmodule

**TEST BENCH:** module JK\_FLIPFLOPTB;

reg CLK;

reg J;

reg K;

wire Q;

wire QB;

JK\_FLIPFLOP uut(.j(J),.k(K),.q(Q),.qb(QB),.clk(CLK));

initial

begin

CLK <=0;

end

always #10 CLK = ~CLK;

initial

begin

J=0;K=0;

#200

J=0;K=1;

#200

J=1;K=0;

#200

J=1;K=1;

#200

J=0;K=0;

#200

J=0;K=1;

#200

J=1;K=0;

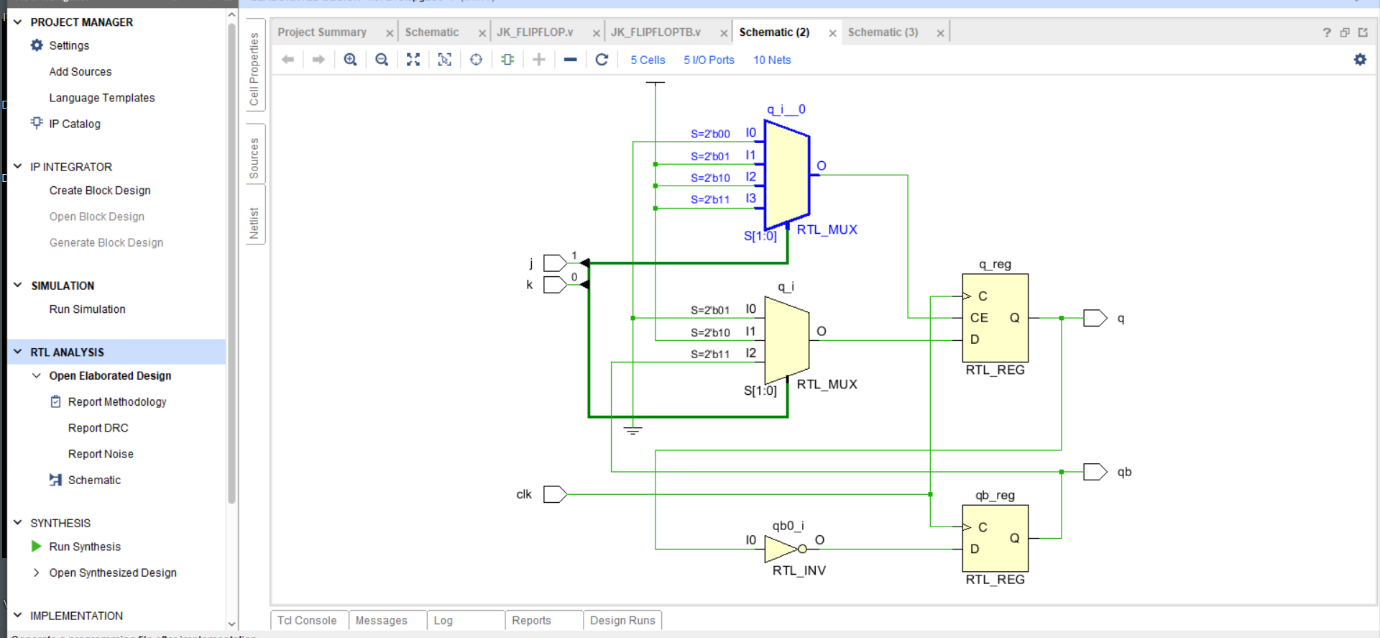
#200

J=1;K=1;

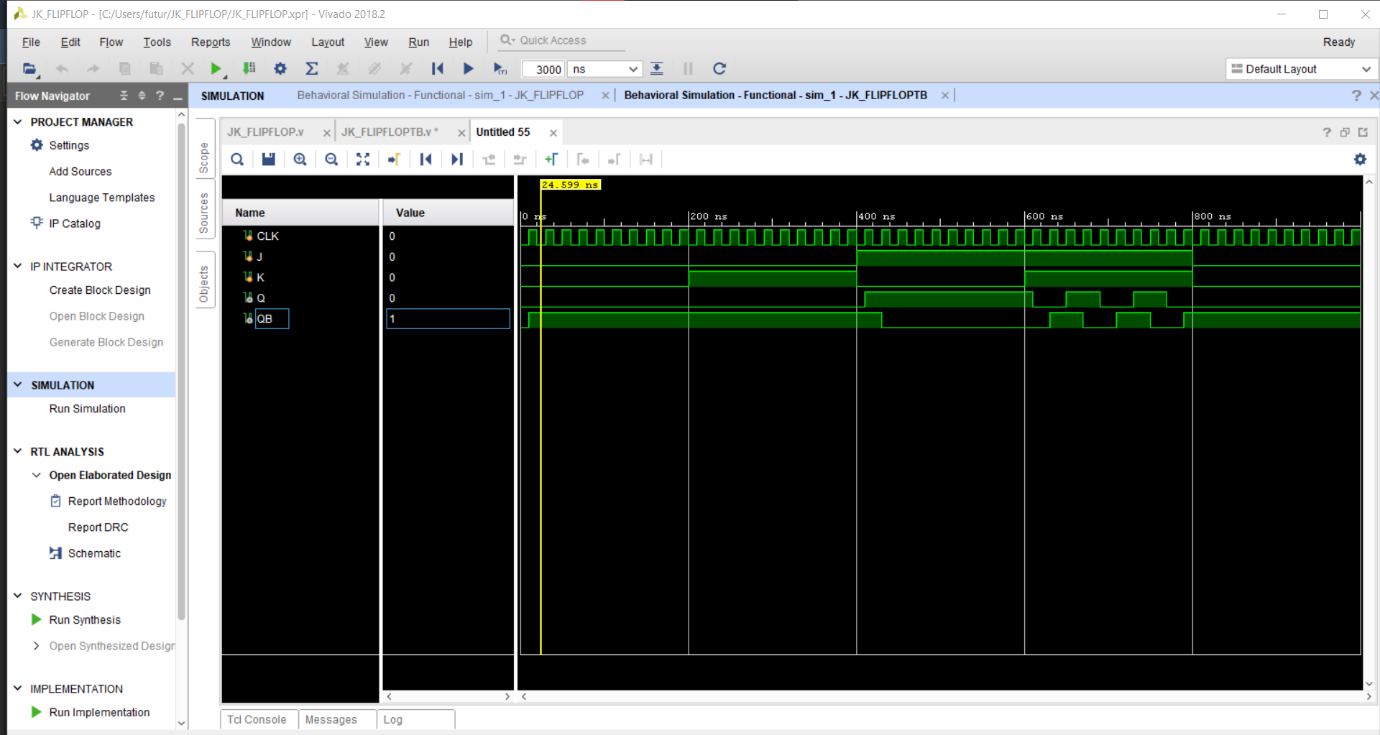
end

endmodule

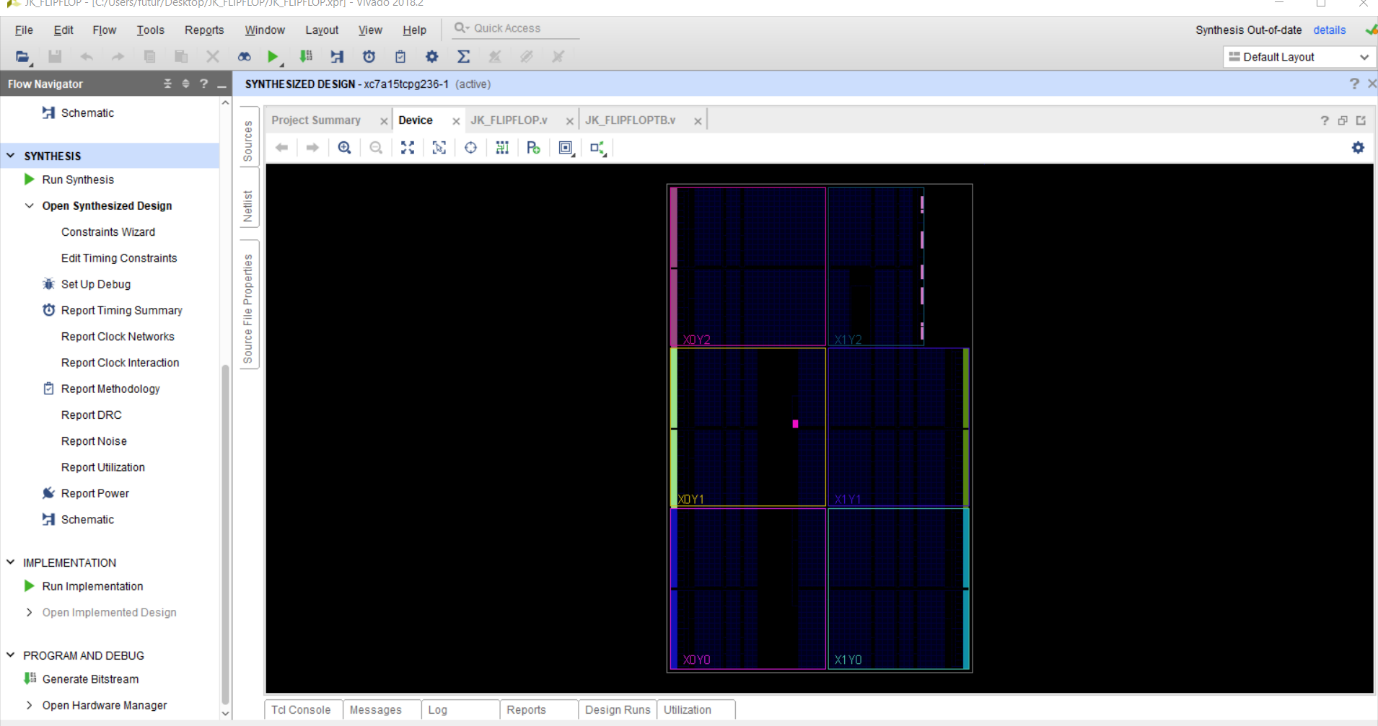
**SCHEMATIC DIAGRAM:**



**OUTPUT:**



**UTILIZATION REPORT:**



**CONCLUSION:** we have learn jk flip flop design using verliog code.