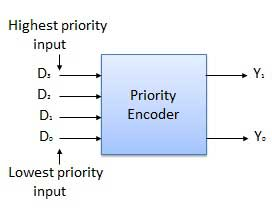
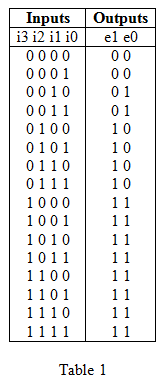
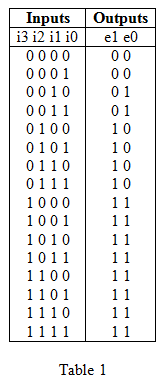
**Problem2(3)**: Write Verilog code for a 4-bit priority encoder

**CIRCUIT DIAGRAM:**

****

**TRUTH TABLE:**

****

****

**VERILOG CODE:**

module encoder(A, Y);

input [3:0]Y;

output reg [1:0]A;

always@(Y)

begin

casex(Y)

4'b0001 : A = 2'b00;

4'b001x : A = 2'b01;

4'b01xx : A = 2'b10;

4'b1xxx : A = 2'b11;

default: A = 2'bxx;

endcase

end

endmodule

**TEST BENCH:**

module priority\_encodertb;

reg [3:0]y;

wire [1:0]a;

encoder uut(.Y(y),.A(a));

initial

begin

y=4'd0;

#100

y=4'd1;

#100

y=4'd2;

#100

y=4'd3;

#100

y=4'd4;

#100

y=4'd5;

#100

y=4'd6;

#100

y=4'd7;

#100

y=4'd8;

#100

y=4'd9;

#100

y=4'd10;

#100

y=4'd11;

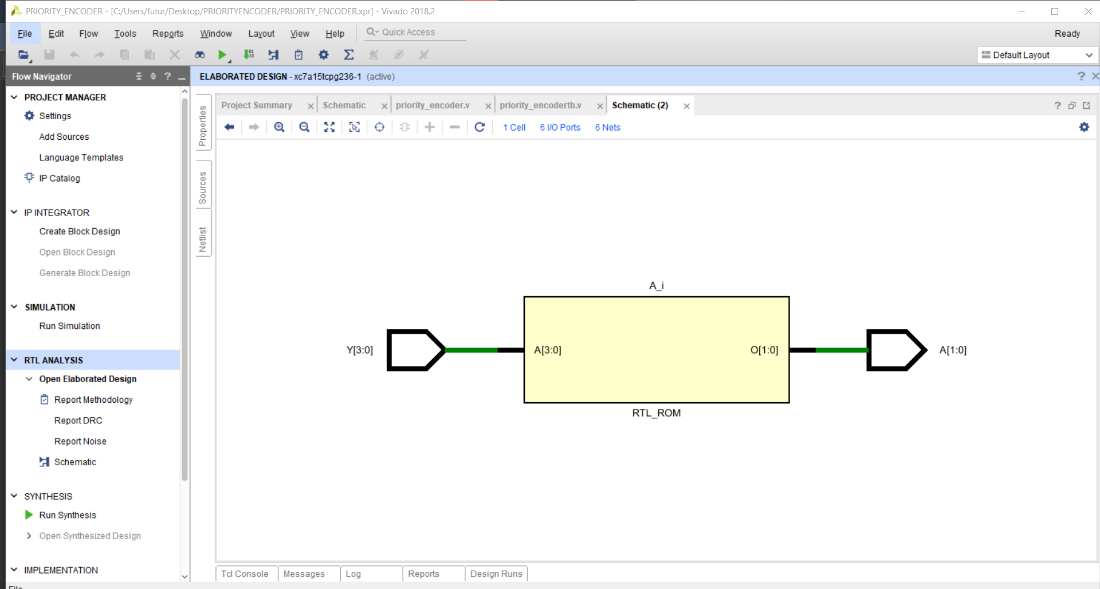
#100

y=4'd12;

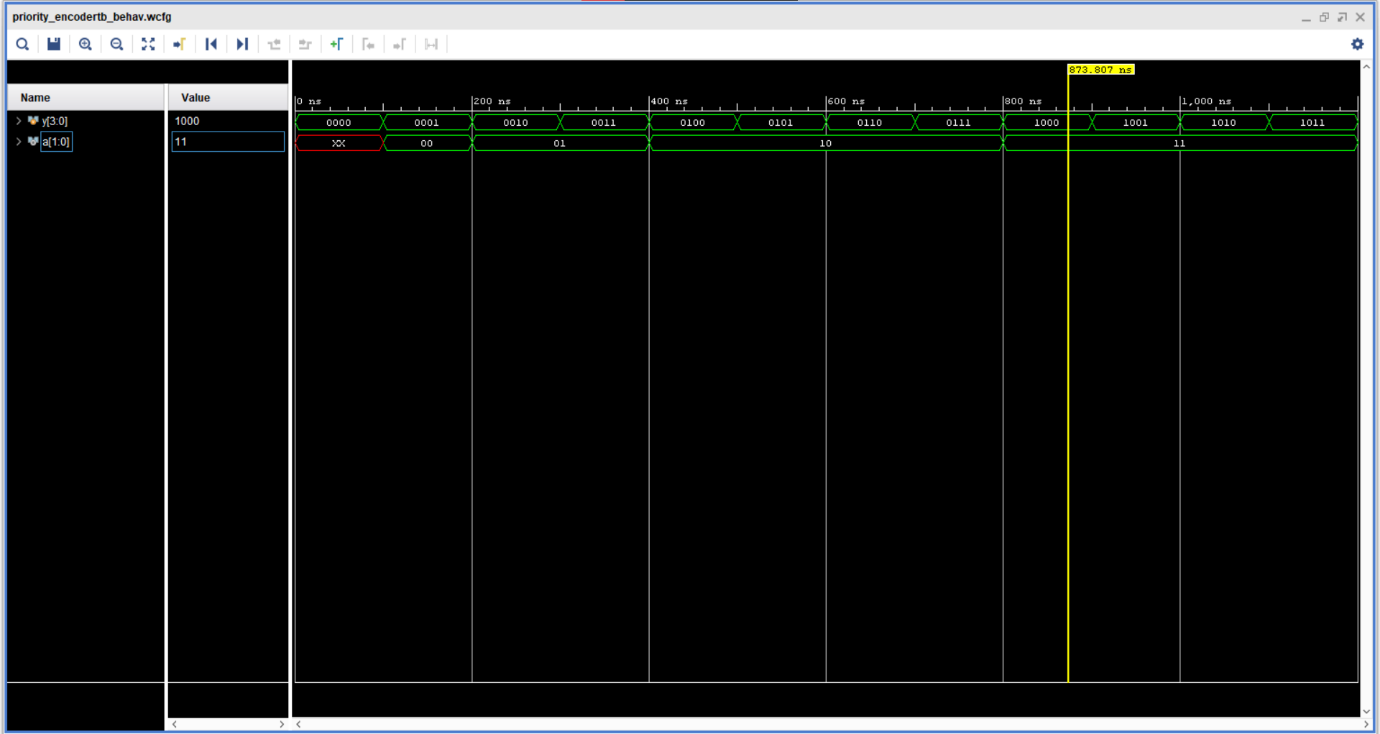
end

endmodule

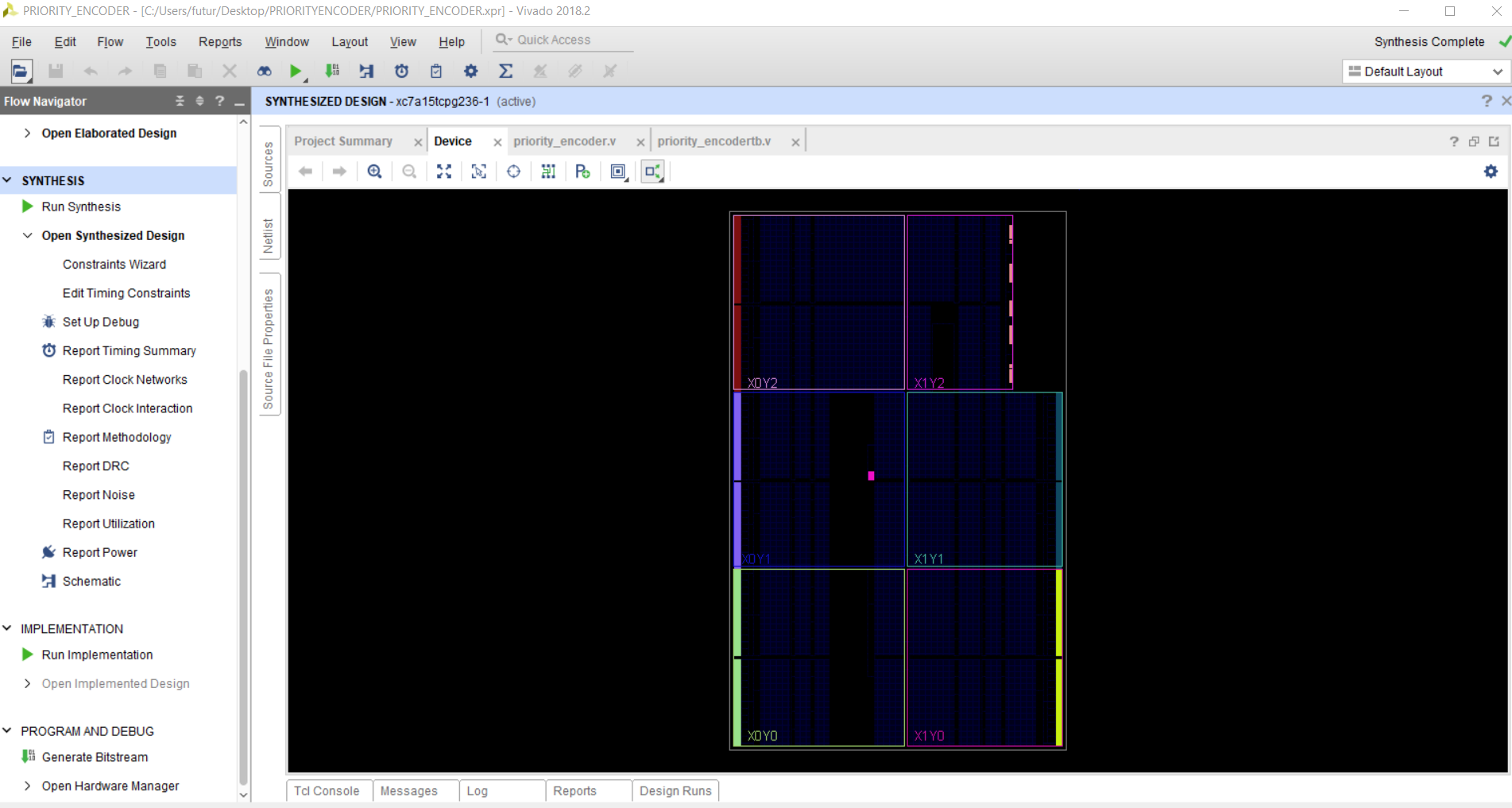




**OUTPUT:**



**Report utilization:**

****

**Conclusion :** we have learn to design 4bit priority encoder using Verilog.