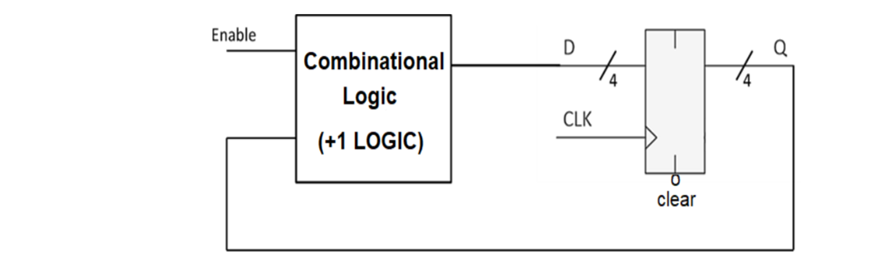
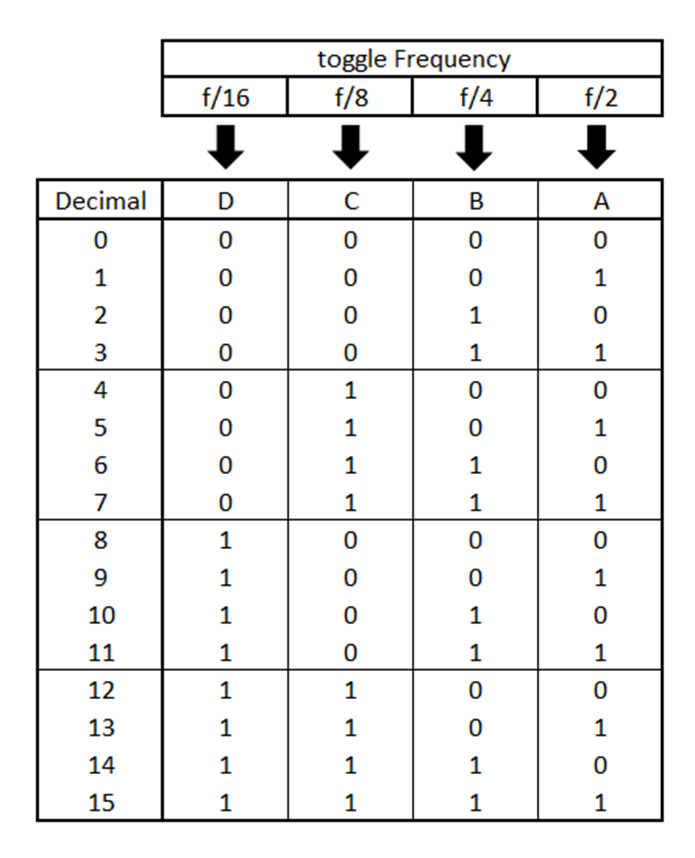
**PROBLEM:** 3. Write Verilog code for up counter.

**CIRCUIT DIAGRAM:**



**TRUTH TABLE:**



**VERILOG CODE:**

module UPCOUNTER(

input rst,

input clk,

output [3:0] count

);

reg [3:0]r;

assign count=r ;

initial

begin

r=0;

end

always@( clk,rst)

begin

if (rst==1)

r<=0;

else

r= r+1;

if (r==16)

r<=0;

end

endmodule

**TEST BENCH:**

module UPCOUNTER\_TB;

reg RST;

reg CLK;

wire [3:0]COUNT;

UPCOUNTER uut(.rst(RST),.clk(CLK),.count(COUNT));

initial

begin

CLK <=0;

end

always #10 CLK=~CLK;

initial

begin

RST=0;

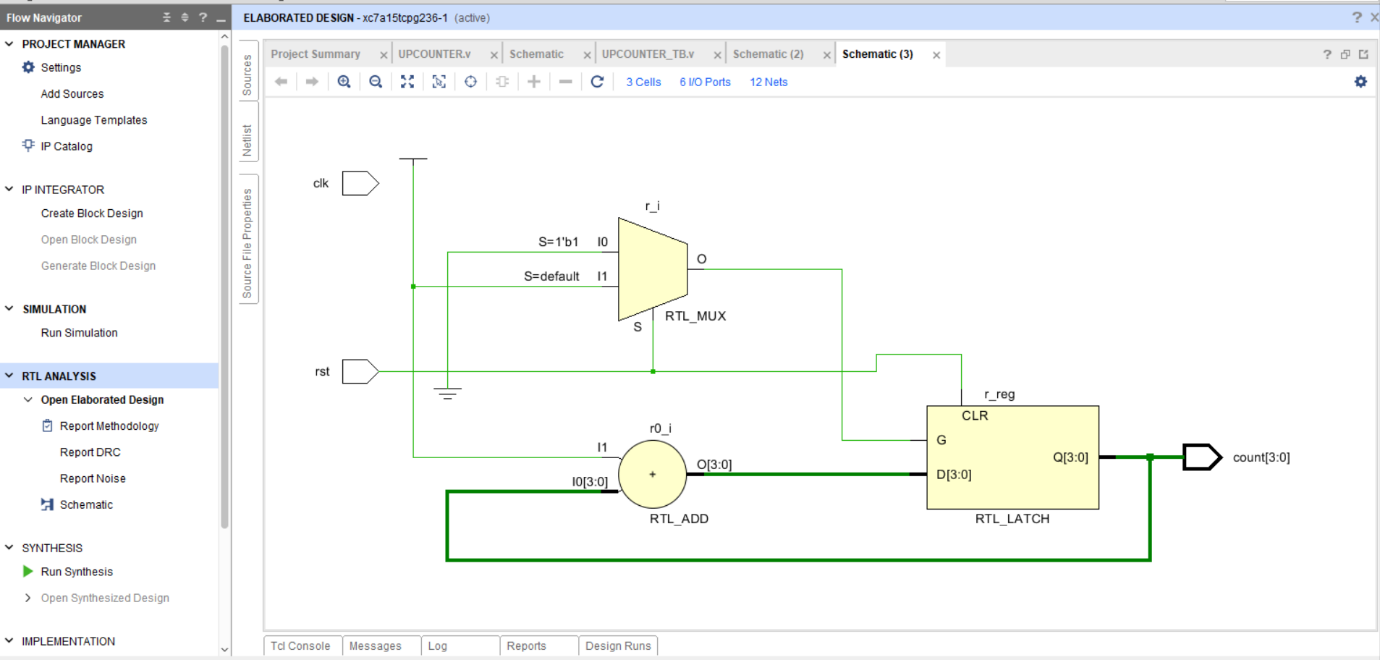
#400

RST=1;

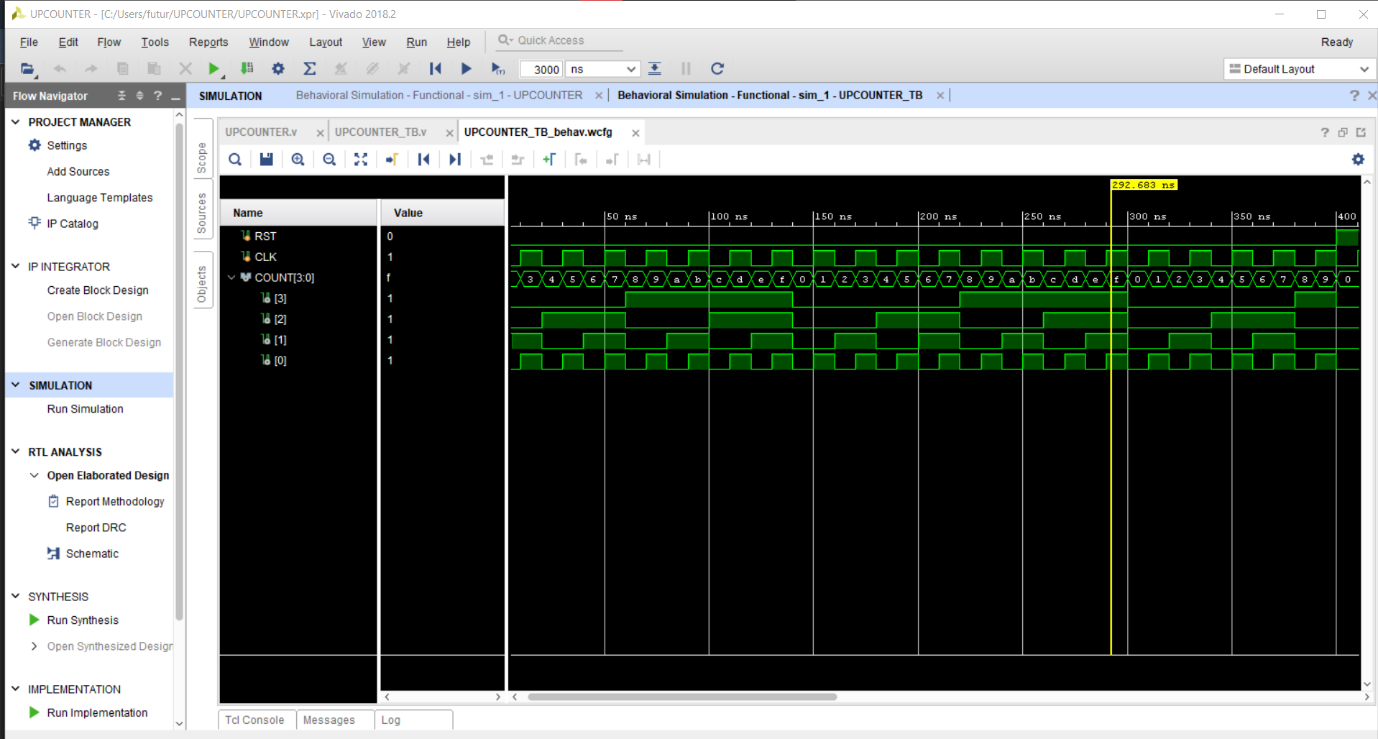
end

endmodule

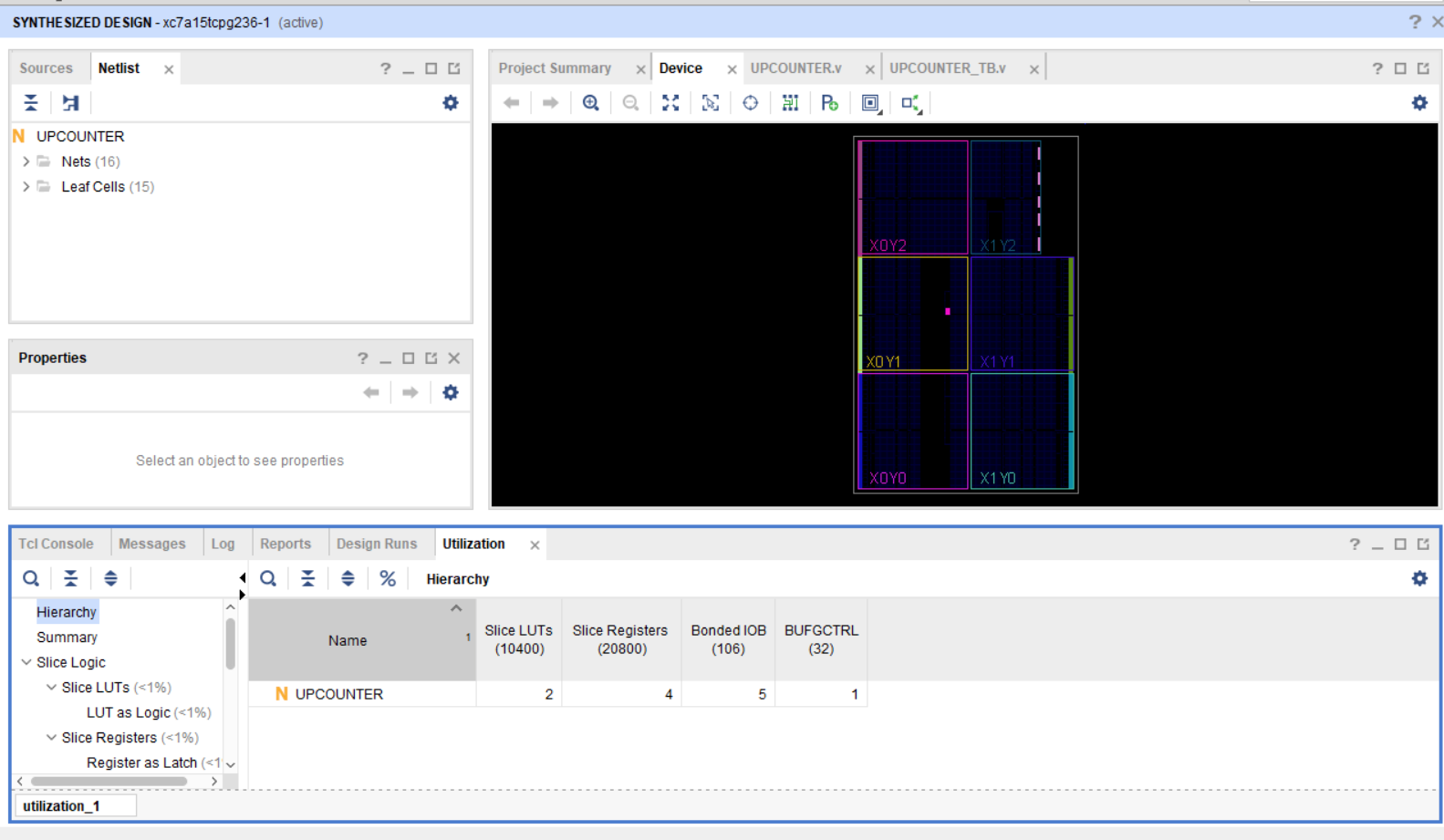
**SCHEMATIC DIAGRAM:**



**OUTPUT:**



**REPORT UTILIZATION:**



**CONCLUSION**: WE HAVE LEARN UP COUNTER DESIGN USING VERILOG CODE.