ECE-GY 6403 – Fundamentals of Analog Integrated Circuit Design

Final Project: Design of a Folded Cascode OTA

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1. Circuit Design

a. Hand Calculation

We will obtain initial gain and output resistance
To satisfy the Requirements, we will design for 15 KHz Bandwidth and an 98 dB gain.

$$GBW = 10^{\left(\frac{98}{20}\right)}\left(15\times10^{3}\right) = 1.19\times10^{9}$$

$$GBW = \frac{1}{R_{OUT}C_L}\cdot G_m R_{OUT} = \frac{G_m}{C_L}, \quad G_m = GBW\cdot C_L = 56.2\times10^{6}\left(2\cdot10^{-12}\right)$$

$$G_m = 2.38\times10^{-3} \rightarrow gm_1$$

$$A_V \geq 5623 \quad (\approx 75\,dB\ gain)$$

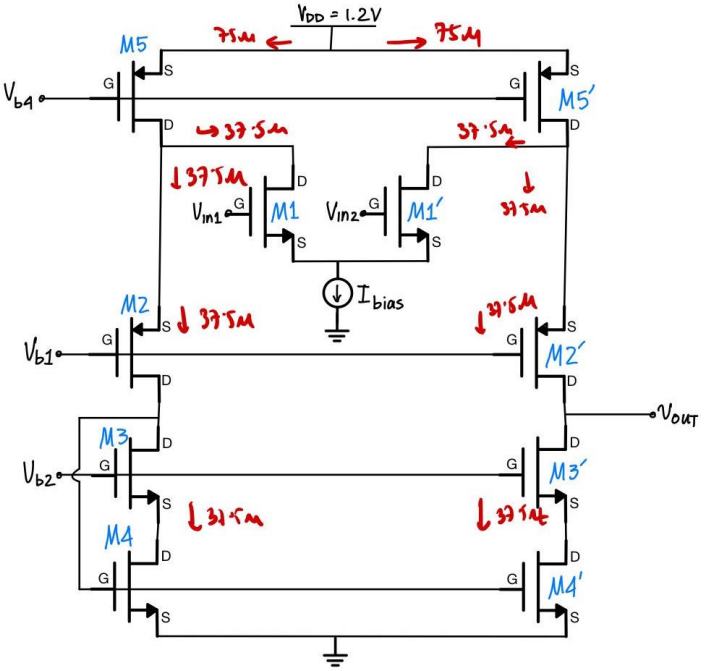
Output Resistance $\Rightarrow \approx 50\,M\Omega$

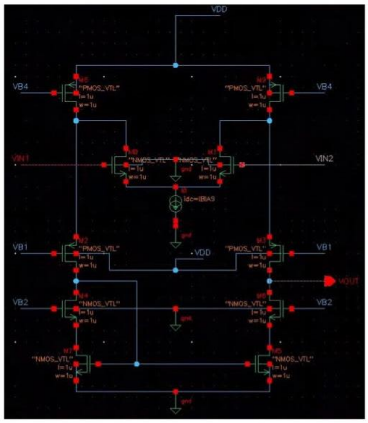
Design Specifications:	I/O Parameters
Gain > 70 dB	$V_{DD} = 1.2V$
$f_{3dB} > 10\,KHz$	$C_L = 2pF$
Slew Rate > 30 $V/\mu s$	
Phase Margin > 60°	
Power Consumption < 200 µW	

Taking Power = $V_{DD} \times I_D$;
∵ Power has to be < 200µW, We take it as 180 µW.
$180\,\mu W = 1.2V \times I_D$; $I_D = \frac{180\mu W}{1.2V} = 150\,\mu A$.

∵ there is no constraint on maximum diff. swing.

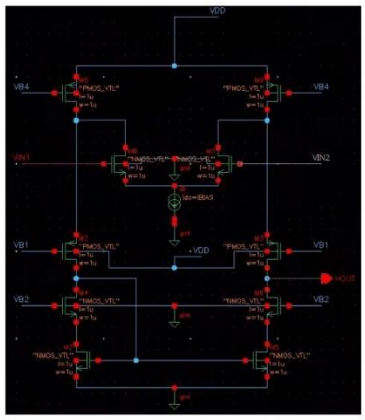
We will use the following topology:
OTA: Differential Input, Single ended output





$2\cdot[V_{DD} - |V_{ov6}| - |V_{ov3}| - V_{ov4} - V_{ov7}] \geq 1.82$
$[V_{DD} - |V_{ov6}| - |V_{ov3}| - V_{ov4} - V_{ov7}] = 0.91$
$V_{DD} - 0.91 = |V_{ov6}| - |V_{ov3}| - V_{ov4} - V_{ov7}$
$\therefore |V_{ov6}| - |V_{ov3}| - V_{ov4} - V_{ov7} = 0.29V$

Considering the gain specification of 70dB, the original hand calculation was set to use a amplifier gain of around 90dB – 100 dB. Using this value, a rough estimate of gm1 was determined to be around 0.002. The desired power specification was considered to be around 180 µW, and due to this, a drain current of 150 µA was calculated. Next, the current paths using KCL were determined and the IBIAS value of 75 µA was determined. Afterwards, overdrive voltages for the transistors were chosen to provide the desired gain and transistor sizes.



Transistor Sizing:

$\left(\frac{W}{L}\right)_{0,1} = \frac{75\times10^{-6}}{265\times10^{-6}\times(0.03)^2} \simeq 325.51$

$\left(\frac{W}{L}\right)_{8,9} = \frac{150\times10^{-6}}{126\times10^{-6}\times(0.1)^2} \simeq 119.048$

$\left(\frac{W}{L}\right)_{2,3} = \frac{75\times10^{-6}}{126\times10^{-6}\times(0.07)^2} \simeq 121.447$

$\left(\frac{W}{L}\right)_{4,6} = \frac{75\times10^{-6}}{265\times10^{-6}\times(0.05)^2} \simeq 117.18$

$\left(\frac{W}{L}\right)_{5,7} = \frac{75\times10^{-6}}{265\times10^{-6}\times(57.75)^2} \simeq 59.790$

$V_{b2} = V_{ov7} + V_{GS4}$ $\because V_{GS_4} - V_{th_n} = V_{ov4}$

$\therefore V_{b_2} = 0.07 + 0.05 + 0.322 = 0.442$

$V_{b4} = V_{DD} - |V_{SG8}| = 1.2 - [V_{ove} - V_{thp}]$

$= 1.2 - [0.1 + 0.302]$

$= 0.798$

$|V_{ov8}| - |V_{ov5}| - V_{ov4} - V_{ov7} = 0.29V$

$\therefore$ Assuming: $V_{ov_{5,7}} = 0.1V$

$V_{ov_{0,1}} = 0.03V$

$V_{ov_{2,3}} = 0.07V$

$V_{ov_{4,6}} = 0.05$

$V_{ov_{8,9}} = 0.07$

$V_{b1} = V_{DD} - |V_{ov8}| - |V_{SG2}|$ $\because V_{SG_2} = V_{ov_2} + V_{thp}$

$= 1.2 - [0.1 + 0.07 + 0.302]$

$= 0.442V$

$A_V = g_{m1}\left[(g_{m4}r_{o4}r_{o7}) \parallel (g_{m2}r_{o2}(r_{o8} \parallel r_{o1})\right]$

Calculating gm's of transistors:

$g_{m1} = \frac{2I_{D1}}{V_{ov_1}} = \frac{75\times10^{-6}}{0.03} = 0.00250$

$g_{m2} = \frac{2I_{D2}}{V_{ov_2}} = \frac{75\times10^{-6}}{0.07} = 0.00107$

$g_{m4} = \frac{2I_{D4}}{V_{ov_4}} = \frac{75\times10^{-6}}{0.05} = 0.00150$

$r_{o2} = \frac{1}{\lambda_p I_{D2}} = \frac{1}{0.2\times37.5\times10^{-6}} = 1.33\times10^5\ \Omega$

$r_{o8} = \frac{1}{\lambda_p I_{D8}} = \frac{1}{0.2\times75\times10^{-6}} = 66.66\ K\Omega$

decrease V_{ov7}; V_{ov1}

$r_{o4} = r_{o7} = r_{o1} = \frac{1}{\lambda_n I_{D4}} = \frac{1}{0.1\times37.5\times10^{-6}} = 2.66\times10^5\ \Omega$

$\therefore$ We input the calculated parameters in:

$A_V = g_{m1}\left[(g_{m4}r_{o4}r_{o7}) \parallel (g_{m2}r_{o2}(r_{o8} \parallel r_{o1})\right]$

$A_V = 250\times10^{-6}\left[(150\times10^{-6})\times(2.66\times10^5)^2 \parallel (107.1\times10^{-6})\times(1.33\times10^5)\times(66.66\times10^3) \parallel (2.66\times10^5)\right]$

$= 17777.77 \Rightarrow 17.77\ K$ gain.

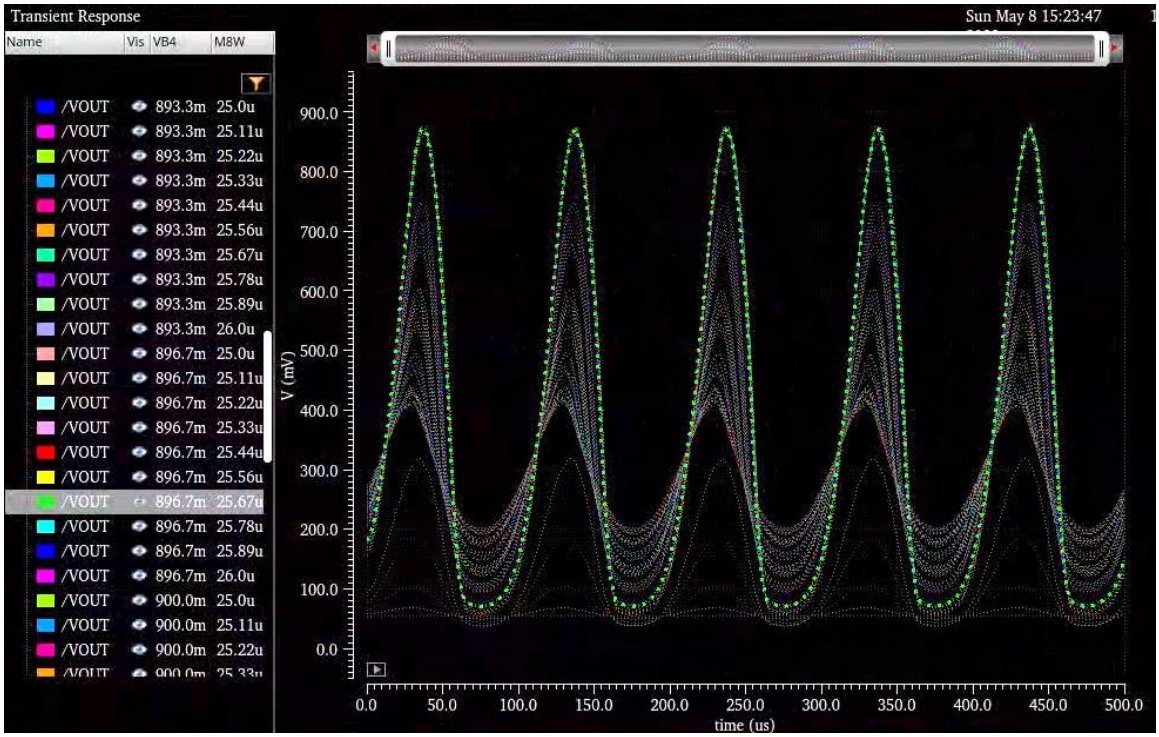
From the calculations above, the estimated transistor size rations were tabulated below.

Transistor Pair	Aspect Ratio
M0, M1	325
M2, M3	121
M4, M6	117
M5, M7	59
M8, M9	119

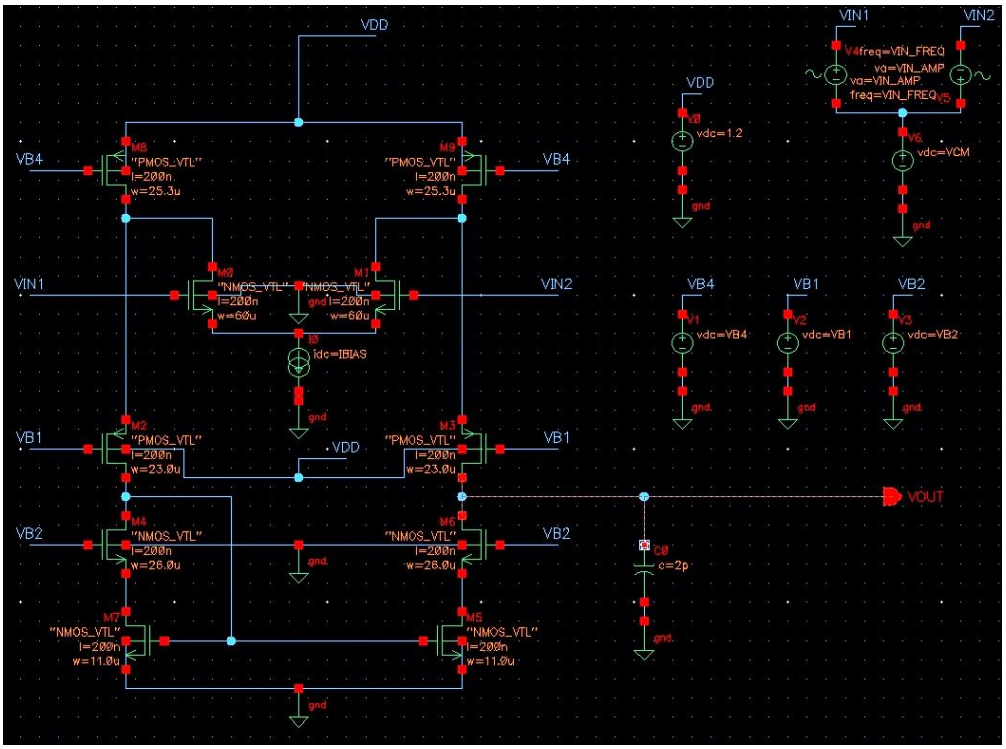
2. Simulation Results

a. Sizing

Once the rough hand calculations were complete, the design was built within Cadence and then several parametric simulations were run. Namely, in order to fine tune both the transistor sizes and the bias voltages, parametric simulations in which both the transistor width and bias voltage were swept within a range close to the calculated hand value. Since the maximum transistor width within cadence is 100 µm, the lengths of each of the transistors were lowered to 200 nm and matched. This allowed for transistor aspect ratios of up to 500, which was useful both when building the amplifier circuit and when building the voltage biasing circuit. An example of a parametric sweep is shown below, and this parametric sweep checked the relationship between the output voltage swing, the voltage of VB4, and the width of transistors M8 and M9. From this sweep, it can be seen that the output swing is the largest when the bias voltage is 896 mV, and the transistor width is 25.6 µm. Similar parametric sweeps were done with the other bias voltages and transistors, and then sweeps were done with multiple bias voltages at once to check if correlating them would result in a higher swing.



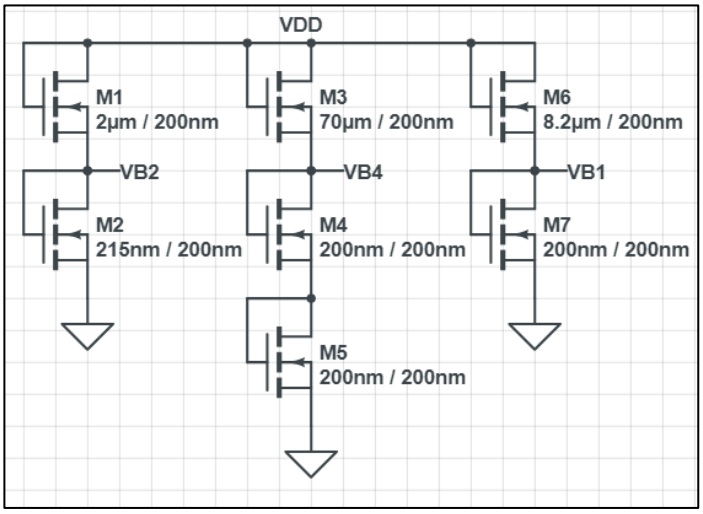
A common mode voltage of 300 mV was chosen in order to bias the input transistors. The common mode voltage was chosen using a parametric sweep, where the largest output was determined at an input of 300 mV. Shown below are the parameters along with the preliminary schematic before creating the voltage biasing circuit. As shown in the design variables table, the final voltage bias values were chosen to be 734 mV for VB1, 670 mV for VB2, and 897 mV for VB4. Using these bias values, the OTA is able to amplify the differential input signal through the use of cascoded transistors. With the benefit of the two folded NMOS input transistors, the amplifier is able to stay on with fluctuations in Vin, through the use of an alternate current path.



Design Variables

	Name	Value
1	VB1	734m
2	VB2	670m
3	VB4	897m
4	IBIAS	75.2u
5	VCM	300m
6	VIN_AMP	100u
7	VIN_FREQ	5K

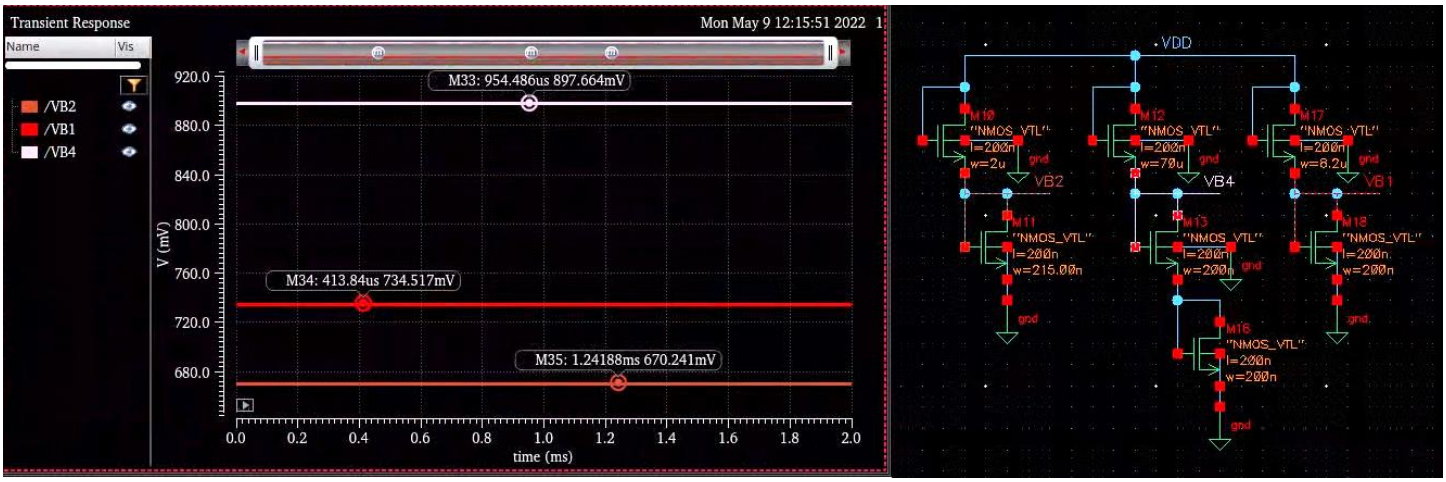
Next, the voltage biasing circuit was created in conjunction with the previously determined bias voltages shown above. NMOS transistors were used in diode connected configurations to create the bias voltages. To generate the desired voltage, the widths of each of the transistors were changed and a transient plot was created. The image below depicts both the transient response and circuit configuration for these NMOS transistors. As shown in the image below, the voltage bias circuit was able to produce the three bias voltages correctly and accurately. A table is also given below with the transistor sizes for the voltage biasing circuit.



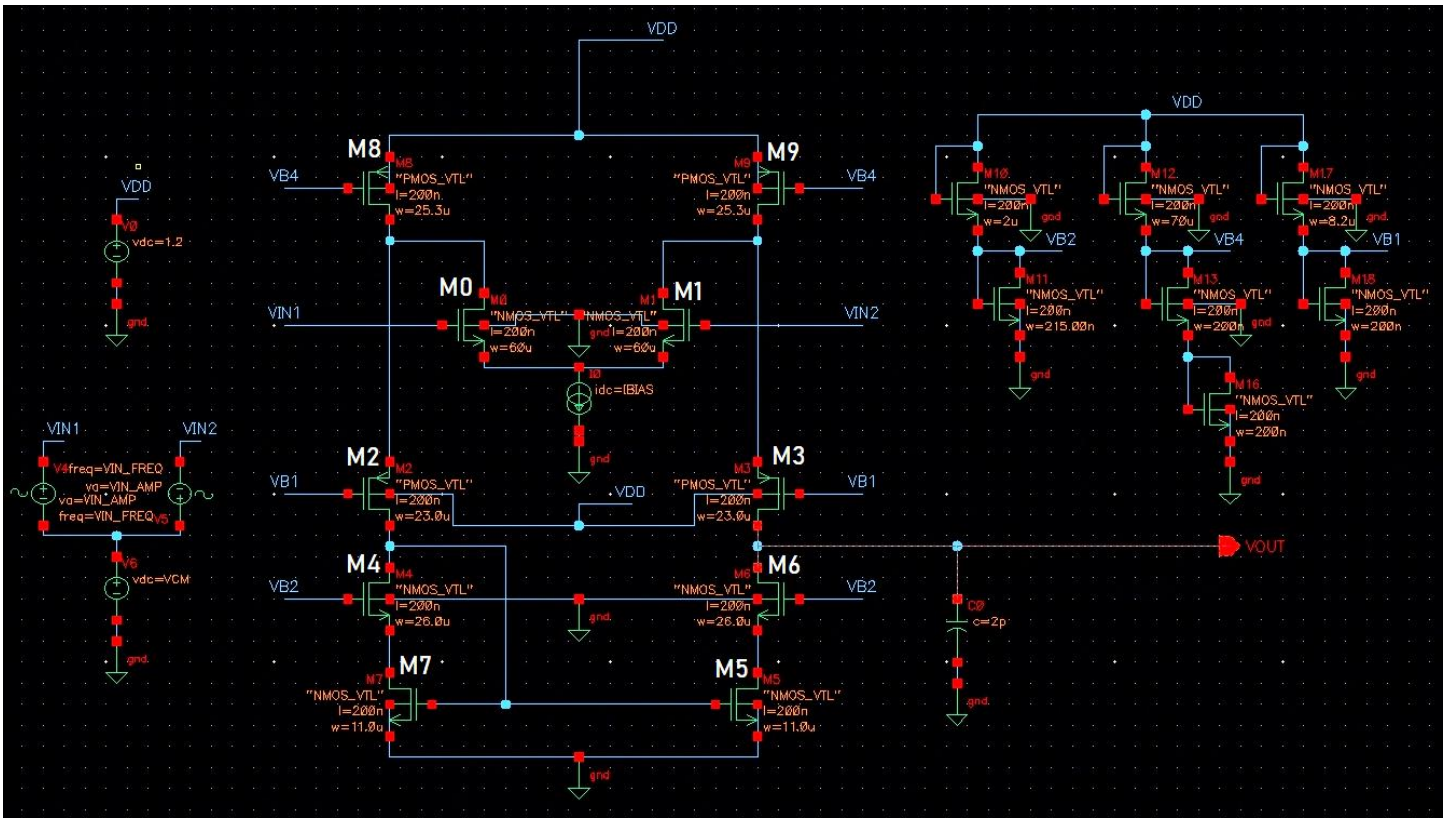
VB2	Width(µm)	Length(µm)	Voltage(V)
M1	2.00	0.20	**0.670**
M2	0.215	0.20	

VB4	Width(µm)	Length(µm)	Voltage
M3	70.00	0.20	**0.897**
M4	0.20	0.20	
M5	0.20	0.20	

VB1	Width(µm)	Length(µm)	Voltage
M6	8.20	0.20	**0.734**
M7	0.20	0.20	



The final schematic for the folded cascode OTA is shown below, along with the voltage biasing circuit.



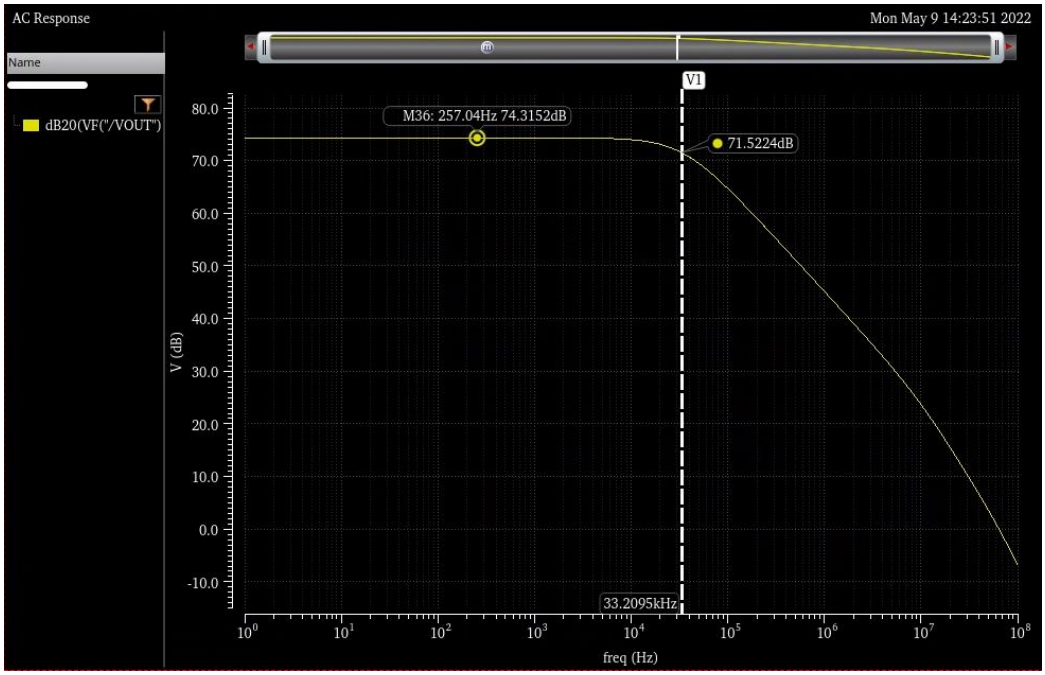
The final parameters for transistor sizing are given below. The final aspect ratio sizes of the transistors were found to be very close to the original hand calculations.

Transistor Pair	Width(µm)	Length(µm)	Aspect Ratio
M0, M1	60.00	0.20	300
M2, M3	23.00	0.20	115
M4, M6	26.00	0.20	130
M5, M7	11.00	0.20	55
M8, M9	25.30	0.20	126.5

b. AC Simulations

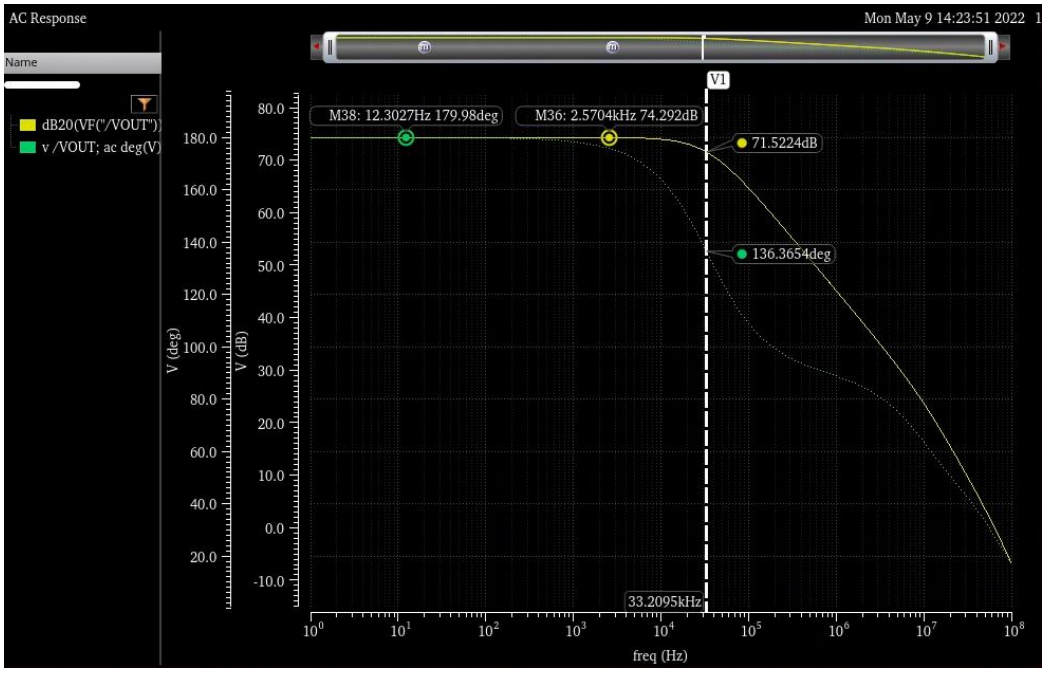
Gain and 3dB Frequency

An AC analysis was conducted to determine the gain and 3dB frequency of the folded cascode OTA. For the AC analysis, the input differential AC sources were removed and replaced with a DC voltage source, with the DC voltage unspecified. The AC analysis was then run for an input frequency range from 1 Hz to 100 MHz. As shown below in the bode plot, the OTA achieved an amplification of 74.31 dB, which is higher than the desired specification. Similarly, the 3dB frequency was found to be around 33.2 kHz, at an amplification of 71.52 dB.



Phase Margin

The phase margin plot was obtained with the same AC analysis by directly plotting the phase margin component. As shown below, the phase margin was found to be stable between 1 Hz and 10 kHz, with a degree value of 180. At the 3dB frequency, the phase dropped to 136 degrees.

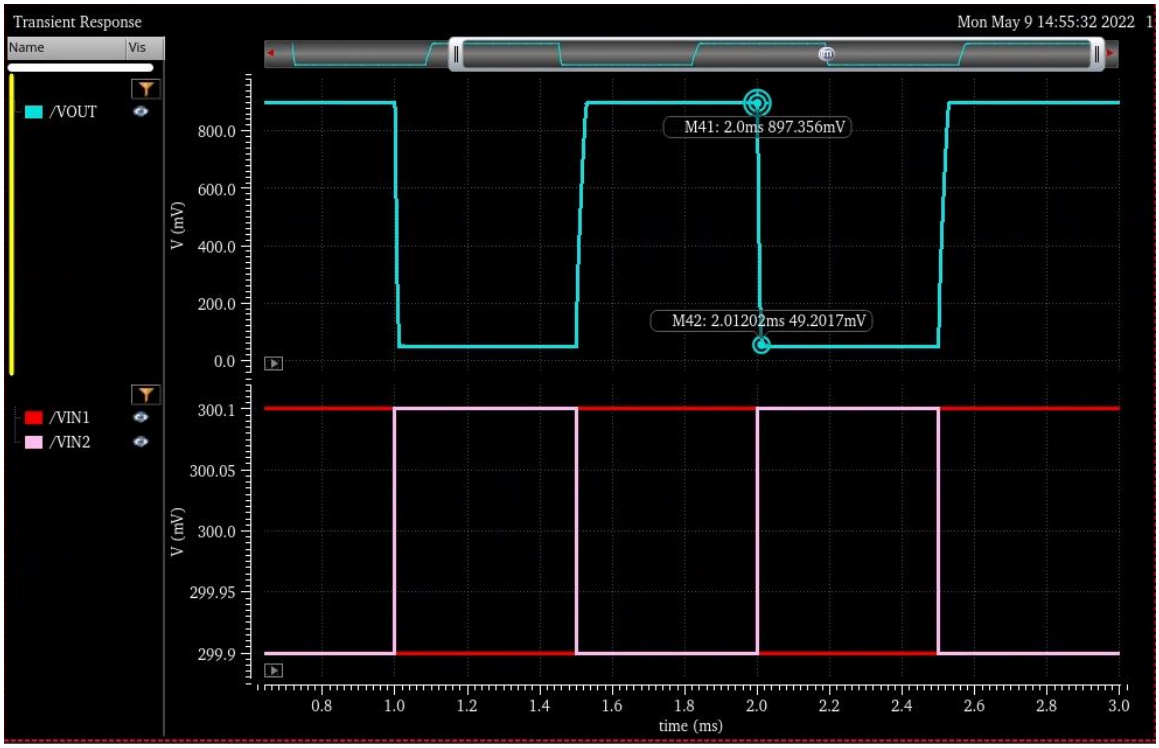


c. Slew Rate

The slew rate was determined using a transient analysis. Two differential pulses were applied to the differential inputs of the OTA, and the change in output voltage and time was measured. The input square wave was specified to have a rise and fall time of 1 fs such that the behavior would mimic an ideal square wave. The frequency of the input square wave was specified to be 1 kHz, with an amplitude of 100 µV. The input and output plots are shown below for this analysis.

Calculating the slew rate, it was found to be 70.65 kV/s, as shown below.

$$Slew\ Rate = \frac{V_{Max} - V_{Min}}{t_{Max} - t_{Min}} = \frac{897\ mV - 49.2\ mV}{2.012\ us - 2.000\ us} = \quad 70.65 * 10^3 \frac{V}{s} \quad = \quad 70.65 \frac{kV}{s}$$



d. Power Consumption

The power consumption of the folded cascode OTA was determined through a DC analysis of the current passed through the VDD source. As shown to the left, the DC power consumption was found to be 143.5 µW. This value was within the specified value of 200 µW.