ECE-GY 6443 – VLSI System Design and Architecture

Project 1: 8-Bit ALU / Sub-Component Timing Vs Area and Power

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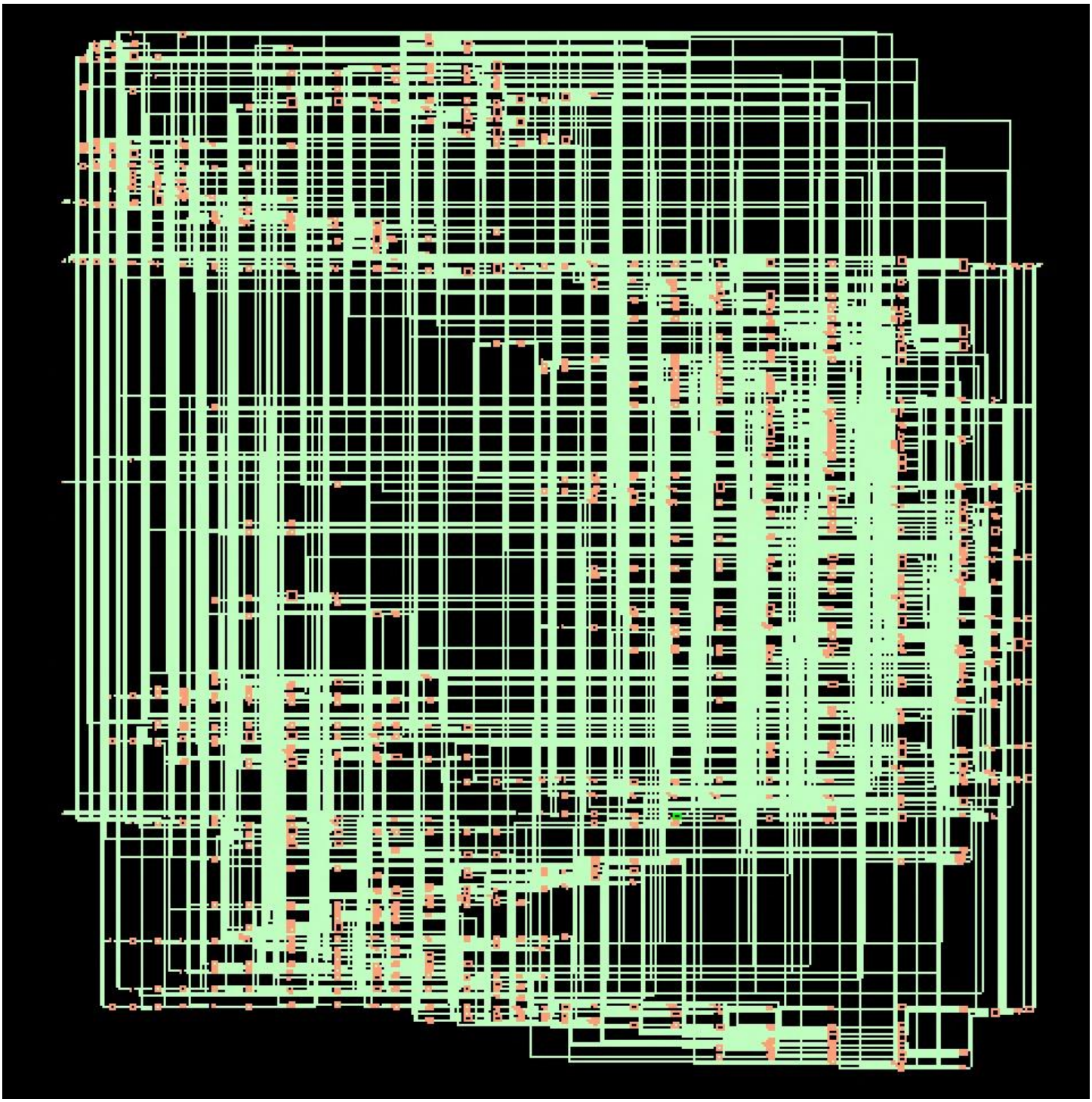
Project Contents: (See Folder)

1) Area Report Folder – Contains Supporting Area Reports
2) Power Report Folder – Contains Supporting Power Reports
3) Timing Report Folder – Contains Supporting Timing Reports
4) Schematic Folder – Contains Images of Schematics Simulated
5) Verilog Files Folder – Contains Verilog and Example SDC files

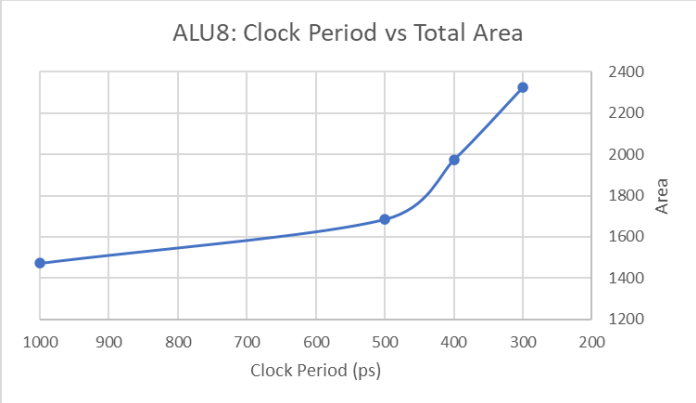
Project Part I :

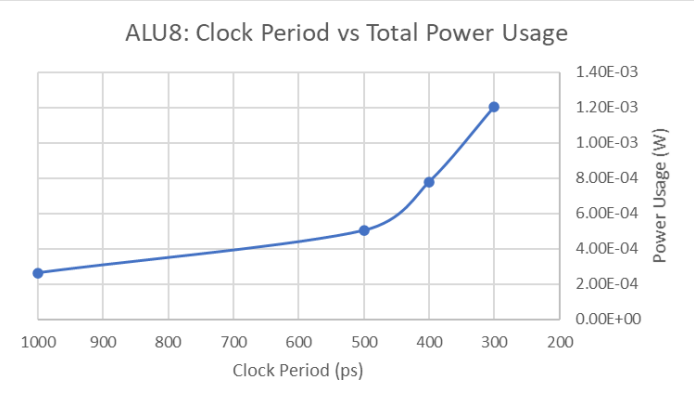
I. Synthesizing the 8-Bit ALU, Smallest Cycle Time

To synthesize and simulate the ALU, the clock constraints file was modified to determine the smallest possible cycle time. The first constraint was set with the clock period to 1 nanosecond, and the input and output delays were fixed to 15 picoseconds. For each synthesis, once the constraints file was set, the HDL and SDC files were read. The ALU was then optimized and mapped using the GENUS TCL commands. After successful completion of these commands, the reports for the area, power, and timing were obtained. If the timing report showed that there were no violated paths during this optimization, the clock cycle constraint was further reduced.



II. Synthesized 8-Bit ALU Plots





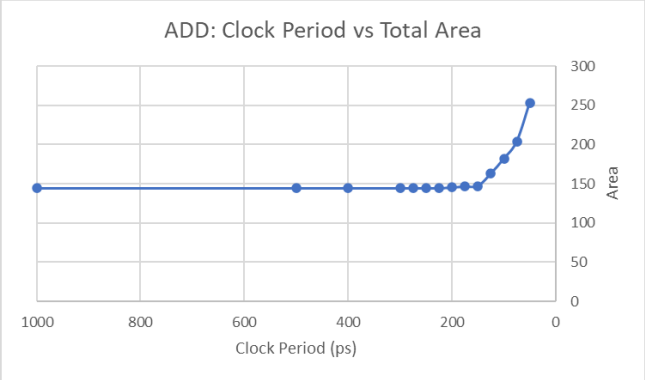
ALU8	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	1471.775	13.66%	84.20%	2.13%	3.720E-06	1.407E-04	1.192E-04	2.637E-04
500	0	1685.487	12.35%	85.42%	2.24%	3.833E-06	2.402E-04	2.601E-04	5.041E-04
400	0	1975.16	10.73%	87.47%	1.80%	4.622E-06	3.676E-04	4.067E-04	7.790E-04
300	2	2327.38	10.09%	88.36%	1.56%	5.541E-06	5.639E-04	6.344E-04	1.204E-03

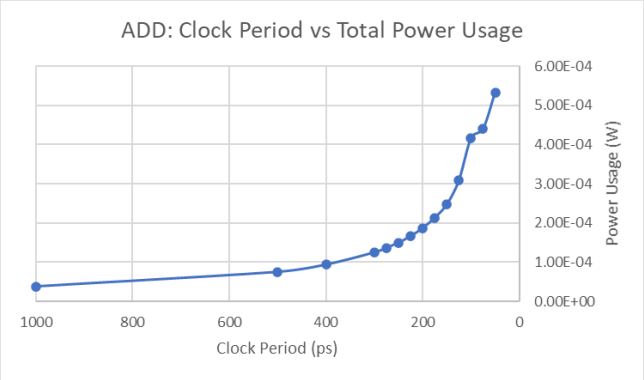
As shown in the two plots above, the area and power usage of the 8-Bit ALU were determined per cycle time. The minimum cycle time which did not violate any timing constraints was found to be 400 ps. The next smallest cycle time, which was 300 ps, gave two path violations with respect to timing constraints. The table above shows the parameters which were obtained for each of the varying cycle times. Some trends which can be seen from the data are that the switching power consumption increases with the clock period decrease, which is expected as decreasing the clock period will increase the number of switches per second, increasing the consumed power. Leakage and internal power consumption also increase with faster clock speeds, but at a rate lower than the switching power consumption increase. Another trend which can be seen is that the total area of the synthesized module increased as the clock period was decreased. This may be because more paths for the clock signal must be created to accommodate a faster speed, resulting in an increased module footprint. The module power usage by category has stayed more or less consistent, as each synthesis is holistic and may provide slightly different register, logic, and clock usage percentages.

III. Synthesizing each Functional Unit

Next, each of the submodules within the ALU were synthesized and timed independently. The submodules within the ALU included the ADD, SUB, MUL, DIV, SHL, SLR, ROL, ROR, AND, OR, XOR, NOR, NAND, XNOR, EQ, and GREAT operations. All operations were suited for 8-Bit vectors, and modules which were more or less identical in the vector operations (such as SHL/SHR and ROR/ROL) had similar or identical timing constraint data. The area and power consumption for each of these modules, along with the data obtained at each clock period constraint are given below.

a. 8-Bit ADD

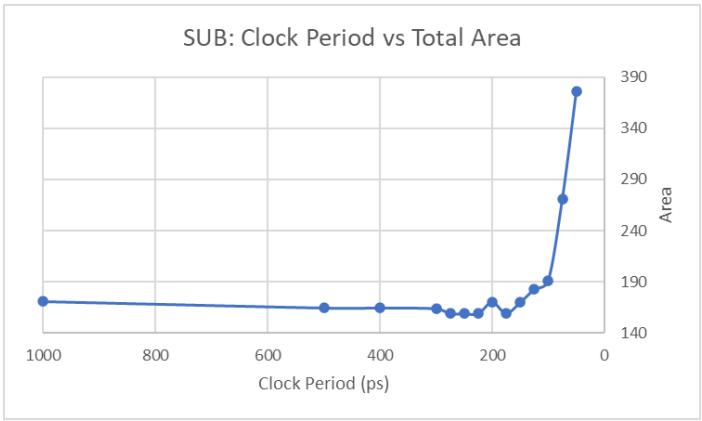


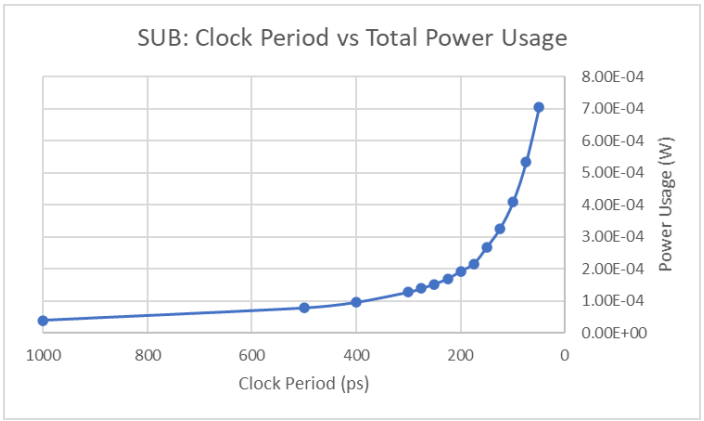


ADD	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	144.343	57.72%	33.76%	8.52%	3.16E-07	2.63E-05	1.09E-05	3.76E-05
500	0	144.343	57.78%	33.67%	8.55%	3.16E-07	5.27E-05	2.19E-05	7.49E-05
400	0	144.343	57.79%	33.65%	8.56%	3.16E-07	6.59E-05	2.73E-05	9.35E-05
300	0	144.343	57.81%	33.63%	8.57%	3.16E-07	8.78E-05	3.64E-05	1.25E-04
275	0	144.343	57.89%	33.56%	8.58%	3.16E-07	9.57E-05	3.97E-05	1.36E-04
250	0	144.343	57.81%	33.61%	8.57%	3.16E-07	1.05E-04	4.37E-05	1.49E-04
225	0	144.343	57.82%	33.61%	8.57%	3.16E-07	1.17E-04	4.86E-05	1.66E-04
200	0	145.257	57.75%	33.69%	8.57%	3.25E-07	1.32E-04	5.44E-05	1.87E-04
175	0	146.728	58.57%	32.85%	8.58%	3.22E-07	1.50E-04	6.28E-05	2.13E-04
150	0	147.265	58.43%	32.93%	8.63%	3.15E-07	1.75E-04	7.17E-05	2.47E-04
125	0	163.046	57.13%	34.58%	8.29%	3.69E-07	2.18E-04	9.01E-05	3.09E-04
100	0	181.99	56.76%	35.55%	7.69%	3.90E-07	2.87E-04	1.29E-04	4.16E-04
75	0	203.98	50.24%	42.29%	7.27%	4.44E-07	2.79E-04	1.61E-04	4.40E-04
50	10	253.147	45.47%	48.64%	5.89%	6.61E-07	3.30E-04	2.03E-04	5.34E-04

The ADD operation was able to sustain clock periods down to 75 picoseconds. At 50 picoseconds, the ADD module exhibited 10 path violations, and inaccurate area and power consumption reports. It can be seen that the total area of the module is very consistent, as there is minimal logic within the ADD module which has been further optimized to take up the least amount of space. The power consumption exhibits an exponential increase as the clock period is decreased. This exponential increase is mostly due to the internal and switching power consumption, as the leakage power consumption stays mostly constant.

b. 8-Bit SUB

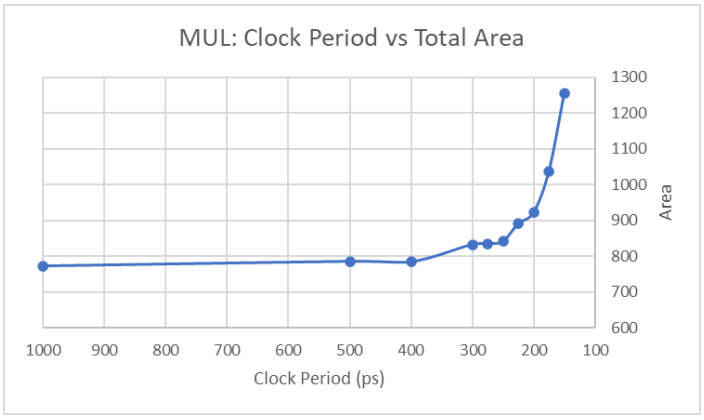


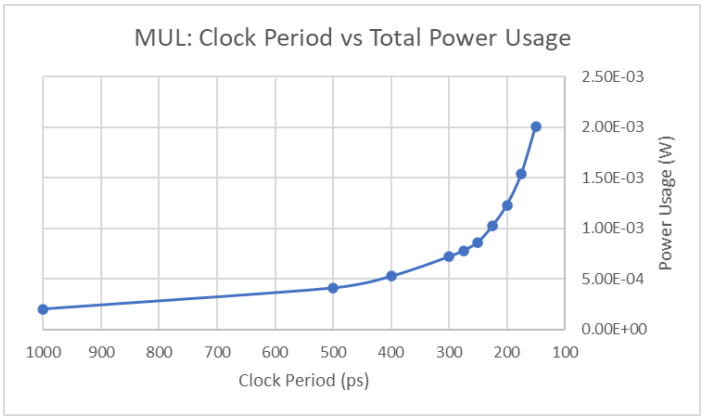


SUB	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	170.923	57.60%	34.10%	8.31%	3.47E-07	2.67E-05	1.15E-05	3.85E-05
500	0	164.625	57.52%	34.07%	8.41%	3.47E-07	5.43E-05	2.26E-05	7.73E-05
400	0	164.625	57.54%	34.04%	8.42%	3.47E-07	6.62E-05	2.85E-05	9.51E-05
300	0	163.893	57.53%	34.04%	8.43%	3.48E-07	8.86E-05	3.77E-05	1.27E-04
275	0	159.079	57.58%	33.99%	8.43%	3.38E-07	9.66E-05	4.12E-05	1.38E-04
250	0	159.079	57.53%	34.05%	8.42%	3.39E-07	1.06E-04	4.54E-05	1.52E-04
225	0	159.079	57.53%	34.04%	8.42%	3.39E-07	1.18E-04	5.05E-05	1.69E-04
200	0	170.191	57.27%	34.43%	8.30%	3.56E-07	1.35E-04	5.76E-05	1.93E-04
175	0	159.556	58.43%	33.11%	8.46%	3.38E-07	1.52E-04	6.39E-05	2.16E-04
150	0	170.017	55.19%	36.86%	7.96%	3.97E-07	1.86E-04	8.14E-05	2.68E-04
125	0	182.741	54.34%	37.80%	7.86%	4.05E-07	2.25E-04	1.01E-04	3.26E-04
100	0	191.237	52.31%	39.86%	7.83%	3.95E-07	2.75E-04	1.34E-04	4.09E-04
75	0	270.581	44.74%	49.59%	5.67%	6.57E-07	3.23E-04	2.09E-04	5.33E-04
50	17	375.68	36.93%	58.94%	4.12%	1.20E-06	3.77E-04	3.26E-04	7.04E-04

The minimum cycle time for the SUB module was found to be 100 picoseconds, after which the module exhibited 10 violated paths at a 50 picosecond clock period. Similarly to the ADD module, the SUB module shows an exponential increase in power consumption and exhibits erroneous area consumption once there are path violations due to timing constraints. The SUB module did consume more area than the ADD module, and due to this, the synthesizer may have been able to further optimize the area and cause some fluctuations in area per clock period, as visible in the area vs clock period graph.

c. 8-Bit MUL

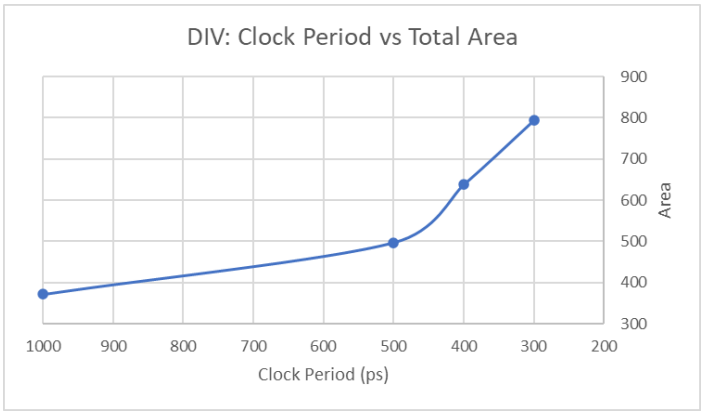


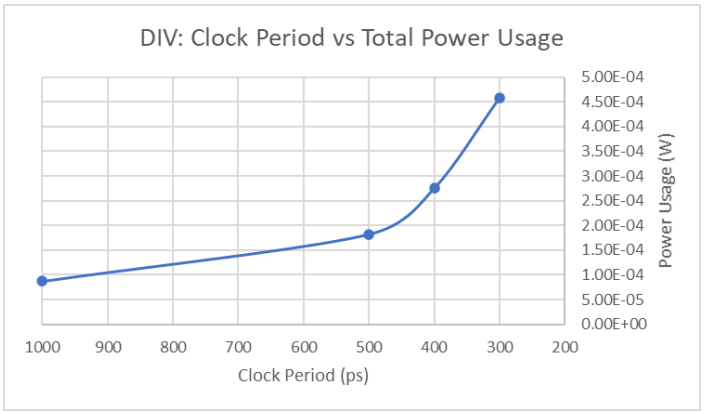


MUL	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	772.124	43.67%	52.01%	4.32%	1.82E-06	1.29E-04	7.40E-05	2.05E-04
500	0	784.868	42.97%	52.74%	4.28%	1.88E-06	2.60E-04	1.51E-04	4.12E-04
400	0	783.57	42.67%	53.14%	4.19%	1.92E-06	3.33E-04	1.92E-04	5.27E-04
300	0	832.466	42.74%	53.20%	4.06%	2.10E-06	4.55E-04	2.63E-04	7.20E-04
275	0	834.658	42.54%	53.37%	4.08%	2.04E-06	4.91E-04	2.88E-04	7.82E-04
250	0	841.019	41.78%	54.13%	4.10%	2.11E-06	5.38E-04	3.22E-04	8.63E-04
225	0	890.555	39.64%	56.55%	3.81%	2.31E-06	6.41E-04	3.80E-04	1.02E-03
200	0	921.877	38.44%	58.04%	3.52%	2.26E-06	7.46E-04	4.83E-04	1.23E-03
175	0	1037.472	35.71%	61.10%	3.20%	2.86E-06	9.34E-04	6.00E-04	1.54E-03
150	12	1254.522	31.04%	66.11%	2.85%	3.86E-06	1.16E-03	8.48E-04	2.01E-03

Since the logic for the MUL module was larger than the other modules, the MUL module was found to have a significantly larger footprint in terms of area consumption. The MUL module was able to have a minimum clock period of 175 ps before there were 16 path violations due to the timing constraint at 150 ps. The area is shown to increase as the clock period is decreased, which is peculiar in that other modules so very little or no increase. This may be due to the fact that this module has more logic to complete the operation than other modules, and the synthesized gates may need more clock paths to meet the stricter timing constraints, resulting in a larger area footprint.

d. 8-Bit DIV

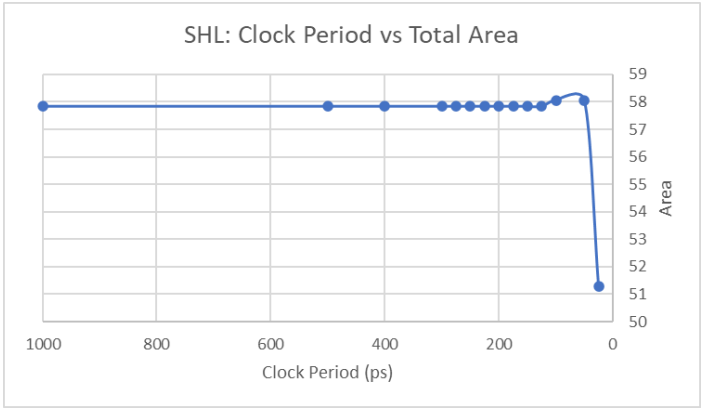


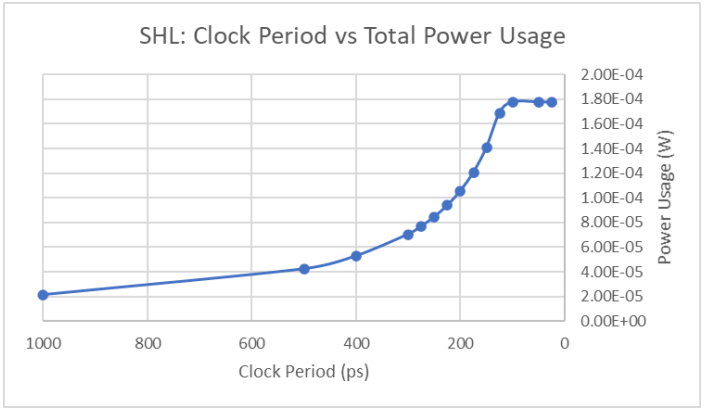


DIV	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	371.692	24.62%	72.25%	3.13%	8.73E-07	5.27E-05	3.36E-05	8.72E-05
500	0	497.433	19.01%	77.86%	3.12%	1.12E-06	9.49E-05	8.61E-05	1.82E-04
400	0	638.033	15.81%	81.60%	2.59%	1.58E-06	1.35E-04	1.38E-04	2.75E-04
300	2	793.88	13.41%	84.56%	2.03%	2.14E-06	2.22E-04	2.33E-04	4.57E-04

The DIV module, of all the modules tested within the ALU, had the least forgiving time constraints, as the module failed to meet the timing paths after 400 ps. The module exhibited a single path violation at 300 ps, and showed an increase in both power consumption and footprint area as the clock period was decreased.

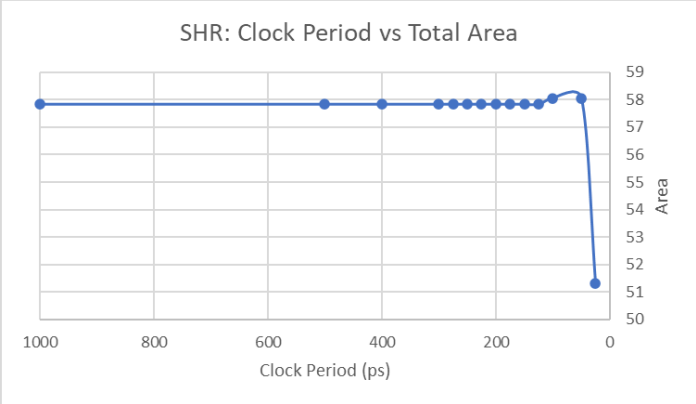
e. 8-Bit SHL

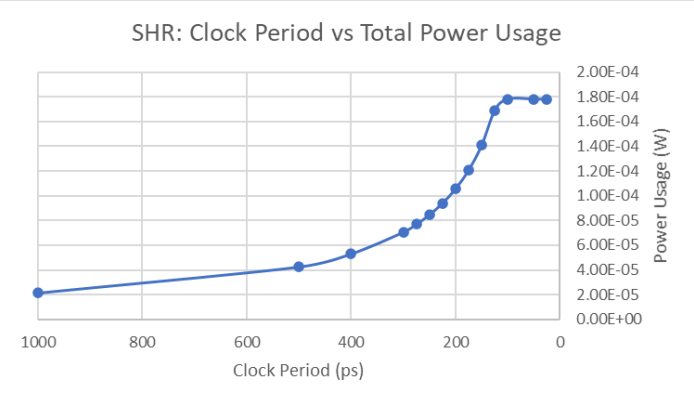




SHL	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	57.83	83.16%	5.15%	11.69%	2.185E-07	1.776E-05	3.320E-06	2.130E-05
500	0	57.83	83.08%	5.17%	11.75%	2.185E-07	3.552E-05	6.640E-06	4.238E-05
400	0	57.83	83.06%	5.18%	11.76%	2.185E-07	4.440E-05	8.301E-06	5.292E-05
300	0	57.83	83.04%	5.18%	11.78%	2.185E-07	5.920E-05	1.107E-05	7.049E-05
275	0	57.83	83.04%	5.18%	11.78%	2.185E-07	6.459E-05	1.207E-05	7.688E-05
250	0	57.83	83.03%	5.18%	11.78%	2.185E-07	7.105E-05	1.328E-05	8.454E-05
225	0	57.83	83.03%	5.19%	11.78%	2.185E-07	7.894E-05	1.476E-05	9.391E-05
200	0	57.83	83.03%	5.19%	11.79%	2.185E-07	8.881E-05	1.660E-05	1.056E-04
175	0	57.83	83.02%	5.19%	11.79%	2.185E-07	1.015E-04	1.897E-05	1.207E-04
150	0	57.83	83.02%	5.19%	11.79%	2.185E-07	1.184E-04	2.213E-05	1.408E-04
125	0	57.83	83.01%	5.19%	11.80%	2.185E-07	1.421E-04	2.656E-05	1.689E-04
100	0	58.055	76.19%	9.82%	13.99%	1.262E-07	1.405E-04	3.735E-05	1.779E-04
50	0	58.055	76.19%	9.82%	13.99%	1.262E-07	1.405E-04	3.735E-05	1.779E-04
25	14	51.298	76.24%	9.74%	14.02%	1.704E-07	1.368E-04	4.067E-05	1.776E-04

f. 8-Bit SHR



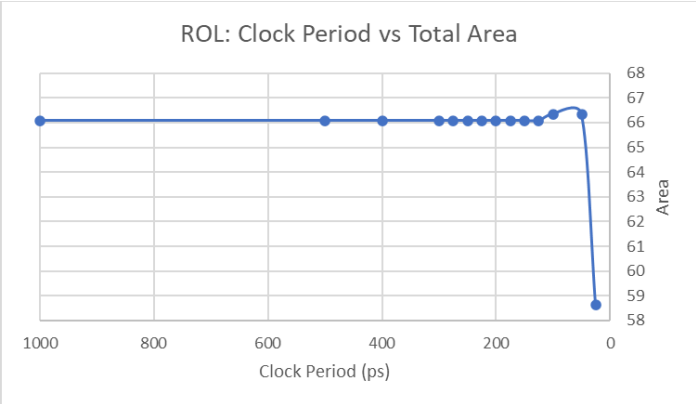


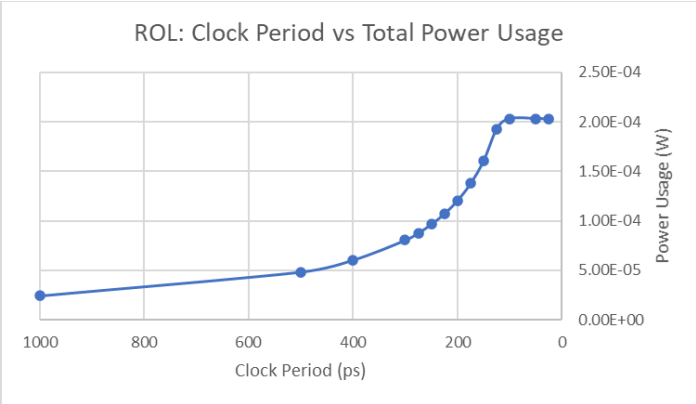
SHR	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	57.83	83.16%	5.15%	11.69%	2.185E-07	1.776E-05	3.320E-06	2.130E-05
500	0	57.83	83.08%	5.17%	11.75%	2.185E-07	3.552E-05	6.640E-06	4.238E-05
400	0	57.83	83.06%	5.18%	11.76%	2.185E-07	4.440E-05	8.301E-06	5.292E-05
300	0	57.83	83.04%	5.18%	11.78%	2.185E-07	5.920E-05	1.107E-05	7.049E-05
275	0	57.83	83.04%	5.18%	11.78%	2.185E-07	6.459E-05	1.207E-05	7.688E-05
250	0	57.83	83.03%	5.18%	11.78%	2.185E-07	7.105E-05	1.328E-05	8.454E-05
225	0	57.83	83.03%	5.19%	11.78%	2.185E-07	7.894E-05	1.476E-05	9.391E-05
200	0	57.83	83.03%	5.19%	11.79%	2.185E-07	8.881E-05	1.660E-05	1.056E-04
175	0	57.83	83.02%	5.19%	11.79%	2.185E-07	1.015E-04	1.897E-05	1.207E-04
150	0	57.83	83.02%	5.19%	11.79%	2.185E-07	1.184E-04	2.213E-05	1.408E-04
125	0	57.83	83.01%	5.19%	11.80%	2.185E-07	1.421E-04	2.656E-05	1.689E-04
100	0	58.055	76.19%	9.82%	13.99%	1.262E-07	1.405E-04	3.735E-05	1.779E-04
50	0	58.055	76.19%	9.82%	13.99%	1.262E-07	1.405E-04	3.735E-05	1.779E-04
25	14	51.298	76.24%	9.74%	14.02%	1.704E-07	1.368E-04	4.067E-05	1.776E-04

The SHL and SHR modules showed identical area and power consumptions, as their operations are inherently similar. Both modules were able to meet timing constraints up to 50 ps, after which they had 14 path violations at 25 ps. The area consumption for both modules stayed more or less consistent, as the

power consumption increased as the clock period was decreased. However, both modules showed no power increase at between 100 ps and 50 ps clock periods, as the synthesizer may have found a clock path which was able to satisfy both 100 ps and 50 ps without change.

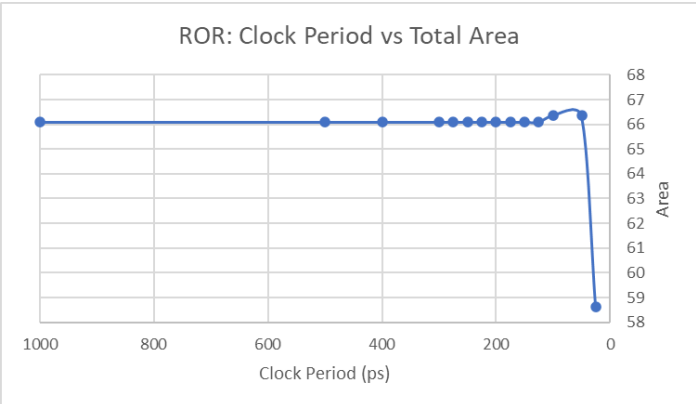
g. 8-Bit ROL

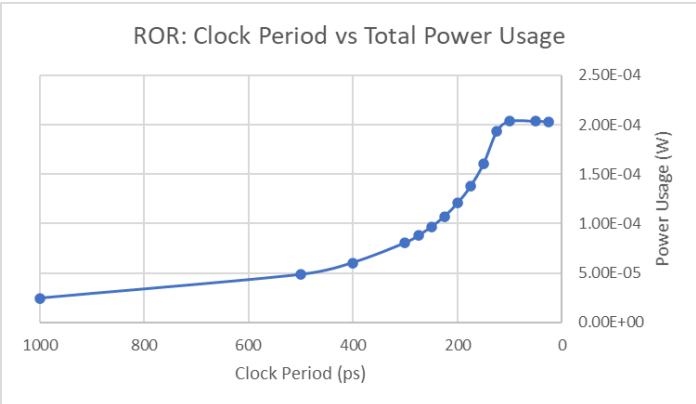




ROL	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	66.091	83.16%	5.15%	11.69%	2.498E-07	2.030E-05	3.795E-06	2.434E-05
500	0	66.091	83.08%	5.17%	11.75%	2.498E-07	4.060E-05	7.589E-06	4.844E-05
400	0	66.091	83.06%	5.18%	11.76%	2.498E-07	5.075E-05	9.486E-06	6.048E-05
300	0	66.091	83.04%	5.18%	11.78%	2.498E-07	6.766E-05	1.265E-05	8.056E-05
275	0	66.091	83.04%	5.18%	11.78%	2.498E-07	7.381E-05	1.380E-05	8.786E-05
250	0	66.091	83.03%	5.18%	11.78%	2.498E-07	8.119E-05	1.518E-05	9.662E-05
225	0	66.091	83.03%	5.19%	11.78%	2.498E-07	9.022E-05	1.686E-05	1.073E-04
200	0	66.091	83.03%	5.19%	11.79%	2.498E-07	1.015E-04	1.897E-05	1.207E-04
175	0	66.091	83.02%	5.19%	11.79%	2.498E-07	1.160E-04	2.168E-05	1.379E-04
150	0	66.091	83.02%	5.19%	11.79%	2.498E-07	1.353E-04	2.530E-05	1.609E-04
125	0	66.091	83.01%	5.19%	11.80%	2.498E-07	1.624E-04	3.036E-05	1.930E-04
100	0	66.349	76.19%	9.82%	13.99%	1.442E-07	1.605E-04	4.269E-05	2.034E-04
50	0	66.349	76.19%	9.82%	13.99%	1.442E-07	1.605E-04	4.269E-05	2.034E-04
25	16	58.626	76.24%	9.74%	14.02%	1.948E-07	1.563E-04	4.648E-05	2.030E-04

h. 8-Bit ROR

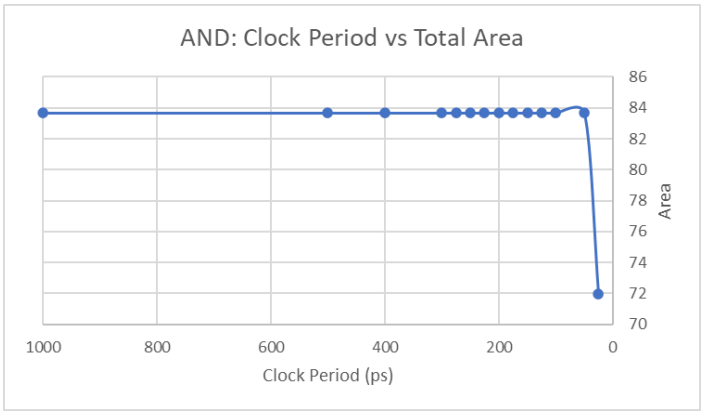


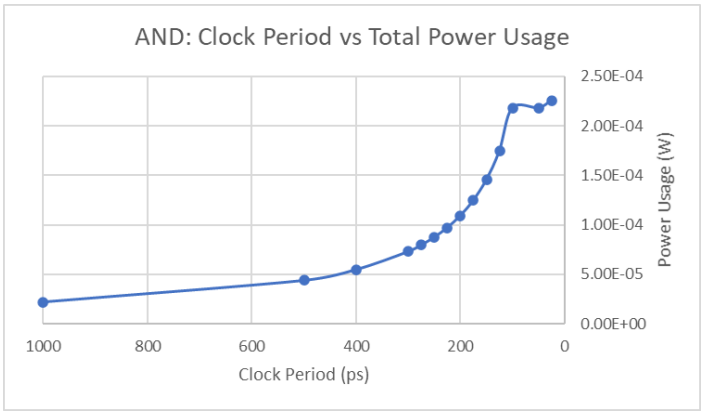


ROR	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	66.091	83.16%	5.15%	11.69%	2.498E-07	2.030E-05	3.795E-06	2.434E-05
500	0	66.091	83.08%	5.17%	11.75%	2.498E-07	4.060E-05	7.589E-06	4.844E-05
400	0	66.091	83.06%	5.18%	11.76%	2.498E-07	5.075E-05	9.486E-06	6.048E-05
300	0	66.091	83.04%	5.18%	11.78%	2.498E-07	6.766E-05	1.265E-05	8.056E-05
275	0	66.091	83.04%	5.18%	11.78%	2.498E-07	7.381E-05	1.380E-05	8.786E-05
250	0	66.091	83.03%	5.18%	11.78%	2.498E-07	8.119E-05	1.518E-05	9.662E-05
225	0	66.091	83.03%	5.19%	11.78%	2.498E-07	9.022E-05	1.686E-05	1.073E-04
200	0	66.091	83.03%	5.19%	11.79%	2.498E-07	1.015E-04	1.897E-05	1.207E-04
175	0	66.091	83.02%	5.19%	11.79%	2.498E-07	1.160E-04	2.168E-05	1.379E-04
150	0	66.091	83.02%	5.19%	11.79%	2.498E-07	1.353E-04	2.530E-05	1.609E-04
125	0	66.091	83.01%	5.19%	11.80%	2.498E-07	1.624E-04	3.036E-05	1.930E-04
100	0	66.349	76.19%	9.82%	13.99%	1.442E-07	1.605E-04	4.269E-05	2.034E-04
50	0	66.349	76.19%	9.82%	13.99%	1.442E-07	1.605E-04	4.269E-05	2.034E-04
25	16	58.626	76.24%	9.74%	14.02%	1.948E-07	1.563E-04	4.648E-05	2.030E-04

Both the ROL and ROR modules shows the same area, time, and power usage characteristics. They both were able to synthesize without failed paths until 50 ps, after which they both had 16 path violations. The area for both modules stayed consistent throughout all the time constraints, meaning that the synthesizer had found the most optimized layout for these two modules. The power consumption increased as expected when the clock period was decreased for both of the modules.

i. 8-Bit AND

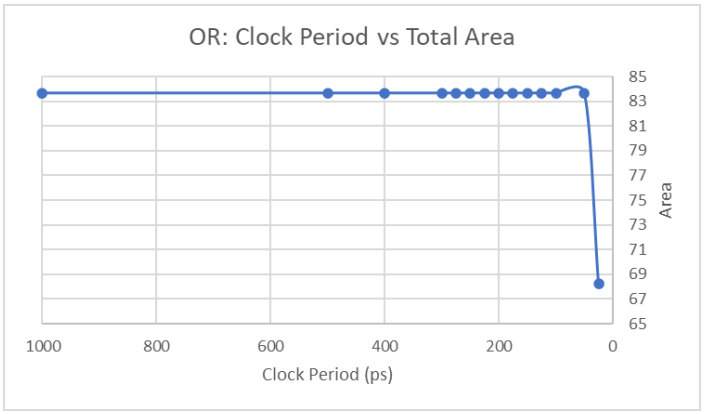


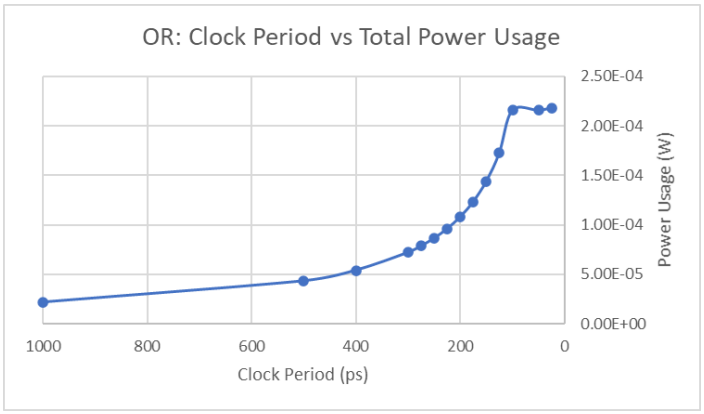


AND	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	83.66	72.46%	14.57%	12.97%	1.392E-07	1.688E-05	4.933E-06	2.195E-05
500	0	83.66	72.44%	14.55%	13.01%	1.392E-07	3.376E-05	9.866E-06	4.376E-05
400	0	83.66	72.44%	14.55%	13.01%	1.392E-07	4.219E-05	1.233E-05	5.467E-05
300	0	83.66	72.43%	14.54%	13.02%	1.392E-07	5.626E-05	1.644E-05	7.284E-05
275	0	83.66	72.43%	14.54%	13.03%	1.392E-07	6.137E-05	1.794E-05	7.945E-05
250	0	83.66	72.43%	14.54%	13.03%	1.392E-07	6.751E-05	1.973E-05	8.738E-05
225	0	83.66	72.43%	14.54%	13.03%	1.392E-07	7.501E-05	2.192E-05	9.708E-05
200	0	83.66	72.43%	14.54%	13.03%	1.392E-07	8.439E-05	2.466E-05	1.092E-04
175	0	83.66	72.43%	14.54%	13.03%	1.392E-07	9.645E-05	2.819E-05	1.248E-04
150	0	83.66	72.43%	14.54%	13.04%	1.392E-07	1.125E-04	3.289E-05	1.455E-04
125	0	83.66	72.43%	14.53%	13.04%	1.392E-07	1.350E-04	3.946E-05	1.746E-04
100	0	83.66	72.43%	14.53%	13.04%	1.392E-07	1.688E-04	4.933E-05	2.182E-04
50	0	83.66	72.43%	14.53%	13.04%	1.392E-07	1.688E-04	4.933E-05	2.182E-04
25	16	71.947	69.93%	17.46%	12.61%	2.018E-07	1.652E-04	6.024E-05	2.257E-04

The AND module implements a small amount of logic and therefore has a more consistent total area when decreasing the clock time constraint. The total power consumption continuously increases exponentially until the final plot constraint of 50 picoseconds after which that's power consumption stagnates and violate 16 paths at a clock constraint of 25 picoseconds. The area stays the same because the synthesizer has optimized the module to the point where the size cannot be decreased any further regardless of the clock speed.

j. 8-Bit OR

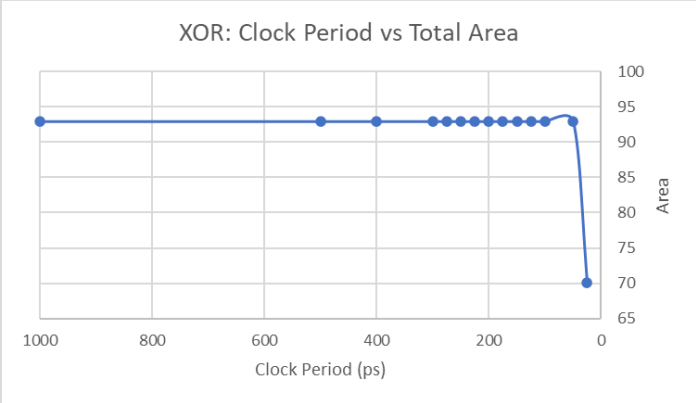


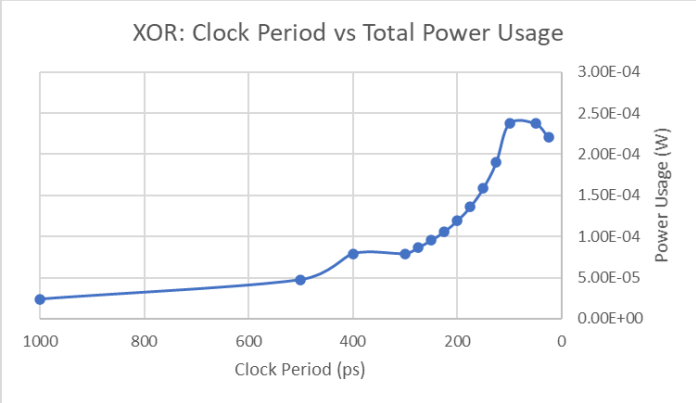


OR	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	83.66	73.57%	13.32%	13.11%	1.344E-07	1.683E-05	4.743E-06	2.170E-05
500	0	83.66	73.53%	13.32%	13.15%	1.344E-07	3.365E-05	9.486E-06	4.327E-05
400	0	83.66	73.52%	13.32%	13.16%	1.344E-07	4.207E-05	1.186E-05	5.406E-05
300	0	83.66	73.51%	13.32%	13.17%	1.344E-07	5.609E-05	1.581E-05	7.203E-05
275	0	83.66	73.51%	13.32%	13.17%	1.344E-07	6.119E-05	1.725E-05	7.857E-05
250	0	83.66	73.51%	13.32%	13.17%	1.344E-07	6.730E-05	1.897E-05	8.641E-05
225	0	83.66	73.51%	13.32%	13.18%	1.344E-07	7.478E-05	2.108E-05	9.600E-05
200	0	83.66	73.50%	13.32%	13.18%	1.344E-07	8.413E-05	2.372E-05	1.080E-04
175	0	83.66	73.50%	13.32%	13.18%	1.344E-07	9.615E-05	2.710E-05	1.234E-04
150	0	83.66	73.50%	13.32%	13.18%	1.344E-07	1.122E-04	3.162E-05	1.439E-04
125	0	83.66	73.50%	13.32%	13.18%	1.344E-07	1.346E-04	3.795E-05	1.727E-04
100	0	83.66	73.50%	13.32%	13.19%	1.344E-07	1.683E-04	4.743E-05	2.158E-04
50	0	83.66	73.50%	13.32%	13.19%	1.344E-07	1.683E-04	4.743E-05	2.158E-04
25	16	68.215	72.41%	14.55%	13.04%	1.787E-07	1.631E-04	5.502E-05	2.183E-04

Applying time constraints to the OR module has given results almost identical to the AND module where the total area is consistent, and the total power consumption increases exponentially before stagnating near the minimum clock speed.

k. 8-Bit XOR

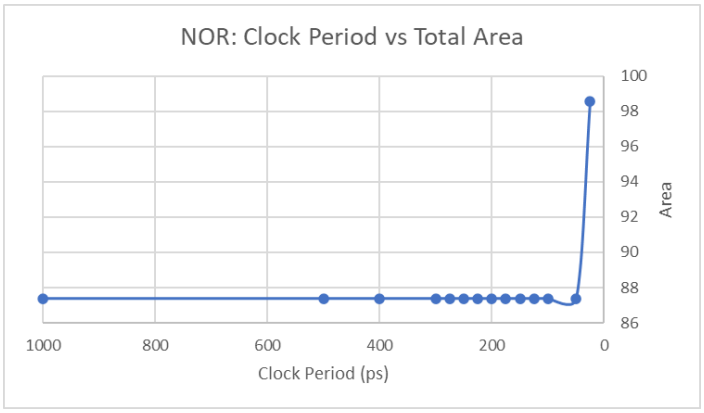


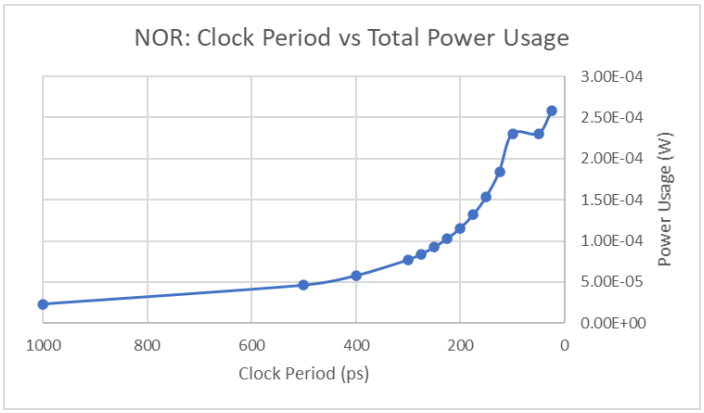


XOR	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	92.991	69.16%	18.96%	11.89%	1.892E-07	1.813E-05	5.621E-06	2.394E-05
500	0	92.991	69.19%	18.88%	11.94%	1.892E-07	3.626E-05	1.124E-05	4.769E-05
400	0	92.991	69.20%	18.84%	11.95%	1.892E-07	6.043E-05	1.874E-05	7.935E-05
300	0	92.991	69.20%	18.84%	11.95%	1.892E-07	6.043E-05	1.874E-05	7.935E-05
275	0	92.991	69.20%	18.84%	11.96%	1.892E-07	6.592E-05	2.044E-05	8.655E-05
250	0	92.991	69.20%	18.84%	11.96%	1.892E-07	7.251E-05	2.248E-05	9.519E-05
225	0	92.991	69.21%	18.83%	11.96%	1.892E-07	8.057E-05	2.498E-05	1.057E-04
200	0	92.991	69.21%	18.83%	11.96%	1.892E-07	9.064E-05	2.810E-05	1.189E-04
175	0	92.991	69.21%	18.82%	11.97%	1.892E-07	1.036E-04	3.212E-05	1.359E-04
150	0	92.991	69.21%	18.82%	11.97%	1.892E-07	1.209E-04	3.747E-05	1.585E-04
125	0	92.991	69.21%	18.82%	11.97%	1.892E-07	1.450E-04	4.497E-05	1.902E-04
100	0	92.991	69.21%	18.81%	11.97%	1.892E-07	1.813E-04	5.621E-05	2.377E-04
50	0	92.991	69.21%	18.81%	11.97%	1.892E-07	1.813E-04	5.621E-05	2.377E-04
25	16	70.081	74.38%	12.74%	12.88%	1.848E-07	1.703E-04	5.052E-05	2.210E-04

The XOR module exhibits an exponential increase in power consumption besides a single anomaly at a 400 picoseconds clock time constraint where the synthesizer may have holistically changed the module and increased the internal power consumption. This module had a maximum clock constraint of 50 picoseconds before 16 paths were violated at a 25 picosecond clock period.

l. 8-Bit NOR

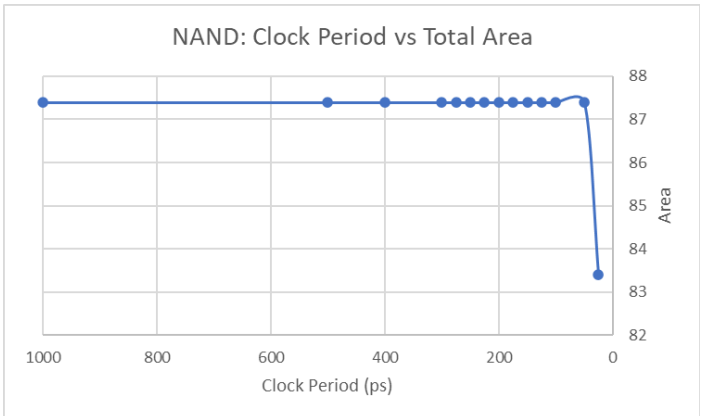


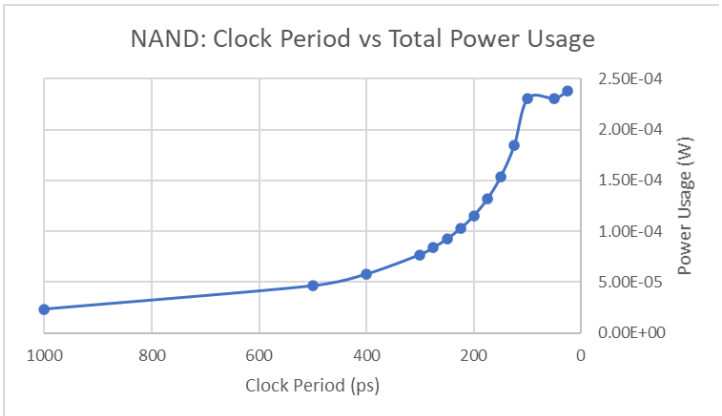


NOR	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	87.393	68.35%	19.40%	12.25%	1.931E-07	1.811E-05	4.933E-06	2.324E-05
500	0	87.393	68.40%	19.30%	12.30%	1.931E-07	3.623E-05	9.866E-06	4.629E-05
400	0	87.393	68.41%	19.28%	12.31%	1.931E-07	4.529E-05	1.233E-05	5.781E-05
300	0	87.393	68.42%	19.26%	12.32%	1.931E-07	6.038E-05	1.644E-05	7.702E-05
275	0	87.393	68.42%	19.26%	12.32%	1.931E-07	6.587E-05	1.794E-05	8.400E-05
250	0	87.393	68.43%	19.25%	12.32%	1.931E-07	7.246E-05	1.973E-05	9.238E-05
225	0	87.393	68.43%	19.25%	12.33%	1.931E-07	8.051E-05	2.192E-05	1.026E-04
200	0	87.393	68.43%	19.24%	12.33%	1.931E-07	9.057E-05	2.466E-05	1.154E-04
175	0	87.393	68.43%	19.24%	12.33%	1.931E-07	1.035E-04	2.819E-05	1.319E-04
150	0	87.393	68.44%	19.23%	12.33%	1.931E-07	1.208E-04	3.289E-05	1.538E-04
125	0	87.393	68.44%	19.23%	12.34%	1.931E-07	1.449E-04	3.946E-05	1.846E-04
100	0	87.393	68.44%	19.22%	12.34%	1.931E-07	1.811E-04	4.933E-05	2.307E-04
50	0	87.393	68.44%	19.22%	12.34%	1.931E-07	1.811E-04	4.933E-05	2.307E-04
25	16	98.59	61.21%	27.76%	11.03%	3.917E-07	1.731E-04	8.443E-05	2.579E-04

The NOR module showed close to identical parameters in terms of area consumption when compared to the ADD module. Similarly, it could bear a minimum clock period of up to 50 ps after which it started to have violating paths at 25 ps. As there is a decrease in clock period, there's a substantial increase in power consumption due to the internal and switching power required at higher speed.

m. 8-Bit NAND

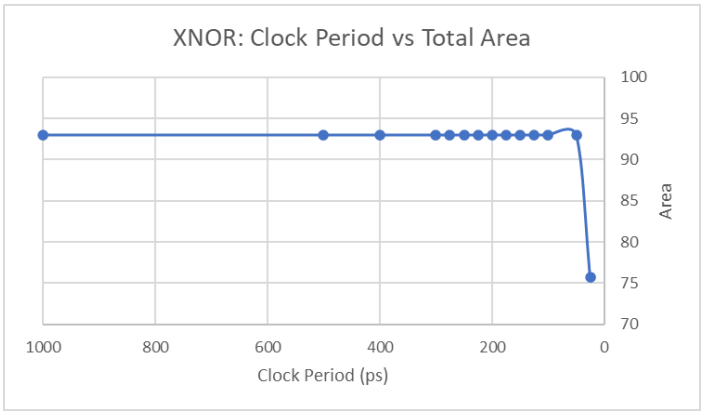


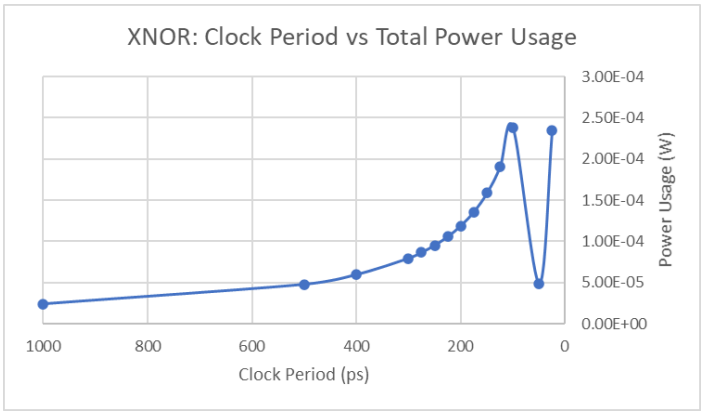


NAND	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	87.393	68.52%	19.22%	12.25%	1.951E-07	1.810E-05	4.933E-06	2.323E-05
500	0	87.393	68.56%	19.13%	12.31%	1.951E-07	3.619E-05	9.866E-06	4.626E-05
400	0	87.393	68.57%	19.12%	12.32%	1.951E-07	4.524E-05	1.233E-05	5.777E-05
300	0	87.393	68.58%	19.10%	12.33%	1.951E-07	6.032E-05	1.644E-05	7.696E-05
275	0	87.393	68.58%	19.09%	12.33%	1.951E-07	6.581E-05	1.794E-05	8.394E-05
250	0	87.393	68.58%	19.09%	12.33%	1.951E-07	7.239E-05	1.973E-05	9.232E-05
225	0	87.393	68.58%	19.09%	12.33%	1.951E-07	8.043E-05	2.192E-05	1.026E-04
200	0	87.393	68.58%	19.08%	12.34%	1.951E-07	9.049E-05	2.466E-05	1.153E-04
175	0	87.393	68.58%	19.08%	12.34%	1.951E-07	1.034E-04	2.819E-05	1.318E-04
150	0	87.393	68.59%	19.07%	12.34%	1.951E-07	1.206E-04	3.289E-05	1.537E-04
125	0	87.393	68.59%	19.07%	12.34%	1.951E-07	1.448E-04	3.946E-05	1.844E-04
100	0	87.393	68.59%	19.07%	12.34%	1.951E-07	1.810E-04	4.933E-05	2.305E-04
50	0	87.393	68.59%	19.06%	12.34%	1.951E-07	1.810E-04	4.933E-05	2.305E-04
25	16	83.402	66.41%	21.63%	11.96%	2.577E-07	1.694E-04	6.830E-05	2.380E-04

The 8-bit NAND module exhibited identical behavior to the NOR module. The area consumption is also similar, where the clock can sustain a minimum of 50 ps. A total of 16 path violations were found between when the clock constraint was set to 25 ps. Likewise, the reason for the substantial increase in total power is due to an increase of internal and switching power whereas leakage power consumption is consistent throughout.

n. 8-Bit XNOR

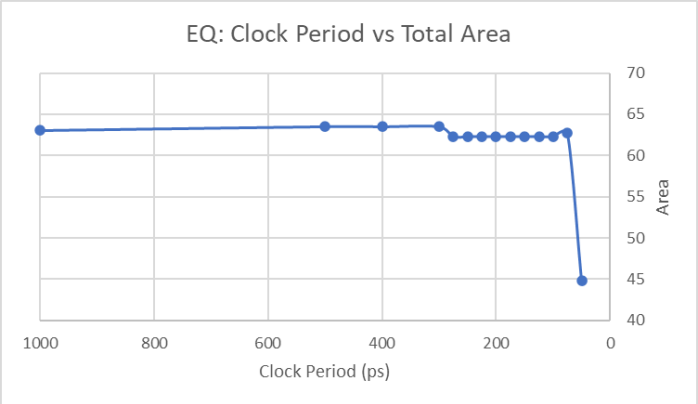


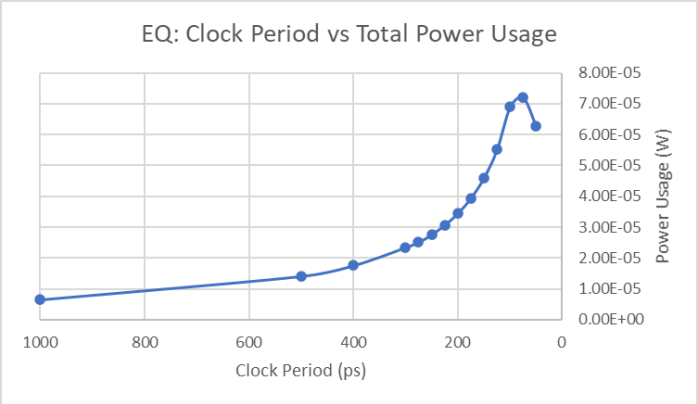


XNOR	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	92.991	69.17%	18.95%	11.89%	1.883E-07	1.813E-05	5.621E-06	2.394E-05
500	0	92.991	69.20%	18.87%	11.94%	1.883E-07	3.626E-05	1.124E-05	4.769E-05
400	0	92.991	69.20%	18.85%	11.95%	1.883E-07	4.532E-05	1.405E-05	5.956E-05
300	0	92.991	69.21%	18.84%	11.95%	1.883E-07	6.043E-05	1.874E-05	7.935E-05
275	0	92.991	69.21%	18.83%	11.96%	1.883E-07	6.592E-05	2.044E-05	8.655E-05
250	0	92.991	69.21%	18.83%	11.96%	1.883E-07	2.248E-05	2.248E-05	9.519E-05
225	0	92.991	69.21%	18.82%	11.96%	1.883E-07	8.057E-05	2.498E-05	1.057E-04
200	0	92.991	69.22%	18.82%	11.96%	1.883E-07	9.064E-05	2.810E-05	1.189E-04
175	0	92.991	69.22%	18.82%	11.97%	1.883E-07	1.036E-04	3.212E-05	1.359E-04
150	0	92.991	69.22%	18.81%	11.97%	1.883E-07	1.209E-04	3.747E-05	1.585E-04
125	0	92.991	69.22%	18.81%	11.97%	1.883E-07	1.450E-04	4.497E-05	1.902E-04
100	0	92.991	69.22%	18.81%	11.97%	1.883E-07	1.813E-04	5.621E-05	2.377E-04
50	0	92.991	69.89%	18.44%	11.67%	1.961E-07	3.735E-05	1.124E-05	4.879E-05
25	16	75.68	70.08%	17.76%	12.16%	2.349E-07	1.763E-04	5.763E-05	2.341E-04

The XNOR module was found to have identical area and power characteristics when compared to the XOR module. The minimum time constraint at which the module exhibited no violated paths was found to be 50 picoseconds. Once the time constraint was set to 25 picoseconds, 16 paths were violated, and both the area and total power consumption decreased erroneously.

o. 8-Bit EQ

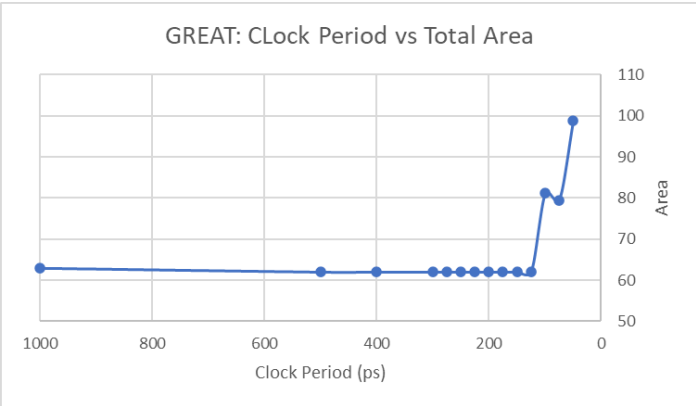


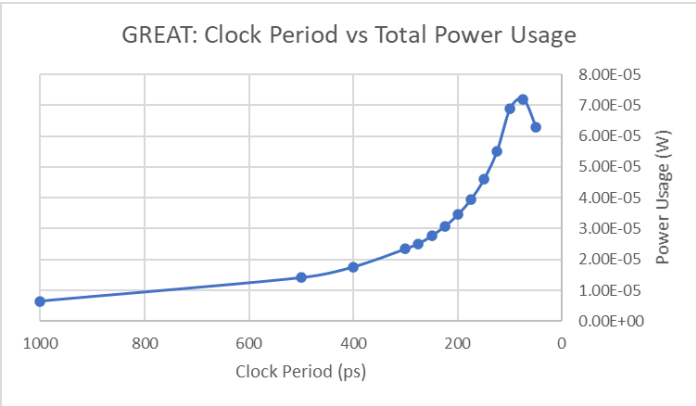


EQ	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	63.054	23.62%	71.80%	4.58%	7.529E-08	3.480E-06	2.915E-06	6.470E-06
500	0	63.521	23.81%	71.14%	5.05%	9.645E-08	7.874E-06	6.120E-06	1.409E-05
400	0	63.521	23.82%	71.12%	5.06%	9.645E-08	9.843E-06	7.650E-06	1.759E-05
300	0	63.521	23.84%	71.10%	5.06%	9.645E-08	1.312E-05	1.020E-05	2.342E-05
275	0	62.322	24.22%	70.64%	5.15%	9.329E-08	1.423E-05	1.082E-05	2.514E-05
250	0	62.322	24.22%	70.63%	5.15%	9.329E-08	1.565E-05	1.190E-05	2.765E-05
225	0	62.322	24.23%	70.62%	5.15%	9.329E-08	1.739E-05	1.322E-05	3.071E-05
200	0	62.322	24.23%	70.62%	5.15%	9.329E-08	1.956E-05	1.488E-05	3.453E-05
175	0	62.322	24.23%	70.61%	5.15%	9.329E-08	2.236E-05	1.700E-05	3.945E-05
150	0	62.322	24.23%	70.61%	5.15%	9.329E-08	2.608E-05	1.984E-05	4.601E-05
125	0	62.322	24.24%	70.60%	5.16%	9.329E-08	3.130E-05	2.380E-05	5.520E-05
100	0	62.322	24.24%	70.60%	5.16%	9.329E-08	3.913E-05	2.976E-05	6.897E-05
75	0	62.737	21.17%	74.72%	4.11%	1.441E-07	4.234E-05	2.956E-05	7.205E-05
50	1	44.758	26.55%	67.79%	5.67%	1.366E-07	3.216E-05	3.050E-05	6.279E-05

In the EQ module, it can be seen that the unit is stable for a minimum clock constraint of 75 ps, after which, a single timing violation was found for a faster clock period of 50 ps. The total area of the EQ module stays consistent until a violating path is found. The total power usage of the module increases exponentially until 75 ps, after which the module erroneously decreases its power consumption.

p. 8-Bit GREAT





GREAT	QOR and Area Report		Power Usage by Category (%)			Total Power Usage (W)			
Clock (ps)	Violated Paths	Total Area	Register	Logic	Clock	Leakage	Internal	Switching	Total
1000	0	62.95	27.64%	68.26%	4.10%	9.301E-08	4.842E-06	3.752E-06	8.687E-06
500	0	61.997	29.54%	66.09%	4.37%	8.653E-08	8.881E-06	7.303E-06	1.627E-05
400	0	61.997	29.57%	66.07%	4.38%	8.653E-08	1.110E-05	9.128E-06	2.032E-05
300	0	61.997	29.57%	66.05%	4.38%	8.653E-08	1.480E-05	1.217E-05	2.706E-05
275	0	61.997	29.57%	66.05%	4.38%	8.653E-08	1.615E-05	1.328E-05	2.951E-05
250	0	61.997	29.57%	66.05%	4.38%	8.653E-08	1.615E-05	1.328E-05	2.951E-05
225	0	61.997	29.58%	66.04%	4.39%	8.653E-08	1.973E-05	1.623E-05	3.605E-05
200	0	61.997	29.58%	66.03%	4.39%	8.653E-08	2.220E-05	1.826E-05	4.054E-05
175	0	61.997	29.58%	66.03%	4.39%	8.653E-08	2.537E-05	2.086E-05	4.632E-05
150	0	61.997	29.59%	66.02%	4.39%	8.653E-08	2.960E-05	2.434E-05	5.403E-05
125	0	61.997	29.48%	66.30%	4.21%	9.066E-08	3.692E-05	3.056E-05	6.757E-05
100	0	81.176	26.42%	69.81%	3.77%	1.040E-07	5.084E-05	4.339E-05	9.433E-05
75	0	79.443	24.61%	71.75%	3.65%	1.291E-07	4.743E-05	4.995E-05	9.751E-05
50	1	98.688	18.55%	78.88%	2.57%	2.982E-07	5.502E-05	8.288E-05	1.382E-04

For the GREAT module, a minimum clock period of 75 picoseconds was achieved without any violating paths. At 50 picoseconds, 1 violated path was found, and both the area and total power consumption became erroneous. Throughout the cycle time constraints, the total area has stayed consistent at around 62 units. After reaching time constraints of 100 picoseconds, the total area increased to around 81 units after which it finally decreased down to 79 units at the minimum clock time constraint.

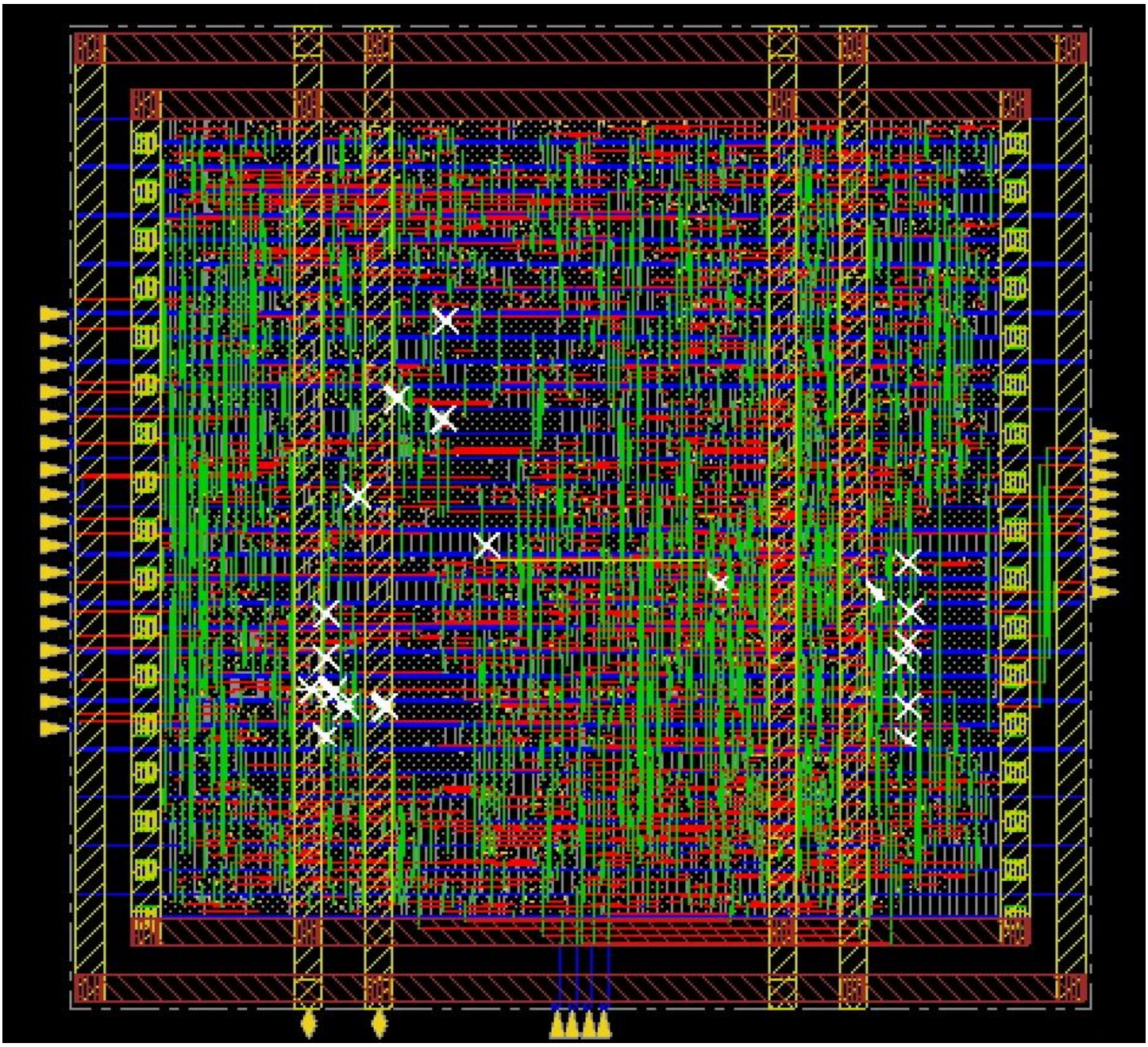
IV. Synthesis Dependencies on Cycle Time

There is a clear dependence between the synthesized component area and power consumption and the cycle time constraint. Through the simulations, it can be seen that as the cycle time constraint decreases from 1000 picoseconds down to 25 picoseconds, both the area consumption and power consumption increase. The power consumption continues to increase exponentially regardless of the size of the synthesized module. However, the increase in area depends on the size and complexity of logic within the module. For smaller modules, the increase in area is relatively linear. However, for larger, more complex modules such as the ALU and the DIV module, the increase is exponential. This difference can be clearly seen in the area and power consumption plots above.

Another phenomenon that can be observed is that the average fan out along the most limiting path for each functional unit increases as the cycle time period is decreased. This is why as the clock period continuously decreases, the total area may slightly increase to accommodate a larger fan out. As the internal and switching power consumptions were tabulated above, it can be seen that in general, as the

clock cycle constraint is decreased both the switching power consumption and internal power consumption increase. Furthermore, the switching power consumption increases at a much faster rate than the internal power consumption, as the switching speed is directly dictated by the clock speed.

Project Part II : Physical Layout of the 8-Bit ALU



As shown above, once the minimum time constraint was found for the 8-Bit ALU, the layout was generated using Innovus.