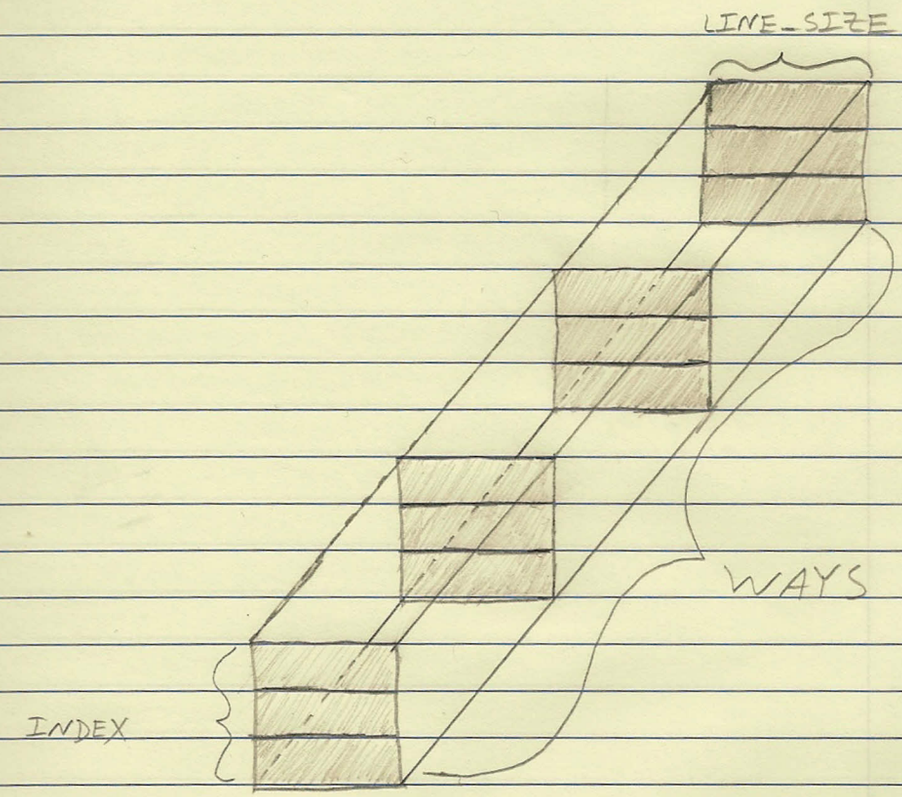
Cache Structure

The cache will be implemented as a 2-D array. It will be of the form:

reg [LINE-SIZE-1:0] cache [INDEX-1:0][WAYS-1:0]



LINE-SIZE = Replacement Bits* + Dirty Bit + Valid Bit + Tag Bits + Data Bits

INDEX = Number of lines per way.

WAYS = Number of ways an item with the same index can be stored.

* For PLRU, there will be a separate array that maintains which line to replace when all ways are occupied.