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Seat No.	
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**[5252]-564**

**S.E. (Computer) (I Sem.) EXAMINATION, 2017**  
**COMPUTER ORGANIZATION AND ARCHITECTURE**  
**(2015 PATTERN)**

**Time : Two Hours**

**Maximum Marks : 50**

- N.B. :—**
- (i) Neat diagrams must be drawn wherever necessary.
  - (ii) Figures to the right side indicate full marks.
  - (iii) Use of calculator is allowed.
  - (iv) Assume suitable data if necessary.

1. (a) Multiply the following using Booth' algorithm. [6]  
Multiplicand = + 11  
Multiplier = - 6
- (b) Explain in brief RAID levels in detail. [6]

*Or*

2. (a) Explain in detail IEEE standards for representing floating point numbers in the following formats. [6]  
(1) Single Precision  
(2) Double Precision [6]
- (b) Explain cache updating policies in detail. [6]
3. (a) What is the use of DMA ? Explain cycle stealing in DMA. [6]  
(b) What is machine instruction ? Explain any *three* types of operations. [6]

*Or*

4. (a) Compare memory mapped I/O and I/O mapped I/O. [06]

P.T.O.

- (b) Explain the following addressing modes with *one* example each : [6]
- (i) Displacement Addressing
  - (ii) Register Indirect
5. (a) List the features of 8086 microprocessor. [7]
- (b) Write a short note on superscalar execution and superscalar implementation. [6]
- Or*
6. (a) Explain the instruction pipelining. [6]
- (b) Draw and explain architecture of 8086. [7]
7. (a) Write a control sequence for the following instruction for single bus organization : ADD (R3), R1 [6]
- (b) Explain in detail state table design method for hardwired control design. [7]
- Or*
8. (a) Draw and explain in detail block diagram of hardwired control unit. [7]
- (b) List the applications of microprogramming. [6]